Inverter for Motor Control

600V IGBT Gen.3 Intelligent Power Module (IPM) Application Note BM6437*S/-VA

Gen.3 IGBT-IPM built in Gate driver, Bootstrap Diode, IGBT device and Fast Recovery Diode for regeneration into one package.
Gen.3 IGBT-IPM inherited strong features from Gen.2 IPM have been improved.

This application note describes Gen.3 IGBT-IPM features and design method to get the best performance.

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1. Introduction

1.1. Application

- AC100 to 240Vrms(DC voltage less than 400V) class motor control
- Motor control for White Goods (Air conditioner, Washing Machine, Refrigerator)

1.2. Lineup

Series	Part Number	Rating
Temperature Output function Thermal Shutdown function	BM64374S-VA	15A/600V
	BM64375S-VA	20A/600V
	BM64377S-VA	30A/600V
	BM64378S-VA	35A/600V

-VA：Long Pin type

Table 1.2.1 Lineup table

1.3. Features

- 3-phase DC/AC inverter
- 600V/15A,20A,30A,35A
- Low Side IGBT Open Emitter
- Built-in Bootstrap Diode
- High side IGBT Gate driver(HVIC)
  SOI(Silicon On Insulator) Process
  Drive Circuit
  High Voltage level Shifting
  Current Limit for Bootstrap Diode
  Control Supply Under-Voltage-Lockout(UVLO)
- Low side IGBT Gate Driver(LVIC)
  Drive Circuit
  Short Circuit Current Protection(SCP)
  Control Supply Under-Voltage-Lockout(UVLO)
  Thermal Shutdown(TSD)
  Temperature Output by Analog Signal(VOT)
- Fault Signal(LVIC)
  Corresponding to SCP, TSD, UVLO Fault(Low Side IGBT)
- Input interface 3.3V, 5V Line
- UL acquisition: UL1557 File E468261

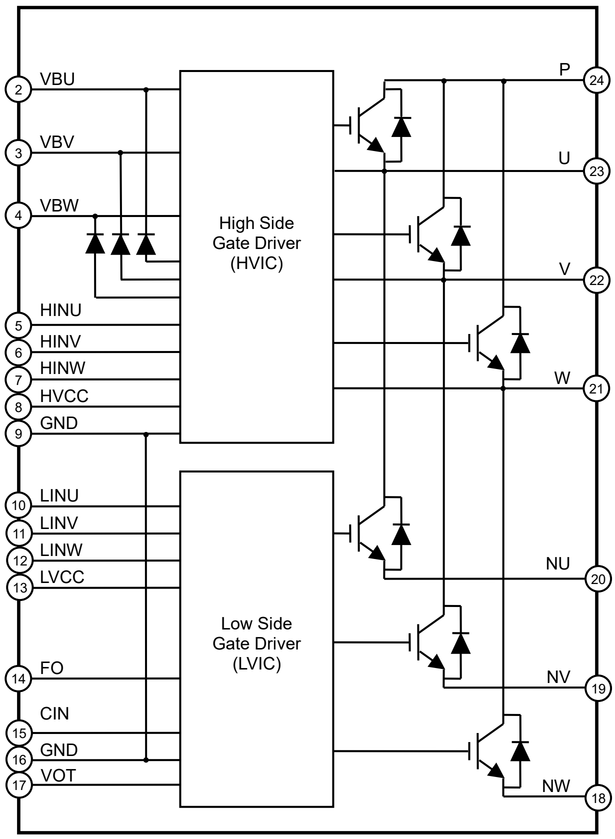


Figure 1.3.1 Block Diagram

1.4. The differences between previous series

Major differences between Gen.3 IGBT-IPM (BM64*7*) and Gen.2 IGBT-IPM (BM64*6*) are described as below.
For more details, refer to device datasheet.

Function	Gen.2 IGBT IPM	Gen.3 IGBT IPM	Related Topics
Current range	15A/20A	15A/20A/30A/35A	1.3
Temperature Monitoring Accuracy	VOT = 2.77±0.14V (at LVIC = 90°C) Equivalent to ±6 °C	VOT = 2.77±0.05V (at LVIC = 90°C) Equivalent to ±2 °C	2.2.4
Thermal Protection	TSD products and VOT products	TSD & VOT products	1.2
Fault Output Identification	Not support (minimum FO assertion period SCP: min 20μs UVLO: min 20μs TSD: min 20μs)	Support (minimum FO assertion period SCP: min 45μs UVLO: min 90μs TSD: min 180μs)	2.2.5
Extension of the disabling IGBT (Fault pulse tuning)	Not Support	Support	2.2.5
Product Identification	Not Support	Support Identify by impedance between HINU - GND,HINV - GND,HINW – GND during power off	2.2.6
Trip voltage for Short Circuit Protection	0.48V ±0.025V (Products with VOT) 0.48V ±0.05V (Products with TSD)	0.480V ±0.025V	-

Table 1.4.1 Differences of function

2. Specifications

2.1. Maximum Ratings

Table 2.1.1 describes Specifications of BM64375S as an example.

Inverter Part

Item		Symbol	Ratings	Unit	Description
Supply Voltage		V_P	450	V	This value is the maximum voltage which can be biased between P-NU, NV, NW without the switching operation. A voltage suppressing circuit is necessary if P-NU, NV, NW voltage exceeds this value.
Supply Voltage(surge)		$V_{P(surge)}$	500	V	This value is the maximum P-NU, NV, NW surge voltage which can be applied during switching operation. A snubber circuit lower pattern inductance is necessary if P-NU, NV, NW voltage exceeds this value.
Collector-emitter Voltage		V_{CES}	600	V	The maximum sustained collector-emitter voltage of built-in IGBT
Each IGBT Collector Current	continuous	I_C	±20	A	Continuous DC current (T_C = 25°C)
	peak	I_{CP}	±40	A	Pulse(less than 1ms) current(T_C = 25°C)
Junction Temperature		Tjmax	150	°C	Maximum junction temperature is150°C (@T_C ≤ 100°C) Average junction temperature should be limited to 125°C (@T_C ≤ 100°C) for the safe operation. Power chips are not damaged immediately at 150°C, its power cycles are reduced.

Control Part

Item	Symbol	Ratings	Unit	Description
Control Supply Voltage	V_{CC}	20	V	Applied between the HVCC and GND pins, the LVCC and GND pins.
Floating Control Supply Voltage	V_{BS}	20	V	Applied between the VBU and U pins, the VBV and V pins, and the VBW and-W pins.
Control Input Voltage	V_{IN}	-0.5 to V_{CC} +0.5	V	Applied between the HINx, LINx and GND pins. (x = U,V,W)
Fault Output Supply Voltage	V_{FO}	-0.5 to V_{CC} +0.5	V	Applied between the FO and GND pins
Fault Output Current	I_{FO}	1	mA	Sink current at the FO pins
Current Sensing Input Voltage	V_{CIN}	-0.5 to +7.0	V	Applied between the CIN and GND pins
Temperature Output Voltage	V_{OT}	-0.5 to +7.0	V	Applied between the VOT and GND pins

Bootstrap Diode Part

Item	Symbol	Ratings	Unit	Description
Reverse Voltage	V_{RB}	600	V	The maximum sustained reverse voltage of built-in bootstrap diode.
Junction Temperature	T_{jmaxD}	150	°C	Maximum junction temperature is 150°C (@T_C ≤100°C) Average junction temperature should be limited to 125°C (@T_C≤100°C) for the safe operation.

Entire System

Item	Symbol	Ratings	Unit	Description
Self Protection Supply Voltage (SCP Capability)	$V_{P(PROT)}$	400	V	Maximum supply voltage for turning off IGBT safely in case of short circuit or over current. (under the conditions of V_{CC} = 13.5 to16.5V, non-repetitive, less than 2μs)
Module Case Temperature	T_C	-25 to +115	°C	Defined as the case temperature just over the chip. Please measure T_C by mounting a thermocouple on the heat sink surface at the defined position. (See Figure 2.1.1)
Isolation Voltage	V_{iso}	1500	V_{rms}	Isolation voltage between all shorted pins and the ceramic parts (Al_2O_3) of IPM. In the case of using the flat heat sink, isolation voltage is 1500Vrms because of discharge between pins and the flat heat sink. If convex shape heat sink will be used for enlarging clearance between pins and the heat sink (2.5mm or more is recommended), isolation voltage is 2500Vrms. (See Figure 2.1.2). IPM is certificated by UL1557 at the condition of 2500Vrms with a convex shape heat sink.

Table 2.1.1 Absolute Maximum Ratings of BM64375S

Tc Detecting Point

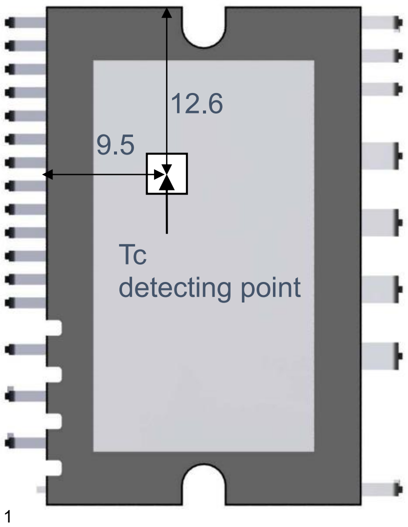


Figure 2.1.1 Tc Detecting Point (unit: mm)

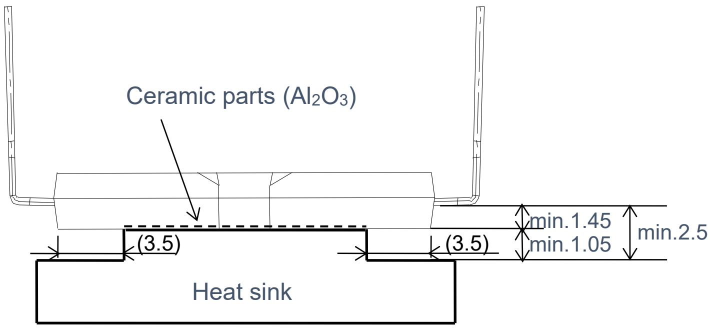


Figure 2.1.2 In the case of using the convex heat sink (unit: mm)

Thermal Resistance

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Junction to Case Thermal Resistance	$R_{th(j-c)\_IGBT}$	-	-	3.0	°C/W	Inverter IGBT(1/6 Module)
	$R_{th(j-c)\_FWD}$	-	-	3.9	°C/W	Inverter FWD(1/6 Module)

The above specification shows the thermal resistance between chip junction and the case at steady state. The thermal resistance saturates in about 10s. The unsaturated thermal resistance or transient thermal impedance is reported in Figure 2.1.3.
Zth (j-c)* is the normalized value of the transient thermal impedance. (Zth (j-c)* = Zth (j-c) / Rth (j-c)).
For example, the IGBT transient thermal impedance of BM64375S in 0.3s is 3.0°C/W ×0.8 = 2.4°C/W.

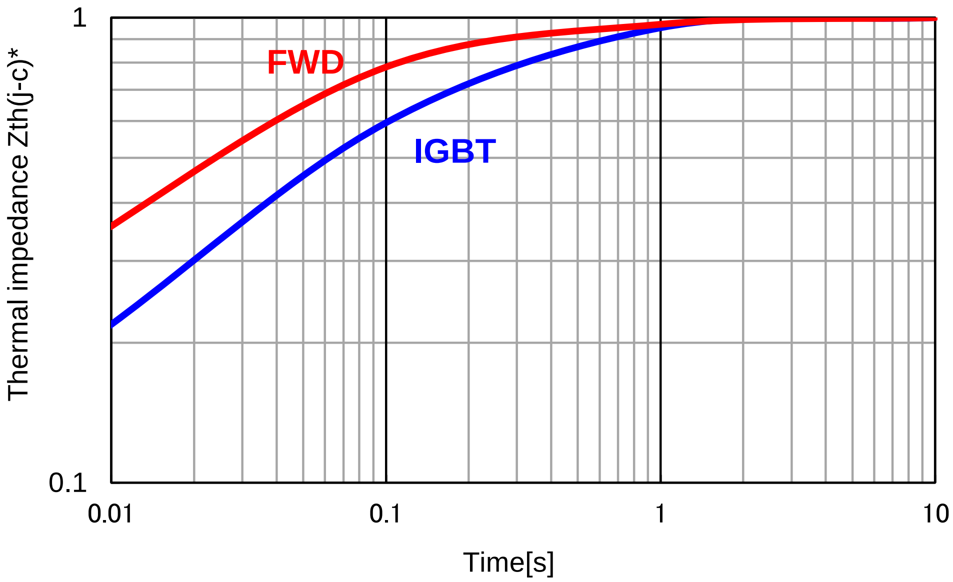


Figure 2.1.3. Transient Thermal Impedance

2.2. Protection Features and Operating Sequence

2.2.1. Short Circuit Protection (SCP)

The IPM's short circuit protection circuit detect the overcurrent by comparing the CIN pin voltage generated at the external shunt resistor.

After the detection of an overcurrent, the SCP protection operates, turns off all low side IGBTs and the FO open drain is activated. In order to prevent malfunction by recovery current or switching noise, it is recommended to mount an RC filter with a 1.0μs time constant, as close as possible to the CIN pin.

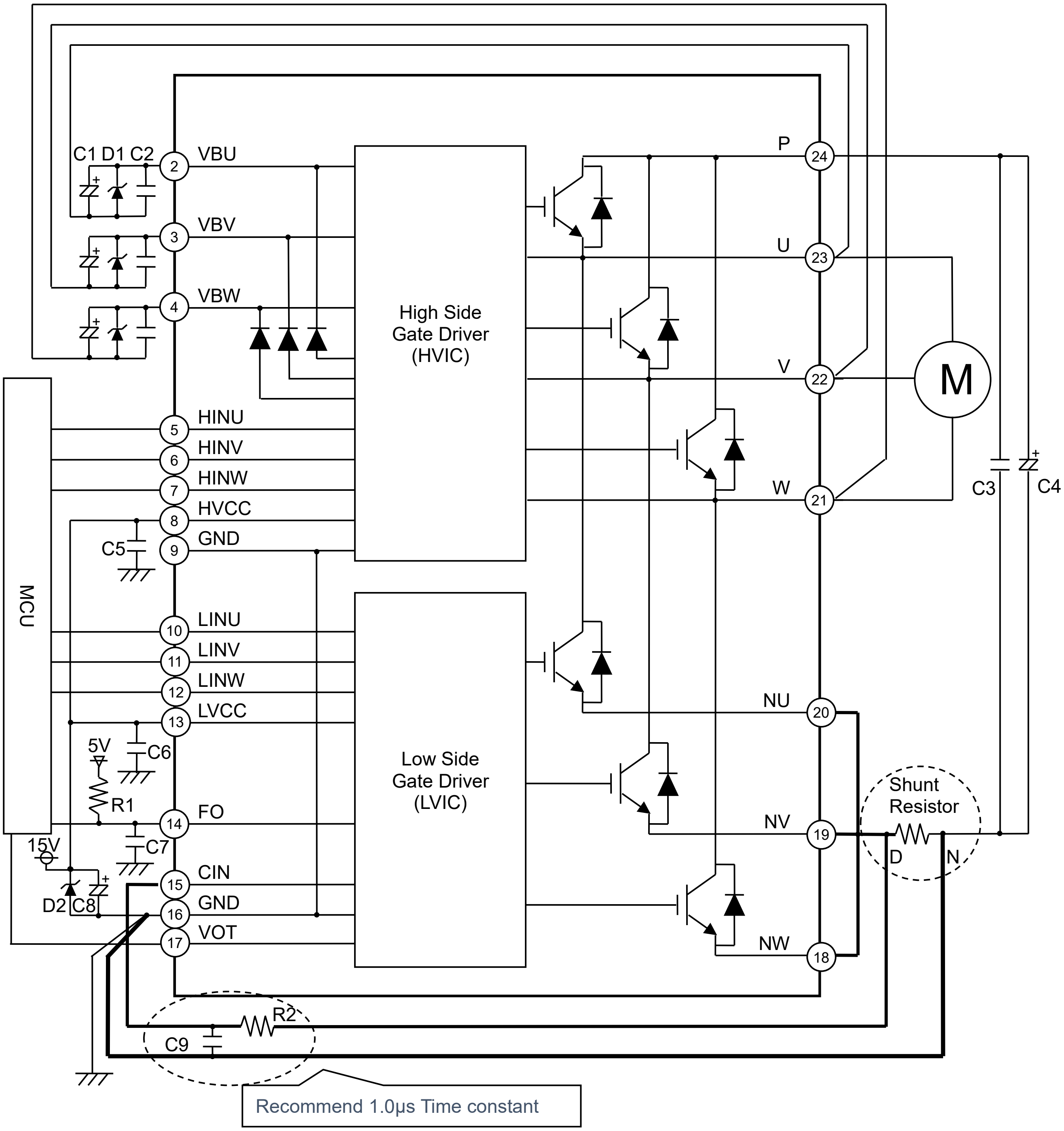


Figure 2.2.1 Short Circuit Current Protection

■Short Circuit Current Protection Timing Chart (protection with the external shunt resistor and RC filter)

a1. Normal operation: IGBT on and outputs current I_C.

a2. Short circuit current detection (trigger SCP)
It is recommended to set RC time constant shorter than 2.0μs (1.0μs recommended).

a3. Turn off of all low side IGBT's gate (soft turn off).

a4. All low side IGBTs are off.

a5. The FO open drain is activated
(SCP = H ≤ 45μs: the FO open drain is activated 45μs (Min),
SCP = H > 45μs: the FO open drain is activated during SCP = H).

a6. LIN = L

a7. LIN = H, but all IGBTs keep OFF during SCP = H.

a8. The FO open drain is deactivated, but IGBTs stay off until the next LIN positive edge (LIN = L→H).
IGBT of each phase can return to normal state by triggering each LIN positive edge.

a9. Normal operation: IGBT on and outputs current I_C.

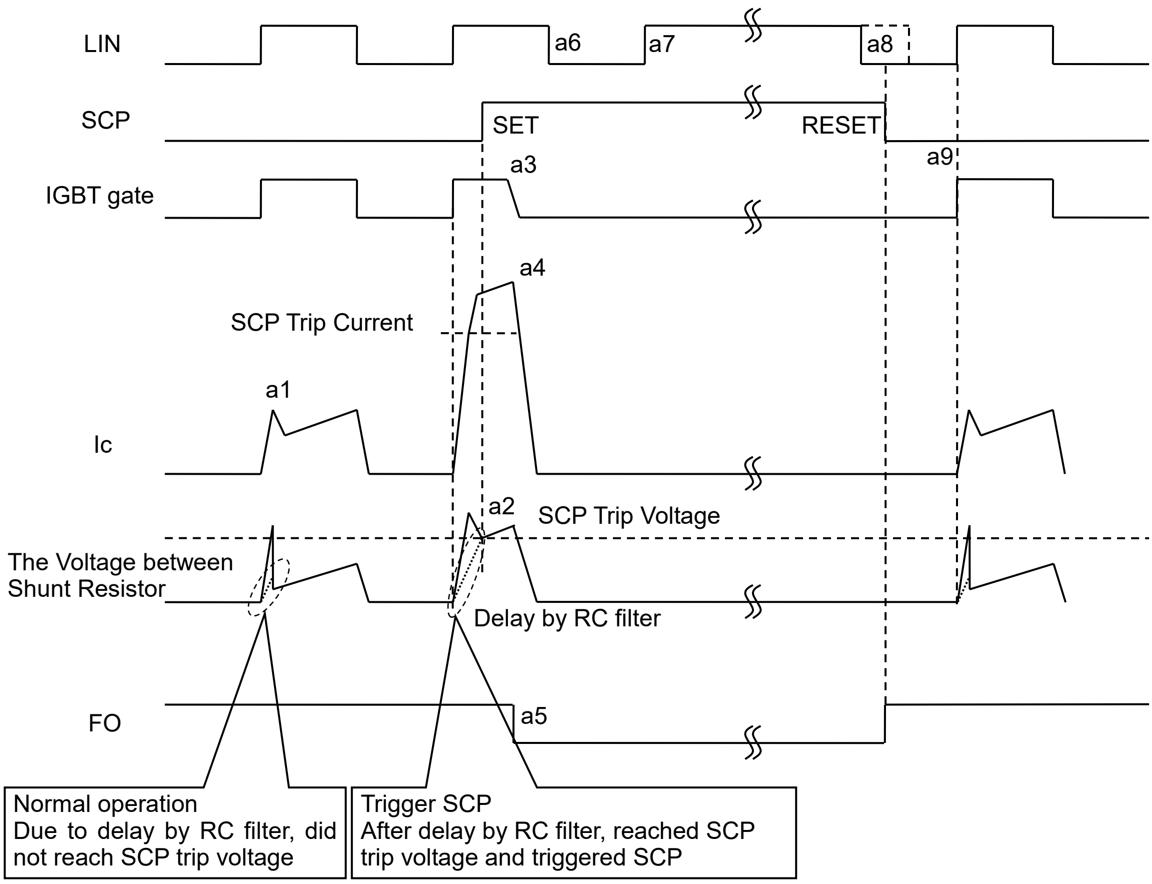


Figure 2.2.2 SCP Timing chart

SCP works switching off low side IGBTs only.
In case of trigged SCP and the FO open drain is activated, please stop controlling IPM quickly to avoid the abnormal state.

■Setting the Value of Shunt Resistor

The value of shunt resistor R_{SHUNT} is set according to following equation. The calculation is based on the short circuit current protection trip voltage V_{SC} and the protection current setting value I_{SCP}

$$R_{SHUNT} = V_{SC} / I_{SCP}$$

The maximum protection current setting value I_{SCP} (max) should be set less than the IGBT minimum saturation current considering variation of shunt resistor or V_{SC}.

In this example we calculate R_{SHUNT} for I_{SCP} = 34A (DC rate current: 20A × 1.7) of BM64375S.

Table 2.2.1 shows variation of V_{SC} (Tj = 25°C、V_{CC} = 15V)

Item	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
SCP Trip Voltage	V_{SC}	0.455	0.480	0.505	V	

Table 2.2.1 Specification of SCP Trip Voltage

The range of the protection current setting value I_{SCP} can be calculated using the following equations

$I_{SCP}(Min) = V_{SC}(Min) / R_{SHUNT}(Max)$・・・(a)

$I_{SCP}(Typ) = V_{SC}(Typ) / R_{SHUNT}(Typ)$・・・(b)

$I_{SCP}(Max) = V_{SC}(Max) / R_{SHUNT}(Min)$・・・(c)

According to (c)

$34A = 0.505V / R_{SHUNT}\ (Min)$
$R_{SHUNT}\ (Min) \approx 14.85m\Omega$

If the shunt resistance precision is within ±5%,

$R_{SHUNT}\ (Typ) \approx 14.85m\Omega / 0.95 \approx 15.63m\Omega$
$R_{SHUNT}\ (Max) \approx 15.63m\Omega \times 1.05 = 16.41m\Omega$

So the range of I_{SCP} is shown in Table 2.2.2 (at Tj = 25°C、V_{CC} = 15V)

Item	Min	Typ	Max
R_{SHUNT} setting range	14.85mΩ	15.63mΩ	16.41mΩ
I_{SCP} operation range	27.7A	30.7A	34.0A

Table 2.2.2 Operative SCP Range

There is the possibility that the actual SCP trip level becomes less than the calculated value. This is considered due to the resonant signals caused mainly by parasitic inductance and capacity. We recommend to make a confirmation of the resistance by prototype evaluation.

■Setting the RC Filter Time Constant

It is necessary to set the RC filter of SCP sensing circuit in order to prevent malfunction of SCP protection due to noise interference. The RC time constant τ depends on the noise interference and the SCSOA of the IPM. (Recommended τ = 1.0µs)

When the voltage drop on the external shunt resistor exceeds the SCP trip voltage (V_{SC}), the time (t_1) that the CIN pin voltage rises to the SCP trip voltage (V_{SC}) can be calculated using the following expression:

$$V_{SC} = R_{SHUNT} \cdot I_C \cdot \{1-\exp(t_1 / \tau)\}$$

$$t_1 = -\tau \cdot \ln(1- V_{SC} / R_{SHUNT} \cdot I_C)$$

V_{SC} : SCP trip voltage
I_C : IGBT peak current
τ : RC filter time constant
t_1 : The time to supply V_{SC} voltage to CIN pin

The IPM internal time delay (t_2) to shut down IGBT gate is shown in Table 2.2.3.

Item	Min	Typ	Max
IPM internal delay time	-	-	0.65µs

Table 2.2.3 IPM internal delay time

Therefore, the total delay time (t_{total}) in the SCP chain is the following:

$$t_{total} = t_1 + t_2$$

After validation by actual environment, please finalize RC filter time constant to keep t_{total} within IGBT SCSOA.

2.2.2. Under Voltage Lockout (UVLO)

The reduction of control power supply voltage causes the gate voltage of IGBTs to drop and IGBTs cannot operate properly. To avoid this the UVLO function is implemented.

Both the floating power supply (V_{BS}) of HVIC and the control power supply (V_{CC}) of LVIC have UVLO function. However, only LVIC power supply activate the FO output signal

Table 2.2.4 shows operating behavior at each supply voltage.

Supply voltage[V] (V_{CC}, V_{BS})	Operating Behavior
0 to 4.0	It is recommended to turn on the control power supply before to energize the DC link to avoid IGBTs malfunctions. HVIC and LVIC may not work properly due to out of normal operating voltage range. Protection functions such as UVLO or FO signaling are not guaranteed.
4.0 to V_{CCUVR}(V_{CC}), V_{BSUVR}(V_{BS})	UVLO function and FO signal outputs are active.
V_{CCUVR} to 13.5(V_{CC}) V_{BSUVR} to 13.0(V_{BS})	IGBT can work. However, IGBT conduction and switching losses could increase and the junction temperature could rise.
13.5 to 16.5(V_{CC}) 13.0 to 18.5(V_{BS})	Recommended working conditions.
16.5 to 20.0(V_{CC}) 18.5 to 20.0(V_{BS})	IGBT can works. However, switching speed becomes fast, resulting in noise level increase. The saturation current of IGBT becomes large, resulting in short circuit withstand time reduction.
20.0 or above	HVIC, LVIC may be destroyed. Using zener diode (1W, 20V to 22V) is recommended.

Table 2.2.4 Operating Behavior versus Control Supply Voltage

■Control Supply (LVCC) Under-Voltage Lockout (UVLO) operating sequence (implemented in LVIC)

b1. Control supply (LVCC) voltage exceeds UVLO release level (V_{CCUVR}), but IGBT turns on by the next ON signal (LIN = L → H). IGBT of each phase return to normal state by LIN ON input signal to each phase.
b2. Normal operation. IGBT ON and output current Ic.
b3. LVCC voltage drops to UVLO trip level (V_{CCUVT}).
b4. All low side IGBTs turn off despite of control input condition.
b5. The FO open drain is activated for (90μs (Min)) : when UVLO = H period of < 90μs, but enabling period is extended while LVCC voltage is below V_{CCUVR}.
b6. LVCC reaches V_{CCUVR}.
b7. Even if LVCC voltage reaches V_{CCUVR}, during LIN = H, IGBTs do not turn on until inputting the next LIN positive edge (LIN = L→H)
b8. Normal operation. IGBT ON and outputs current Ic.

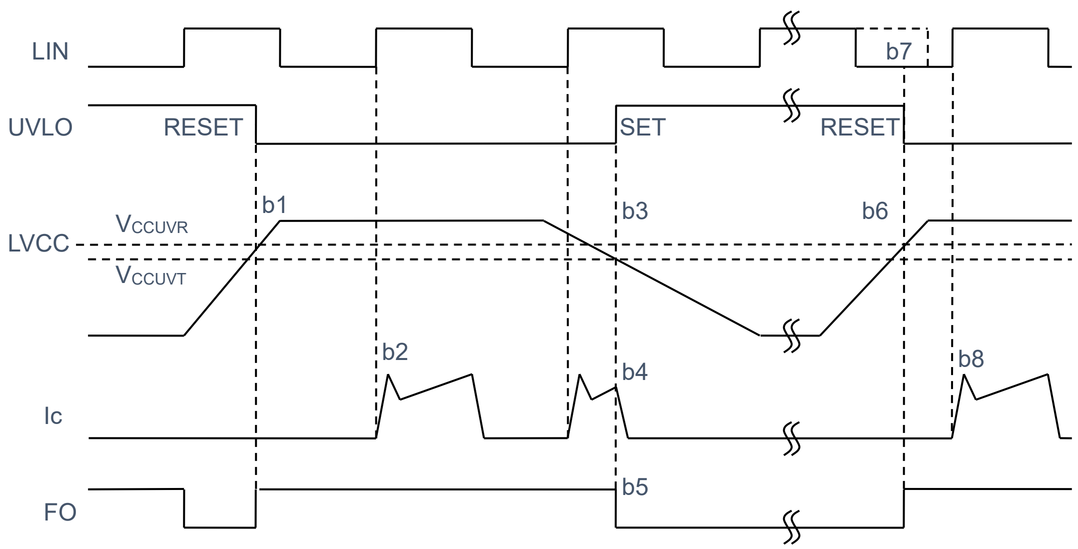


Figure 2.2.3 LVCC UVLO Timing chart

■Control supply (VBS) Under-Voltage Lockout (UVLO) operating sequence (implemented in HVIC)

c1. Control supply (VBS) voltage exceeds UVLO release level (V_{BSUVR}), but IGBT turns on by the next ON signal (HIN = L→H).

c2. Normal operation. IGBT ON and output current Ic.

c3. VBS voltage drops to UVLO trip level (V_{BSUVT})

c4. Only IGBT of the corresponding phase turns off despite control input signal, there is no FO signal output.

c5. VBS reaches V_{BSUVR}.

c6. Even if VBS reaches V_{BSUVR} during HIN = H, IGBTs do not turn on until inputting the next ON signal (HIN = L→H).

c7. Normal operation IGBT ON and outputs current Ic.

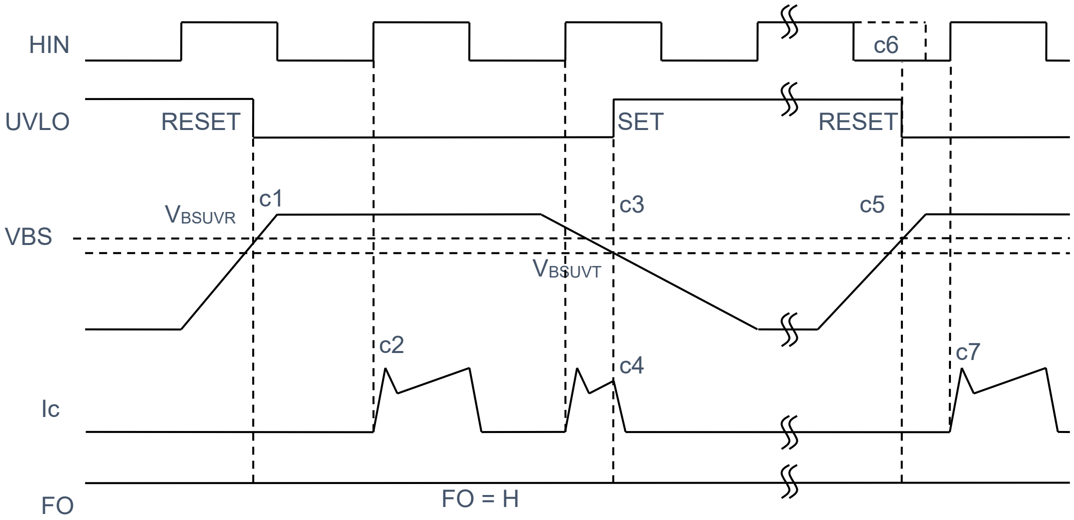


Figure 2.2.4 VBS UVLO Timing chart

2.2.3. Thermal Shutdown (TSD)

IPM has thermal shutdown function by monitor the LVIC temperature. In case the LVIC temperature exceeds and keeps over the thermal shutdown trip level, the FO open drain is activated and all low side IGBTs turn off.

Item	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Trip Temperature	T_{SDT}	115	130	-	°C	Monitor LVIC temperature
Hysteresis Temperature	T_{SDHYS}	-	20	-	°C	Monitor LVIC temperature

Table 2.2.5 Thermal Shutdown temperature

■Thermal Shutdown (TSD) Operating sequence (Monitoring LVIC temperature)

d1. Normal operation. IGBT ON and outputs current Ic.
d2. LVIC temperature (Tj) exceeds thermal shutdown trip level (T_{SDT}).
d3. All low side IGBTs turn off despite control input condition.
d4. The FO open drain is activated for (180μs (Min)) : when TSD = H period of < 180μs, but enabling period is extended while LVIC temperature (Tj) is above T_{SDT}-T_{SDHYS}.
d5. LVIC temperature (Tj) drops to T_{SDT}-T_{SDHYS}.
d6. Even if LVIC temperature (Tj) reaches T_{SDT}-T_{SDHYS} during LIN = H, IGBTs do not turn on until inputting the next LIN positive edge (LIN = L→H).
d7. Normal operation: IGBT ON and outputs current I_C.

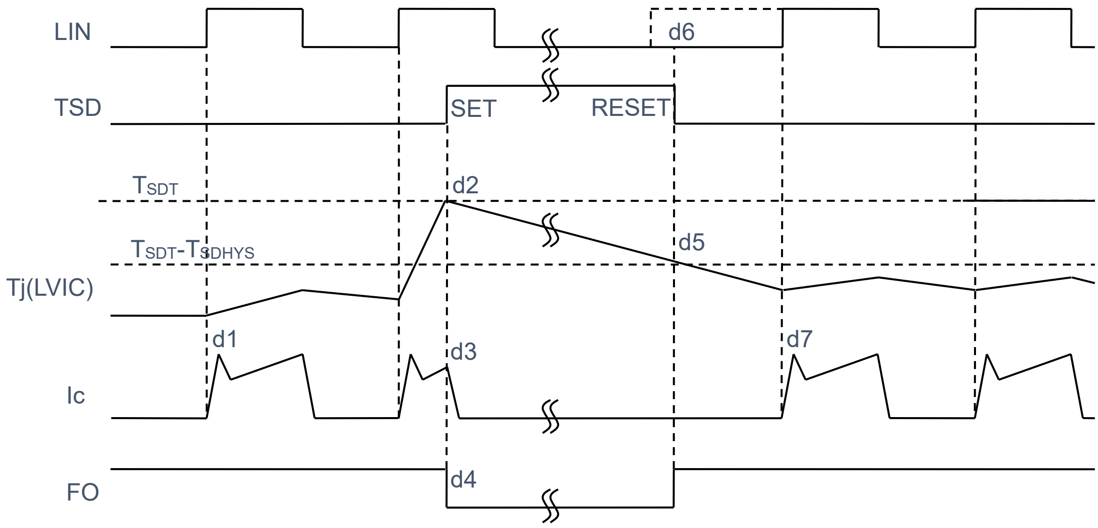


Figure 2.2.5 TSD Timing chart

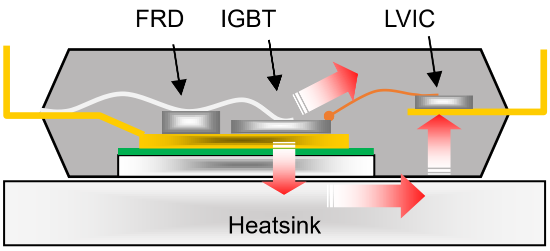


Figure 2.2.6 Heat conduction from power devices

Notice

1) In case of TSD trip and FO output, please stop controlling IPM quickly in order to avoid the device damage.
2) If the cooling system is in abnormal state (e.g. heat sink comes off, fixed loosely, or cooling fan stops) when TSD trips, do not operate the IPM. This may cause the junction temperature of power chips to exceed its maximum Tjmax rating (150°C).
3) TSD function detects LVIC temperature, so it cannot respond to fast temperature increase of power chip. Therefore, TSD will not work properly in the case of events like motor lock or over current.

2.2.4. Temperature Output by Analog Signal (VOT)

The IPM has built in temperature sensor on LVIC, and outputs the analog voltage according to the LVIC temperature. The heat generated at IGBT and FWD transfers to LVIC through the package and outer heat sink. So LVIC temperature cannot respond to fast temperature increase of power chips effectively. (e.g. motor lock, short circuit)

It is recommended to use this function only to protect against slow transient events like cooling system malfunctions and continuous overload operation. (i.e. use the same way a thermistor that was implemented on a heat sink.)

■Temperature Output (VOT) Characteristics

Table 2.2.6 shows the current capability of VOT output. VOT output is created by amplifying the temperature signal as described in Figure 2.2.7. Figure 2.2.7 is an example of VOT output circuit in the case of using an RC filter. The characteristics of VOT output vs. LVIC temperature is linear as in Figure 2.2.11.

	Min
Source current(Note 2)	1.7mA
Sink current(Note 3)	0.1mA

(Note 2) Current flow from VOT to outside
(Note 3) Current flow from outside to VOT

Table 2.2.6 VOT Output Capability (Tc = -25 to 100°C)

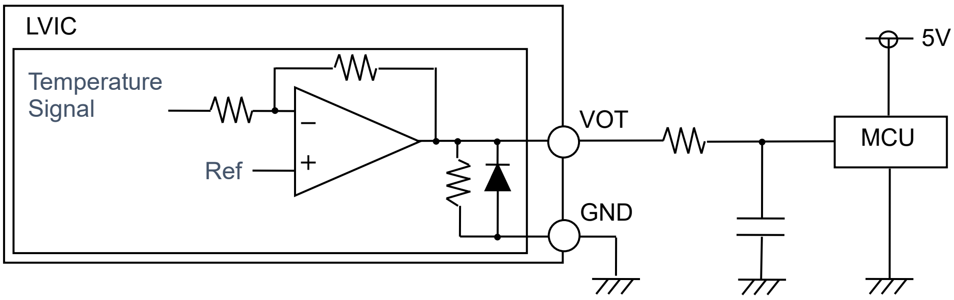


Figure 2.2.7 VOT Output circuit

■Detection of temperature lower than room one

It is recommended to place 5.1kΩ pull down resistor to get linear output characteristics at temperature lower than room temperature. When the pull-down resistor is placed between the VOT and GND pins (control GND), the extra current calculated by VOT output voltage divided by pull down resistance flows as LVIC circuit current continuously.

In the case VOT is used to detect only temperature higher than room temperature, it isn't necessary to insert the pull down resistor.

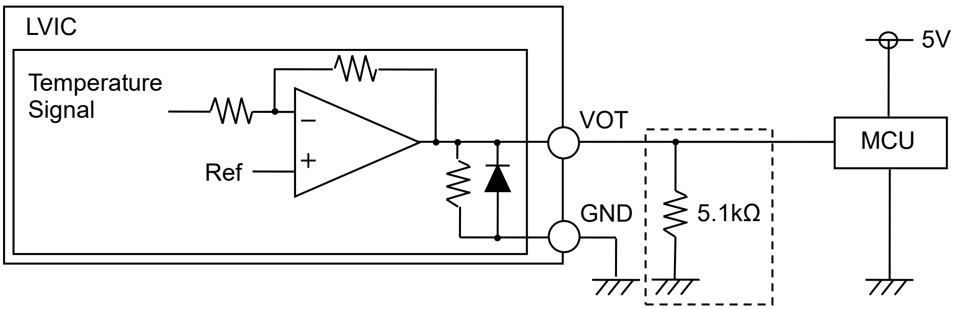


Figure 2.2.8 VOT Output Circuit in the case of temperature detection lower than room one

■Using VOT with low voltage controller (MCU)

In the case of using VOT with low voltage controller (e.g. 3.3V MCU), VOT output might exceed control supply voltage when temperature rises excessively. If system uses low voltage controller, it is recommended to place a clamp diode between controller supply control and VOT output to prevent over voltage.

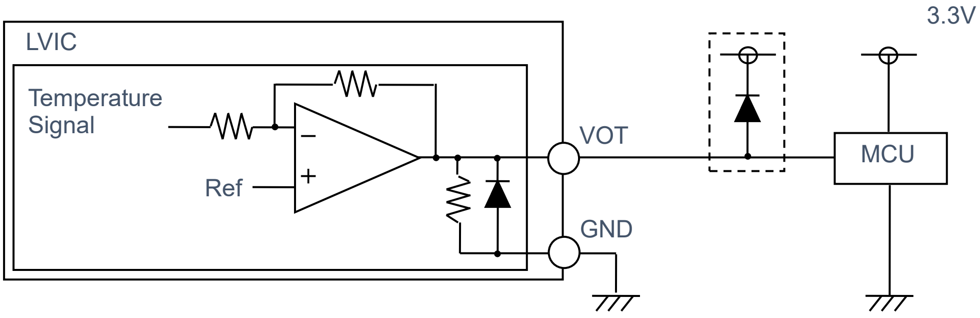


Figure 2.2.9 VOT Output circuit in the case of using with low voltage controller

■VOT protection level exceeding control supply voltage of controller

In the case of using low voltage controller, if it is necessary to set the trip VOT level to control supply voltage (e.g. 3.3V) or higher the VOT output need to be divided by resistance voltage divider circuit and then input to A/D converter on MCU. In that case, sum of the resistance of divider circuit should be as much as 5kΩ.

Considering the divided output voltage not exceeding the supply voltage of controller clamp diode is not necessary. However, the use of the diode is related to the divided output level.

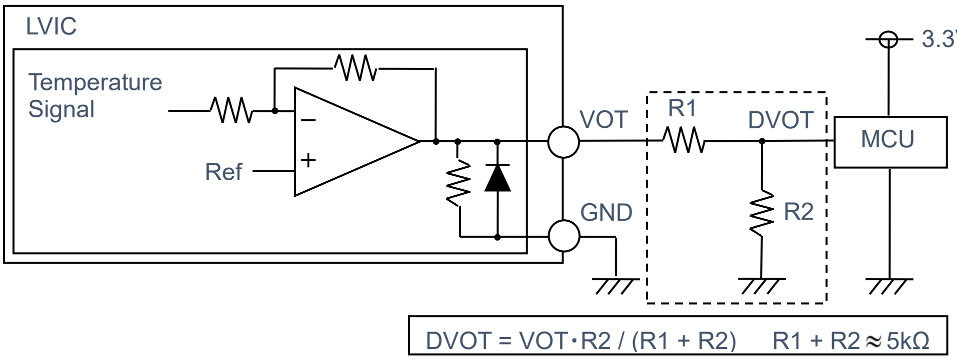


Figure 2.2.10 VOT Output circuit in the case with high protection level

■VOT Output vs LVIC temperature

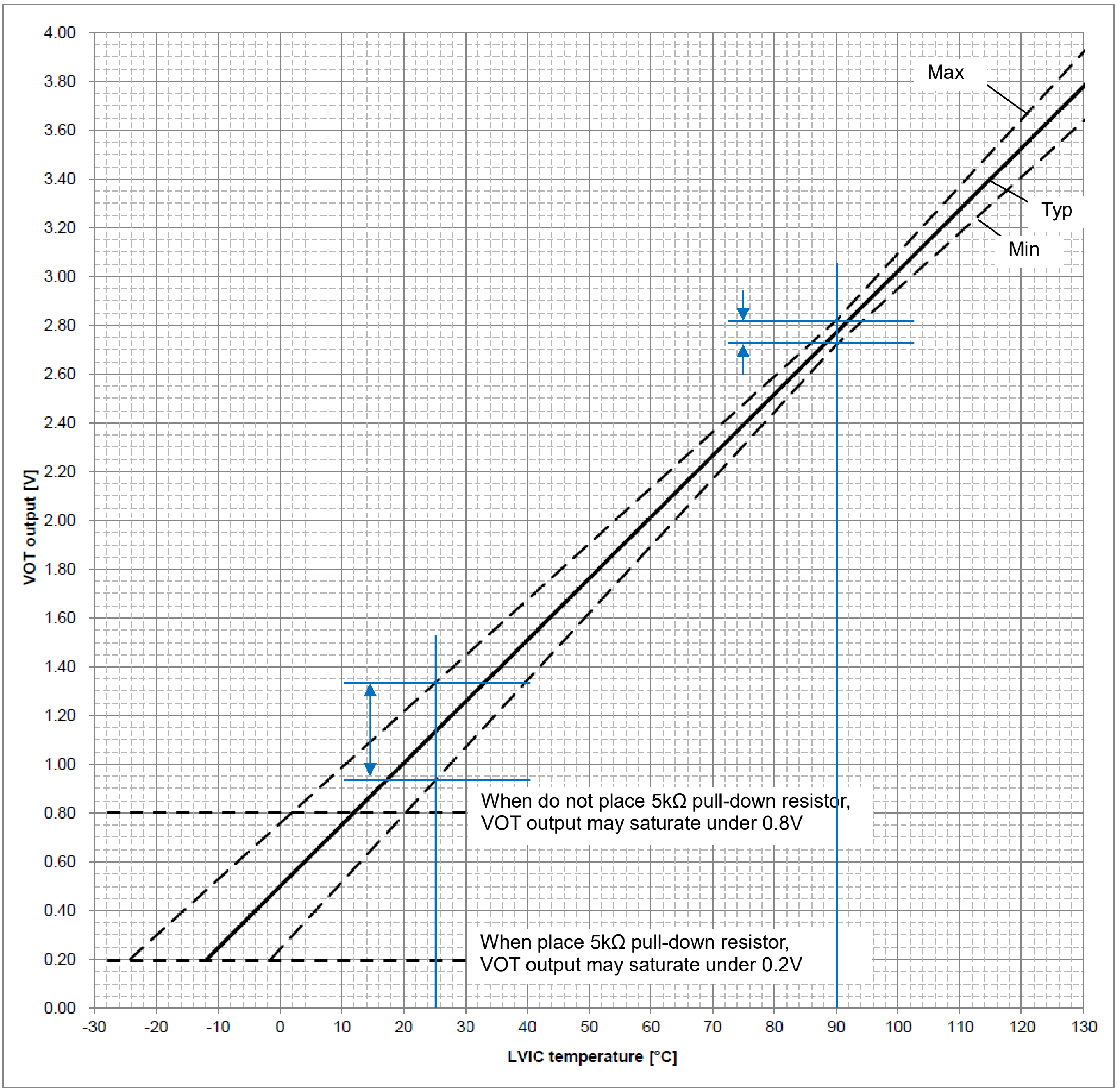


Figure 2.2.11 VOT Output vs LVIC temperature Characteristics

Item	Symbol	Limit			Unit	Condition
		min	typ	Max		
VOT voltage	V_{OT}	2.72	2.77	2.82	V	LVIC temperature 90°C
		0.93	1.13	1.33	V	LVIC temperature 25°C

Table 2.2.7 VOT voltage

2.2.5. Fault Output (FO)

The FO pin consists in open drain output and Schmitt input.

The device supports SCP (Short Circuit Protection), UVLO (Under Voltage Lockout) and TSD (Thermal Shutdown) as protection function for LVIC. When a protection function detect a malfunction, the FO open drain is activated for the period shown in Table 2.2.9 for each factor, and all low side IGBTs turn off in spite of control input condition.

The device supports UVLO (Under Voltage Lockout) as protection function for HVIC, but the FO open drain is not activated. (Refer to 2.2.2).

The IPM monitors the FO pin input voltage in order to turn off low side IGBTs. The low side IGBTs turn off period can be extended by external CR. (Fault pulse tuning)

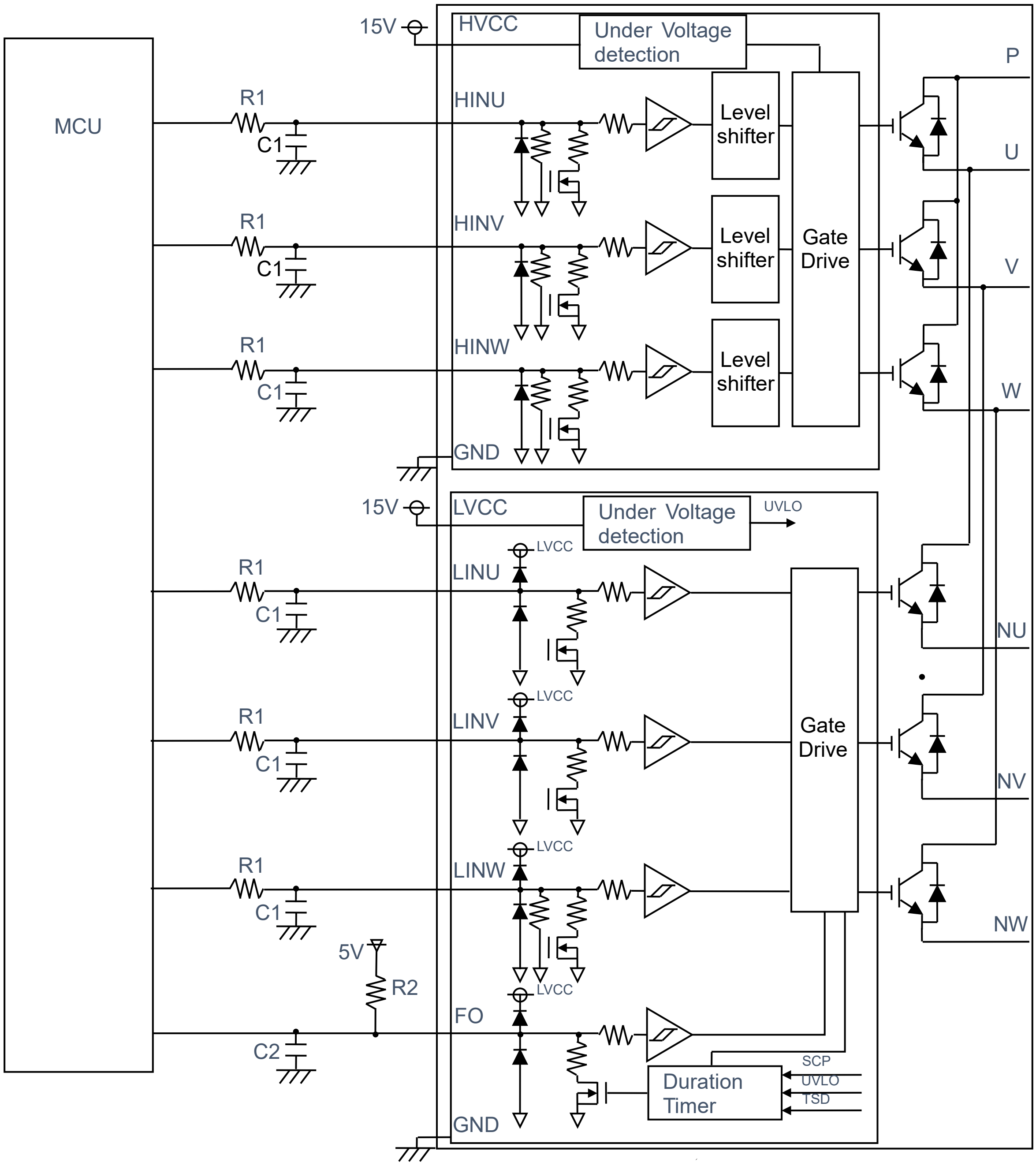


Figure 2.2.12 FO pin and other control pins

■FO pin output feature

The device integrates an open drain output that need to be pulled up to external power supply.

Figure 2.2.13 shows V-I characteristics of the FO pin as a representative example. A maximum sink current: 1mA.

i.e.
An external pull up voltage: 5.0V, pull up resistor: 10kΩ
Minimum high voltage of the FO pin:
5.0V - 10kΩ × 10μA = 4.9V

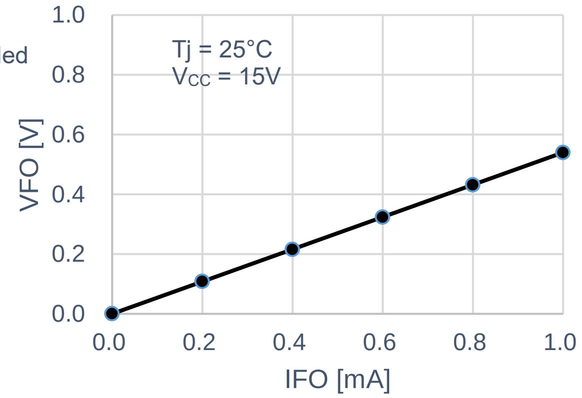


Figure 2.2.13 FO pin V-I characteristics

Item	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Output low voltage	V_{FO}	-	-	0.95	V	I_{FO} = 1mA
Leak current	I_{FOLEAK}	-	-	10	μA	V_{FO} = 5V

Table 2.2.8 FO pin Electric characteristics (output)

FO activated timing

	Event	Event time(min)	FO activated timing(Note 1)
SCP	Short Current Circuit Protection	≤ 45μs	45μs
		> 45μs	SCP time
UVLO	Under Voltage Lockout	≤ 90μs	90μs
		> 90μs	UVLO time (until the LVCC(LVIC) exceeds the V_{CCUVR})
TSD	Thermal Shutdown	≤ 180μs	180μs
		> 180μs	TSD time (until Tj(LVIC) is below the T_{SDT}-T_{SDHYS})

(Note 1) No external RC component on the FO pin

Table 2.2.9 FO timing

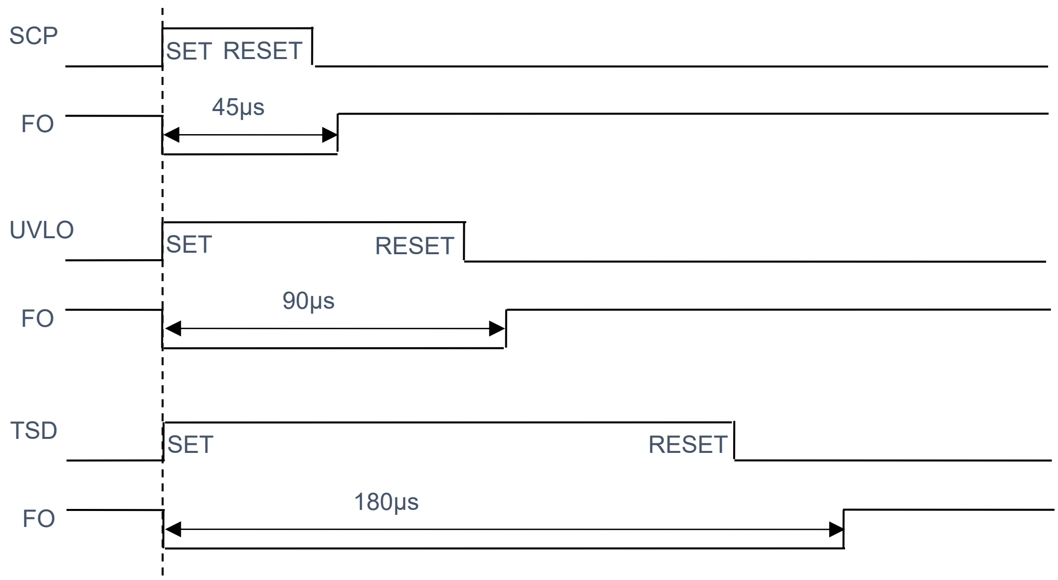


Figure 2.2.14 FO activated timing chart (min)

■The FO pin output feature

Item	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
H input threshold voltage	V_{INH}	-	-	2.6	V	
L input threshold voltage	V_{INL}	0.8	-	-	V	
Input hysteresis voltage	V_{HYS}	-	0.25	-	V	

Table 2.2.10 FO pin Electric characteristics (input)

The low side IGBTs turn off period can be extended by tuning charge time of C2 by placing external C2 and R2. This is useful for providing a SCP information of a very short time (min 45μ) when implemented with isolation products that have a long delay such as photo coupler..

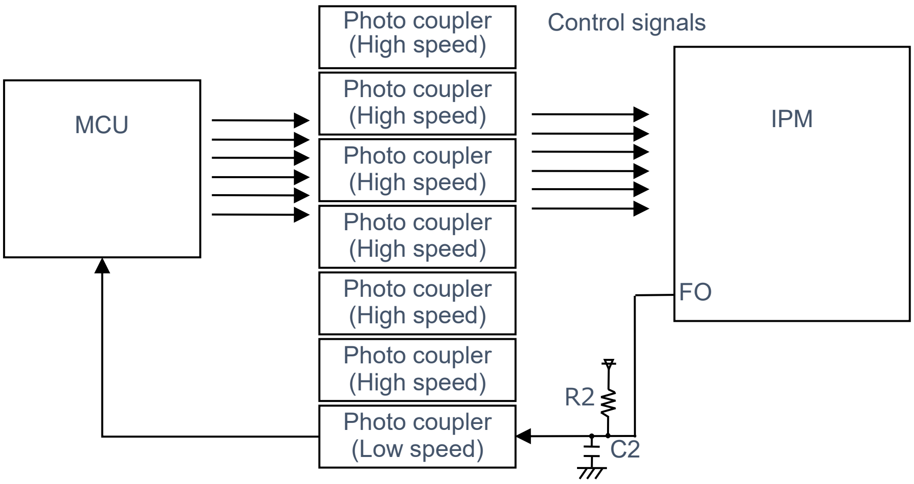


Figure 2.2.15 Extension IGBT turn off period

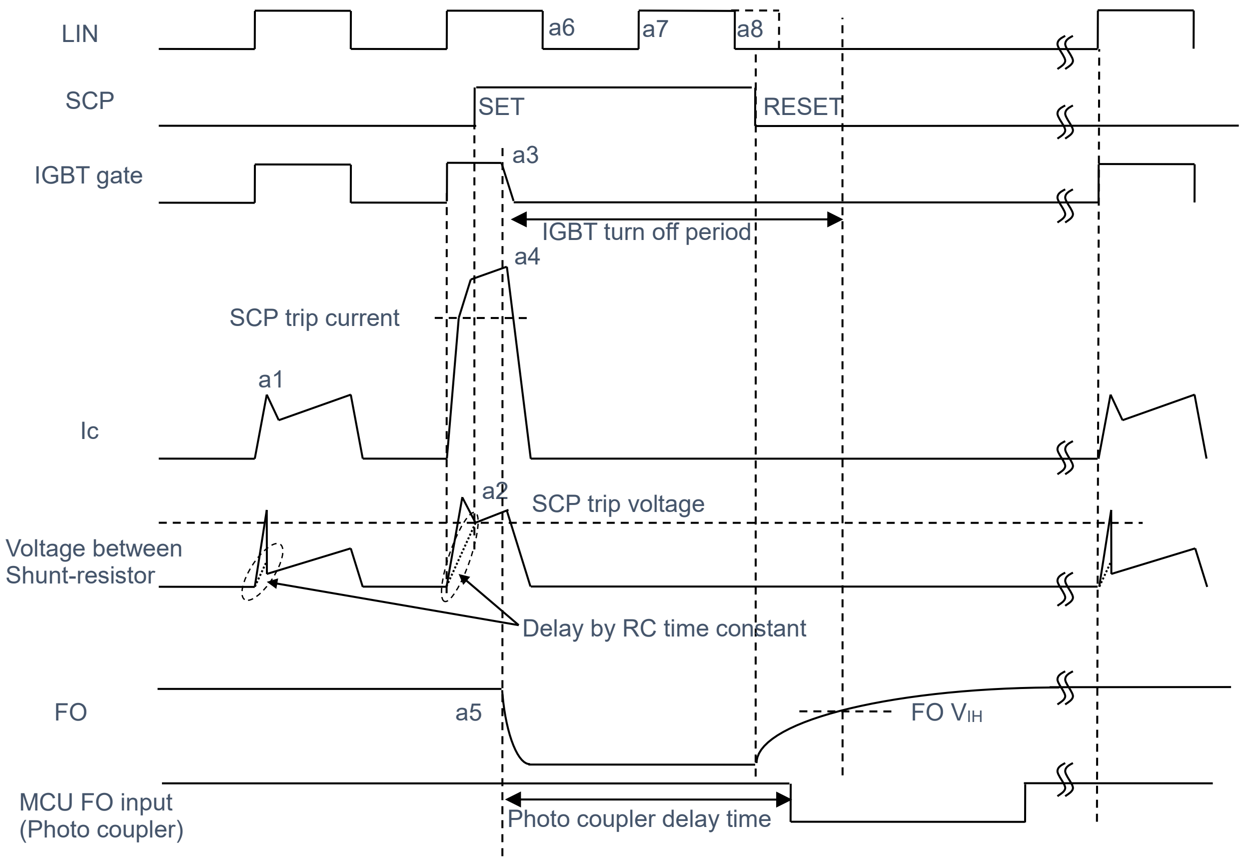


Figure 2.2.16 Extension IGBT turn off period timing chart

2.2.6. Control inputs (HINU, HINV, HINW, LINU, LINV and LINW)

Figure 2.2.12 FO pin and other control pins shows a typical control pin connection.
HINU, HINV, HINW, LINU, LINV and LINW pins are pulled down by 3.3/5.0/7.1kΩ (min/typ/max) internally.
An additional filter can be used to reduce the noise, please make sure that R1 C1 constant meets input threshold voltage in proper timing.

Item	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
H input current	I_{INH}	0.7	1.0	1.5	mA	V_{IN} = 5V
L input current	I_{INL}	-10	-	-	μA	V_{IN} = 0V
H input threshold voltage	V_{INH}	-	-	2.6	V	
L input threshold voltage	V_{INL}	0.8	-	-	V	
Input hysteresis voltage	V_{HYS}	-	0.25	-	V	

Table 2.2.11 Control input, HINU, HINV, HINW, LINU, LINV, LINW Specification

When there is no power at HVCC, Table 2.2.12 shows the input resistance value of HINU, HINV and HINW on each product respectively.

Series	Part Number	Rating	Input resistance(kΩ)(Note 1) During no power at HVCC								
			5:HINU – 9 or 16:GND			6:HINV – 9 or 16:GND			7:HINW – 9 or 16:GND		
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
Temperature Output function Thermal Shutdown function	BM64374S-VA	15A/600V	17.5	25	34	70	100	136	70	100	136
	BM64375S-VA	20A/600V	35	50	68						
	BM64377S-VA	30A/600V	70	100	136						
	BM64378S-VA	35A/600V	140	200	272						

Table 2.2.12 Lineup table

-VA：Long Pin type

(Note 1) When power on at HVCC, input resistance shows 3.3/5.0/7.1kΩ (min/typ/max).
Depending on the connection method of the +/- terminal of the instrument, the resistance may be smaller than the actual value.

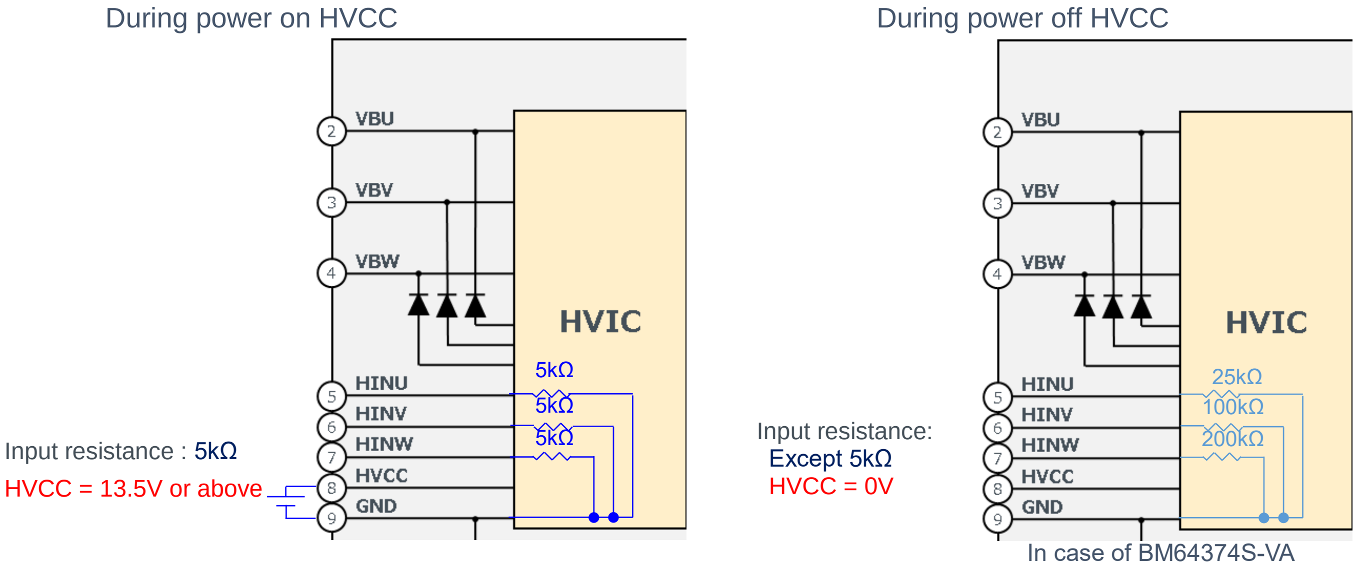
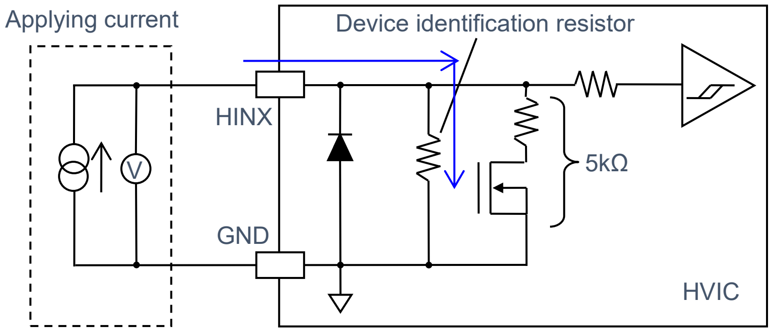


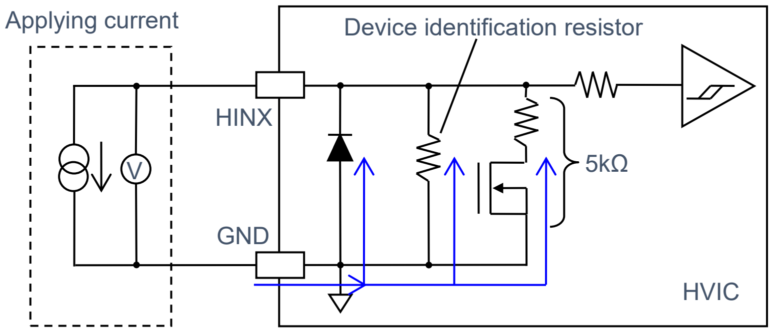
Figure 2.2.17 Input resistance equivalent block diagram

Each device can be distinguished by input resistance of HINU, HINV and HINW.

When measuring input resistance, apply current from HINX pins. Warning: applying current form GND leads to improper resistance value.



a) When applying current form HINX pins
→ Input resistance shows proper value



b) When applying current from GND
→ Current flows Di and pull down resistor (5kΩ), too.
Then input resistance shows improper value.

Figure 2.2.18 Notes on measurement

2.3. Package

There are two type of packages

2.3.1. Outline drawing

Package Name	HSDIP25

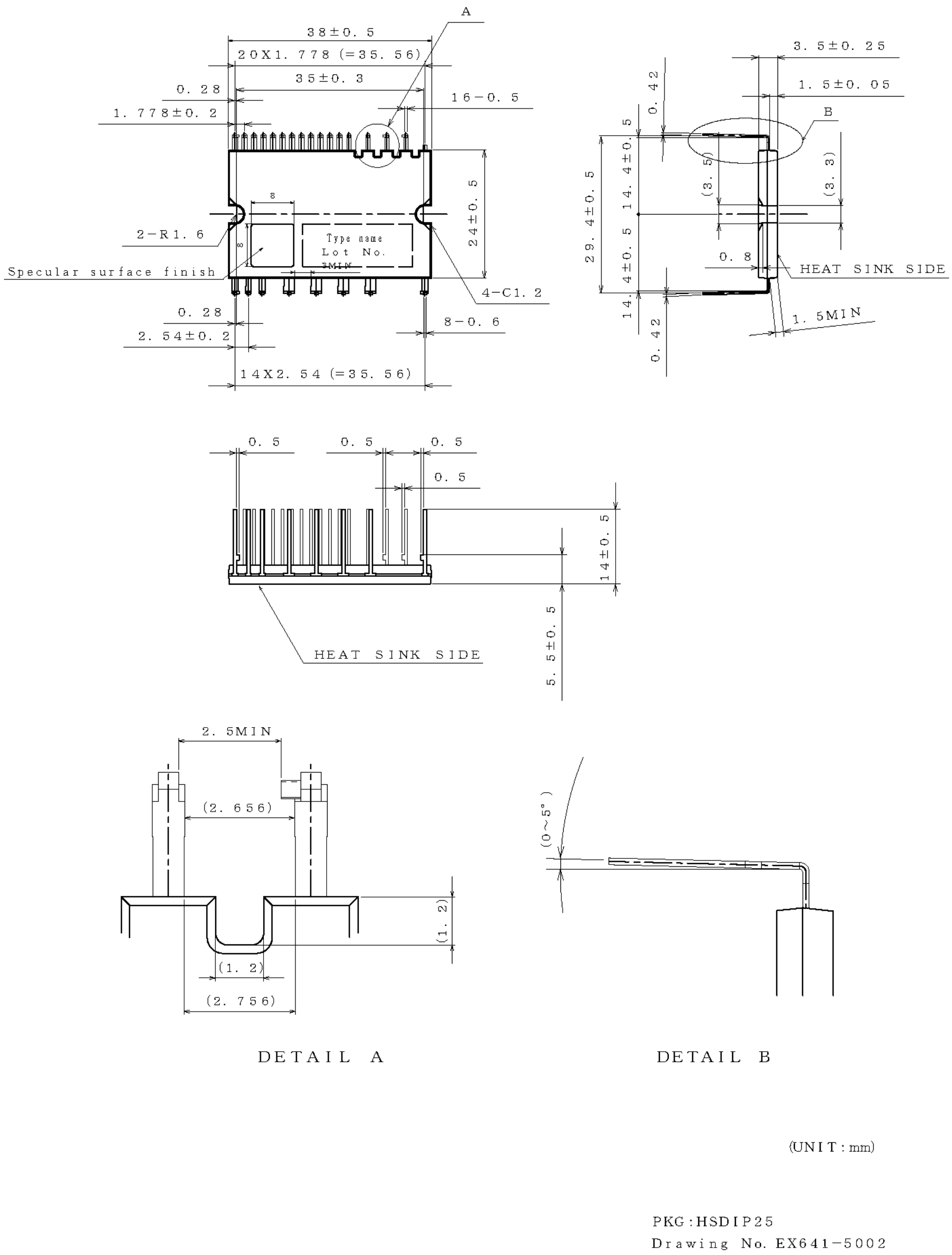


Figure 2.3.1 VA Long Pin Type

2.3.2. Pin Description

Pin No.	Pin Name	Function
1	NC	Not connected (GND potential)
2	VBU	U phase floating control supply
3	VBV	V phase floating control supply
4	VBW	W phase floating control supply
5	HINU	U phase high side IGBT control
6	HINV	V phase high side IGBT control
7	HINW	W phase high side IGBT control
8	HVCC	Control supply for HVIC
9	GND	Ground *(Note 1)*
10	LINU	U phase low side IGBT control
11	LINV	V phase low side IGBT control
12	LINW	W phase low side IGBT control
13	LVCC	Control supply for LVIC
14	FO	Alarm output
15	CIN	Short circuit detection
16	GND	Ground *(Note 1)*
17	VOT	Temperature Output
18	NW	W phase low side IGBT emitter
19	NV	V phase low side IGBT emitter
20	NU	U phase low side IGBT emitter
21	W	W phase output
22	V	V phase output
23	U	U phase output
24	P	Inverter supply
25	NC	Not connected *(Note 2)*

(Note 1) Two GND pins (9 & 16pin) are connected inside IPM, please connect one pin (16pin is recommended) to the 15V power supply GND outside and leave the other open.
(Note 2) NC pin is not electrically connected to any other potential inside.

Table 2.3.1 Pin Description

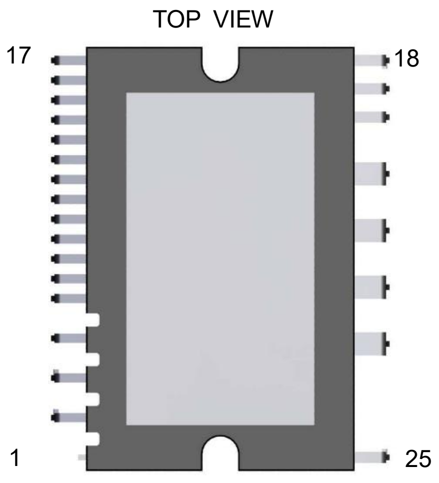


Figure 2.3.2 Pin Configuration

2.3.3. Marking

Figure 2.3.3 shows Marking Diagram There is a bottom side.

BOTTOM NIEW

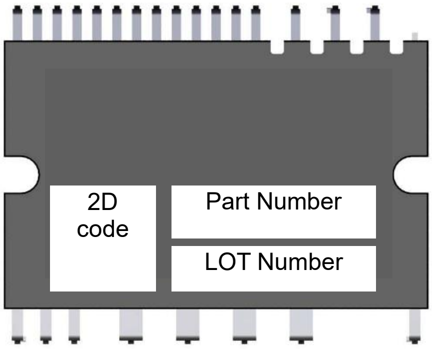
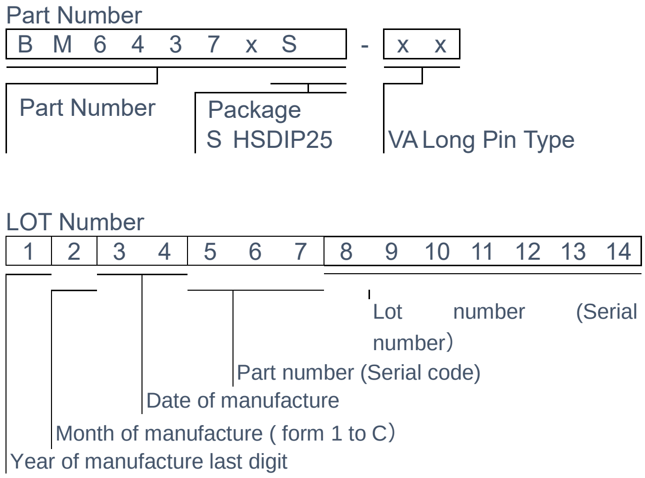


Figure 2.3.3 Marking Diagram



2.3.4. Insulation distance

Table 2.3.2 shows insulation distance.

Item	Clearance[mm]	Creepage[mm]
Between live pins with high potential	2.50	3.00
Between pins and heat sink	1.45	1.50

Table 2.3.2 Distance of insulation

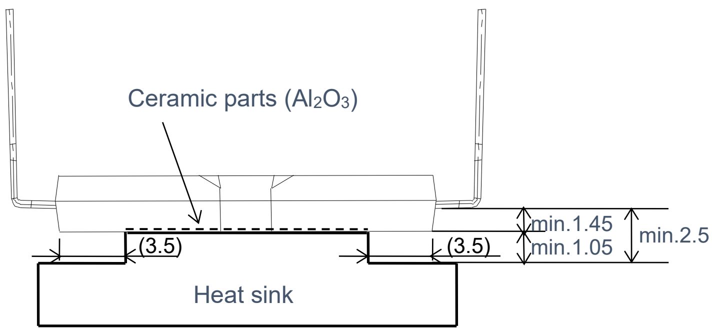


Figure 2.3.4 In the case of using the convex heat sink (unit: mm)

2.3.5. Heat sink mounting and precautions

When installing a module to a heat sink, excessive uneven fastening force might apply stress to inside chips or ceramic of heat sink plate, which will lead to breakage, crack or degraded device. Figure 2.3.6 shows recommended fastening sequence. Use a torque driver to fasten to the specified torque. The temporary fastening torque is set from 20 to 30% of the maximum torque rating. Evenly apply thermally conductive grease with 100μm to 200μm thickness over the contact surface between the module and the heat sink. Please use a type of grease that does not change in quality and age within operating temperature range. Deeply clean the contact surface of module and the heat sink before mounting.

It is recommended to install the module directly to the heat sink after applying grease. When inserting a heat radiation sheet between a module and a heat sink, it might apply stress depending on thickness and elastic modulus of the sheet to inside chips or ceramic of heat sink plate, which will break, crack or degrade the module. A heat radiation sheet is needed to prevent IPM from bending into + side of Figure 2.3.5.

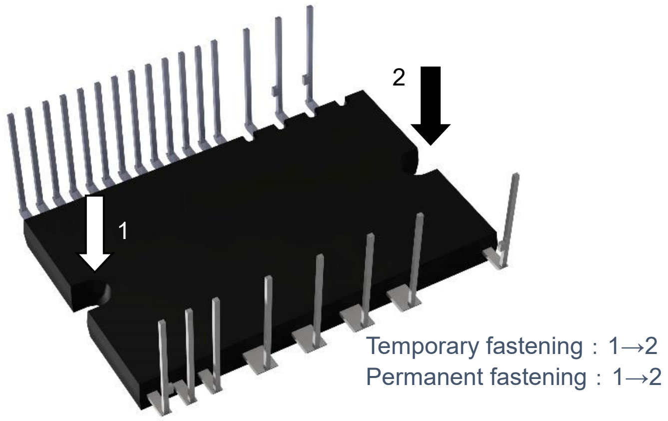


Figure 2.3.6 example of recommended Fastening Sequence

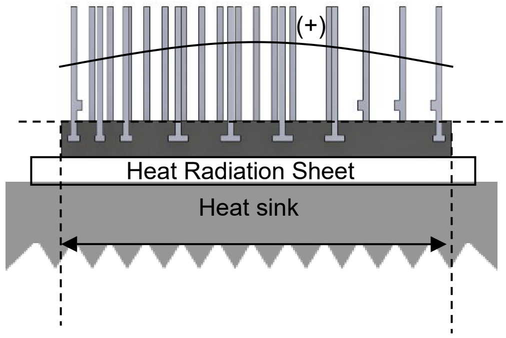


Figure 2.3.5 Flatness after Installing to a Heat sink (When Using a Heat Radiation Sheet)

Item	Limit			Unit	Conditions
	Min	Typ	Max		
Mounting Torque	0.59	0.69	0.78	N･m	Mounting Screw M3 *(Note 1)* Recommended 0.69N･m
Flatness of Outer Heat Sink	-50	-	+100	μm	Refer to Figure 2.3.7

(Note 1) Plain washers (ISO 7089 to 7094) are recommended.

Table 2.3.3 Mounting Torque and Heat Sink Flatness Specification

In order to get effective heat dissipation, it is necessary to enlarge the contact area as much as possible to minimize the contact thermal resistance.
Figure 2.3.7 shows measurement Part for Heat Sink.

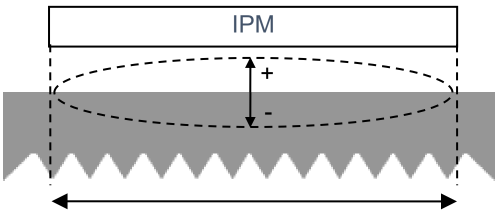


Figure 2.3.7 Measurement Point of Heat Sink Flatness

3. Application

3.1. Application example

3.1.1. Non-isolated control by driving IPM directly

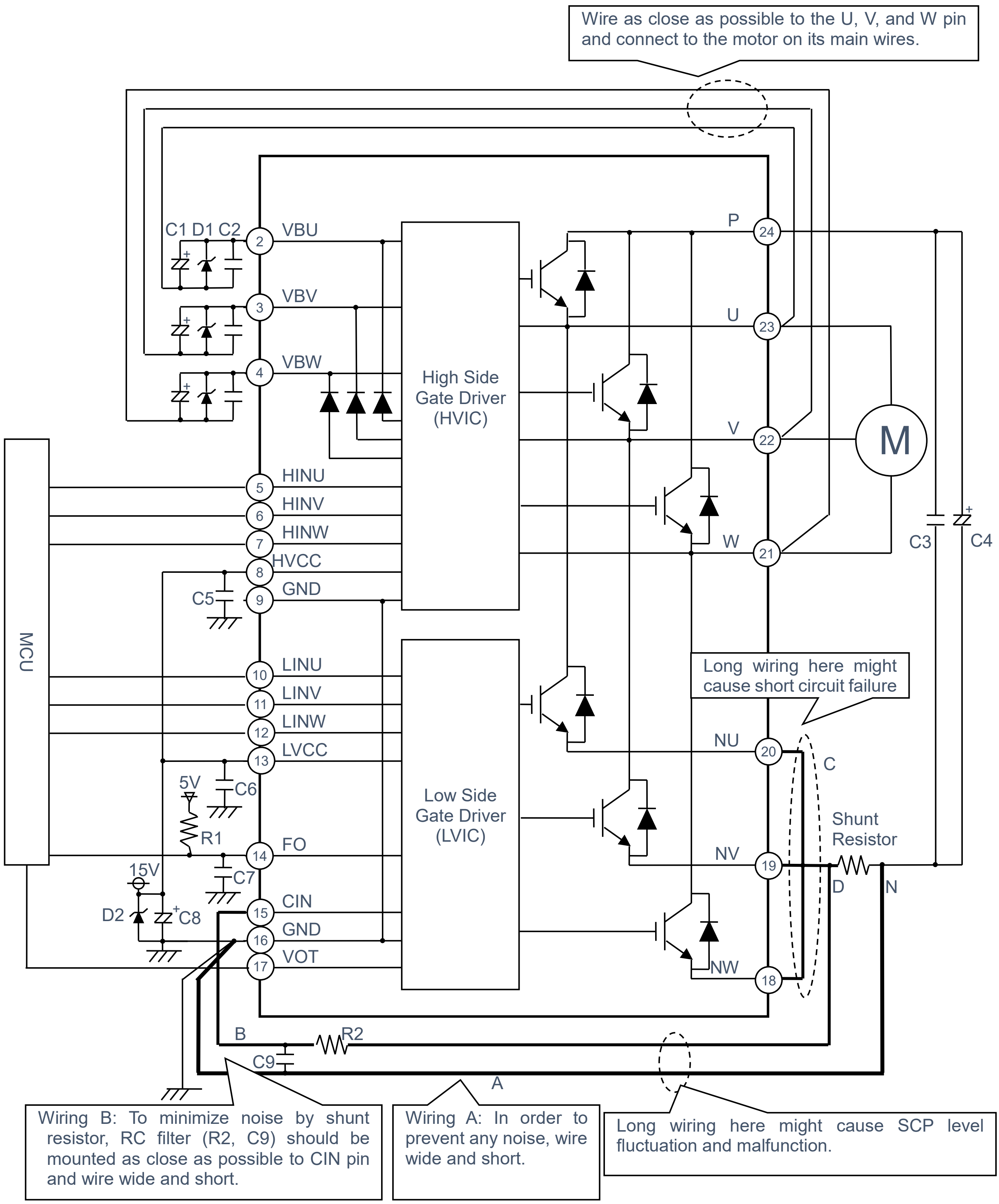


Figure 3.1.1 Application Example (Non-isolated control by driving IPM directly)

3.1.2. Isolated control by driving IPM through photo coupler

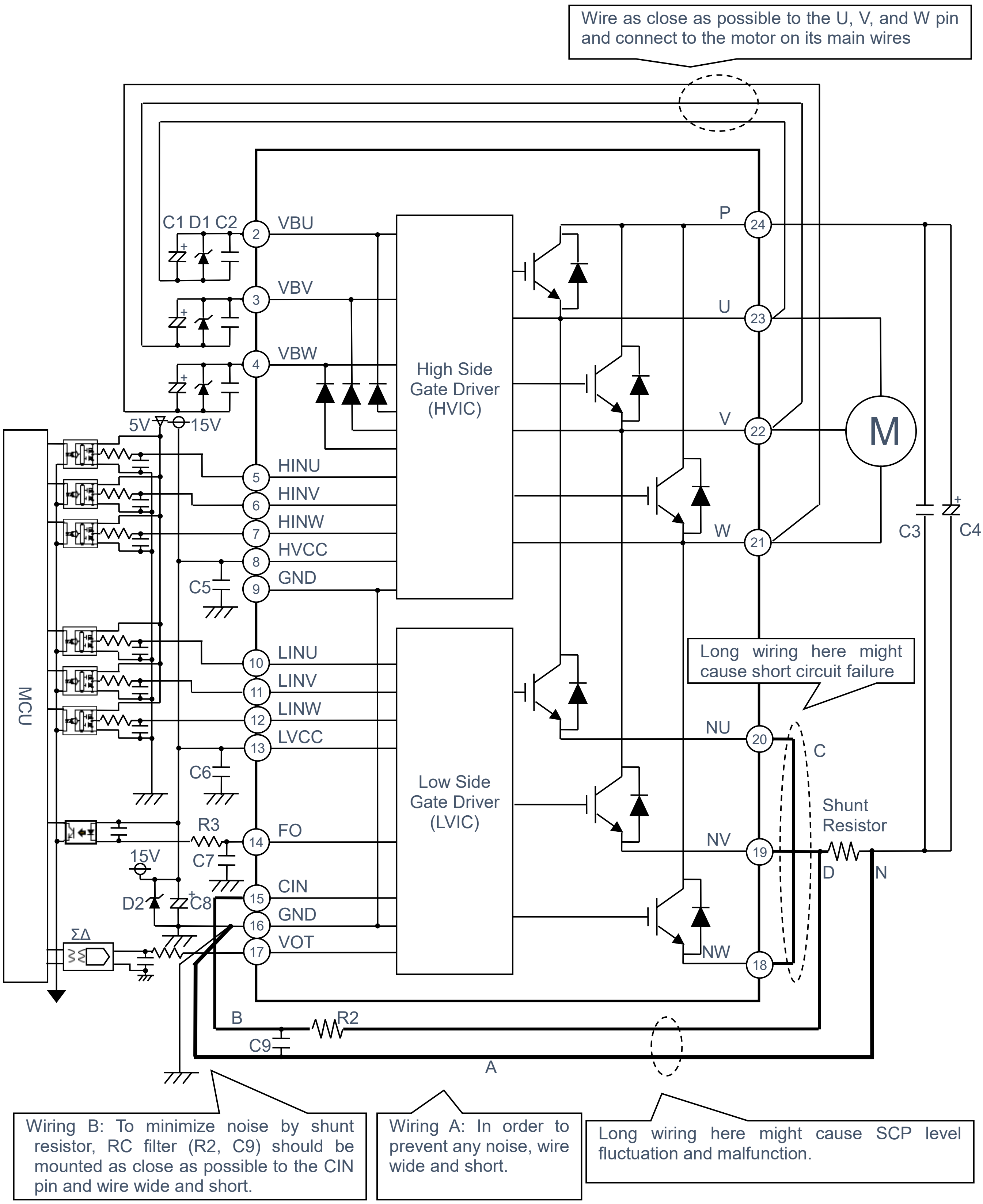


Figure 3.1.2 Isolated control by driving IPM through photo coupler

3.2. Selection of Components (Refer to Figure 3.1.1)

1) The VBU, VBV, VBW pin

·The bypass capacitor(good temperature, frequency characteristic electrolytic type C1: 22μF to 100μF) should be mounted as close as possible to the pin in order to prevent malfunction or destruction due to switching noise and power supply ripple. In addition, to reduce the power supply's impedance in wide frequency bandwidth, ceramic capacitor (good temperature, frequency and DC bias characteristic ceramic type C2: 0.1μF to 0.22μF) should also be mounted.

·Zener diode D1 (1W / 20 to 22V) should be mounted between each pair of control supply pins to prevent surge destruction. (Recommended PDZV20B)

·Line ripple voltage should meet dV/dt ≤1V/μs, Vripple ≤2$V_{p\text{-}p}$.

·The wiring from U, V, and W pin should be as thick and as short as possible. They should be connected directly and separated from the main output wires.

2) The HVCC, LVCC pin

·The bypass capacitor (good temperature, frequency characteristic electrolytic type C9) should be mounted as close as possible to the pin in order to prevent malfunction or destruction due to switching noise and power supply ripple. In addition, to reduce the power supply's impedance in wide frequency bandwidth, ceramic capacitor (good temperature, frequency and DC bias characteristic ceramic type C5 and C6: 0.1μF to 0.22μF) should also be mounted.

·Zener diode D2 (20 to 22V) should be mounted between each pair of control supply pins to prevent surge destruction. (Recommended PDZV20B)

·Line ripple voltage should meet dV/dt ≤1V/μs, V_{ripple} ≤2$V_{p\text{-}p}$.

3) The P pin

·To prevent surge destruction, the wiring between the smoothing capacitor C4 and the P pin, N point should be as short as possible.

·Snubber capacitor (C3: 0.1μF to 0.22μF) should be mounted between the P pin and the N point.

4) Control input pins (HINU、HINV、HINW、LINU、LINV、LINW)

·The wiring should be as short as possible to prevent malfunction.

·Input drive is active-high type. There is a 3.3kΩ (Min) pull-down resistor in the input circuit of IC. When using RC coupling circuit, make sure the input signal level meets the input threshold voltage.

·Dead time of input signal should be more than specified value.

·The pull-down resistors of Control input are enabled during supplying recommended voltage at the LVCC pin and the HVCC pin. Otherwise, the LINU, LINV and LINW show high impedance, the HINU, HINV and HINW show specific resistance correspond to (2.2.6 Control inputs (HINU, HINV, HINW, LINU, LINV and LINW))

5) The FO pin

·The FO output is open drain. It should be pulled up to control power supply(e.g. 5V, 15V) by a resistor that makes I_{FO} up to 1mA.I_{FO} is estimated roughly by the formula of control power supply voltage divided by pull-up resistance(R1).
In the case of pulled up to 5V, R1 = 10kΩ is recommended.

·In case of input to MCU by photo coupler or something, FO output duration timing can expand adding a capacitor (C7) in order to align the propagation delay of photo coupler.

6) The CIN pin

·RC filter (R2, C5) should be mounted as close as possible to the pin in order to prevent malfunction by recovery current or switching noise. It is recommended to select low tolerance, temp-compensated type for RC filter (R2, C9).
The time constant R2xC9 (1.0μs is recommended) should be set in order to shut down SCP current within 2μs.
The time constant is subjected to the wiring pattern on the board, etc. and should be evaluated in the actual application. .

·The point D at which the wiring to the CIN filter is divided should be near the pin of shunt resistor. The NU, NV, NW pins should be connected near to NU, NV, NW pins.

·To prevent malfunction, the wiring of B should be as short as possible.

7) The VOT pin (refer to 2.2.4)

·It is recommended to place 5.1kΩ pull down resistor to get linear output characteristics at temperature lower than room temperature. When the pull down resistor is placed between the VOT pin and the GND pin (control GND), the extra current calculated by the VOT output voltage divided by pull down resistance flows in LVIC circuit current continuously.
In the case of only using the VOT to detect only temperature higher than room temperature, it is not necessary to insert the pull down resistor.

·In the case of using the VOT with low voltage controller (e.g. 3.3V MCU), the VOT output might exceed control supply voltage 3.3V when temperature rises excessively. If system uses low voltage controller, it is recommended to insert a clamp diode between control supply of the controller and the VOT for preventing over voltage.

·When the VOT pin is not used, please do not connect the VOT pin.

8) The GND pins

·Two GND pins (9 & 16 pin) are connected inside IPM. Please connect one pin (16 pin is recommended.) to the 15V power supply GND outside and leave the other open.

·Connect control GND to power GND by common broad pattern can cause malfunction due to power GND fluctuation. It is recommended to connect control GND and power GND to a single point N (near the pin of shunt resistor).

·To prevent malfunction, the wiring of A should be as short as possible.

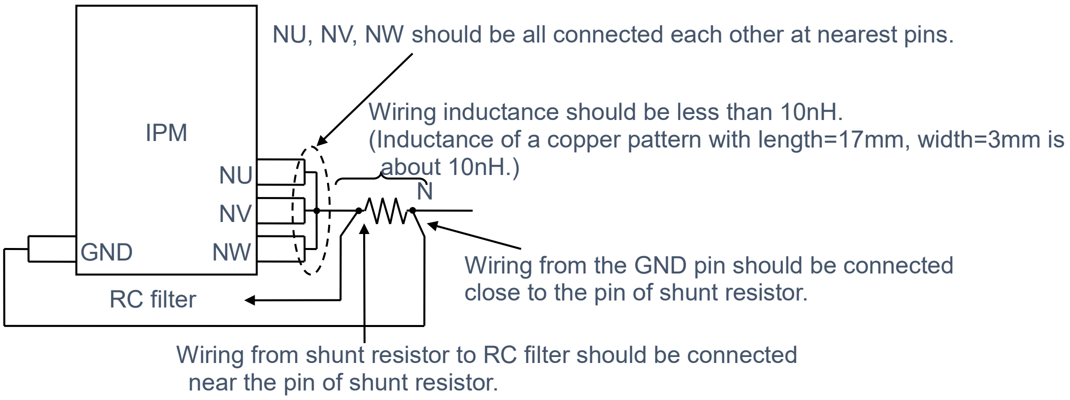
9) The NU、NV、NW pins

·In case of operation with a single shunt resistor, please short the three pins (NU, NV and NW). In addition, to prevent malfunction, the wiring of C should be as short as possible.

10) One-shunt resistor drive

·Recommended Shunt Resistors	: 1mΩ to 10mΩ	PMR series (Metal plate type)
	:10mΩ to 910mΩ	LTR series (Long terminal type)

https://www.rohm.com/products/resistors



Low inductance shunt resistor like surface mounted (SMD) type is recommended.

Figure 3.2.1 Wiring Pattern around the Shunt Resistor when Operating with One-shunt Resistor

11) Three-shunt Resistors Drive

·It is not recommended to use the voltage of each shunt resistor directly in the CIN pin when IPM is operated with three shunt resistor. In that case, it is necessary to use the external protection circuit as below.

·Set the time constant R_fC_f (1.0μs is recommended) of external comparator input in order to stop the IGBT within 2μs when short circuit occurs. The time constant is subjected to the wiring pattern on the board, etc. and should be evaluated in the actual application.

·It is recommended to set the threshold voltage VREF to the same rating of short circuit trip level (V_{SC} = 0.48V(Typ))

·To prevent malfunction, the wiring of A, B, C should be as short as possible.

·OR output high level should be set greater than maximum V_{SC} rating 0.505V and lower than the CIN absolute maximum rating 7V when the protection is active.

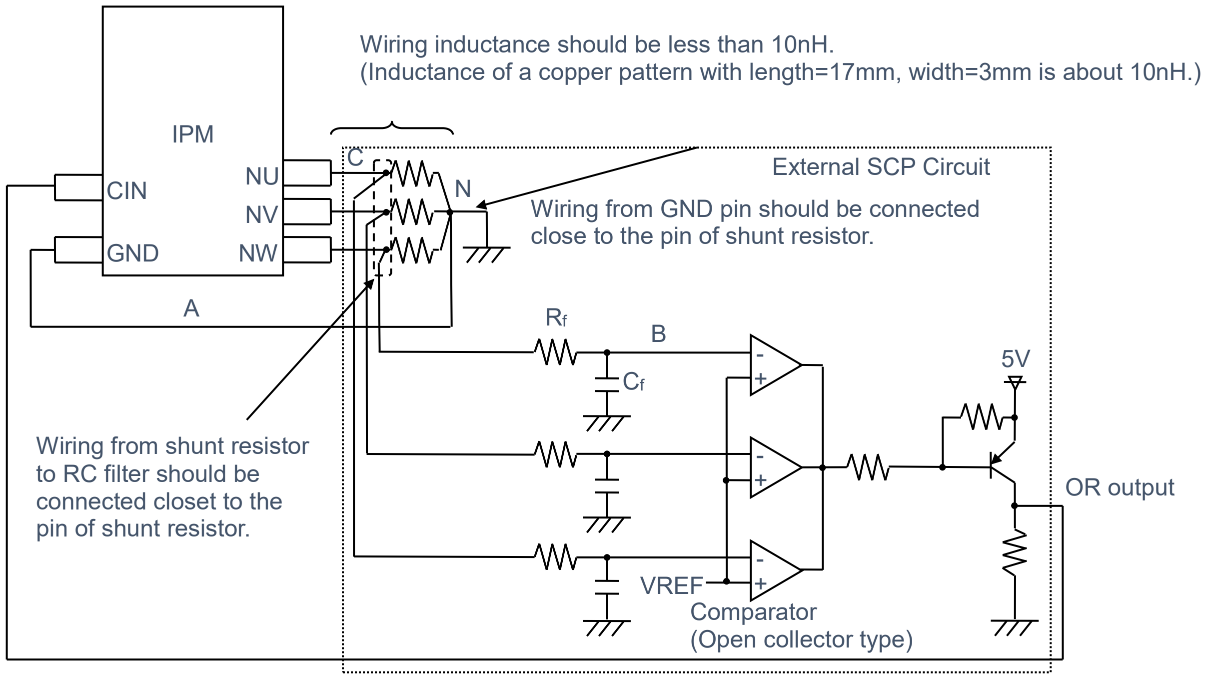


Figure 3.2.2 Wiring Pattern around the Shunt Resistor when Operating with Three-shunt Resistor

3.3. Application configuration example

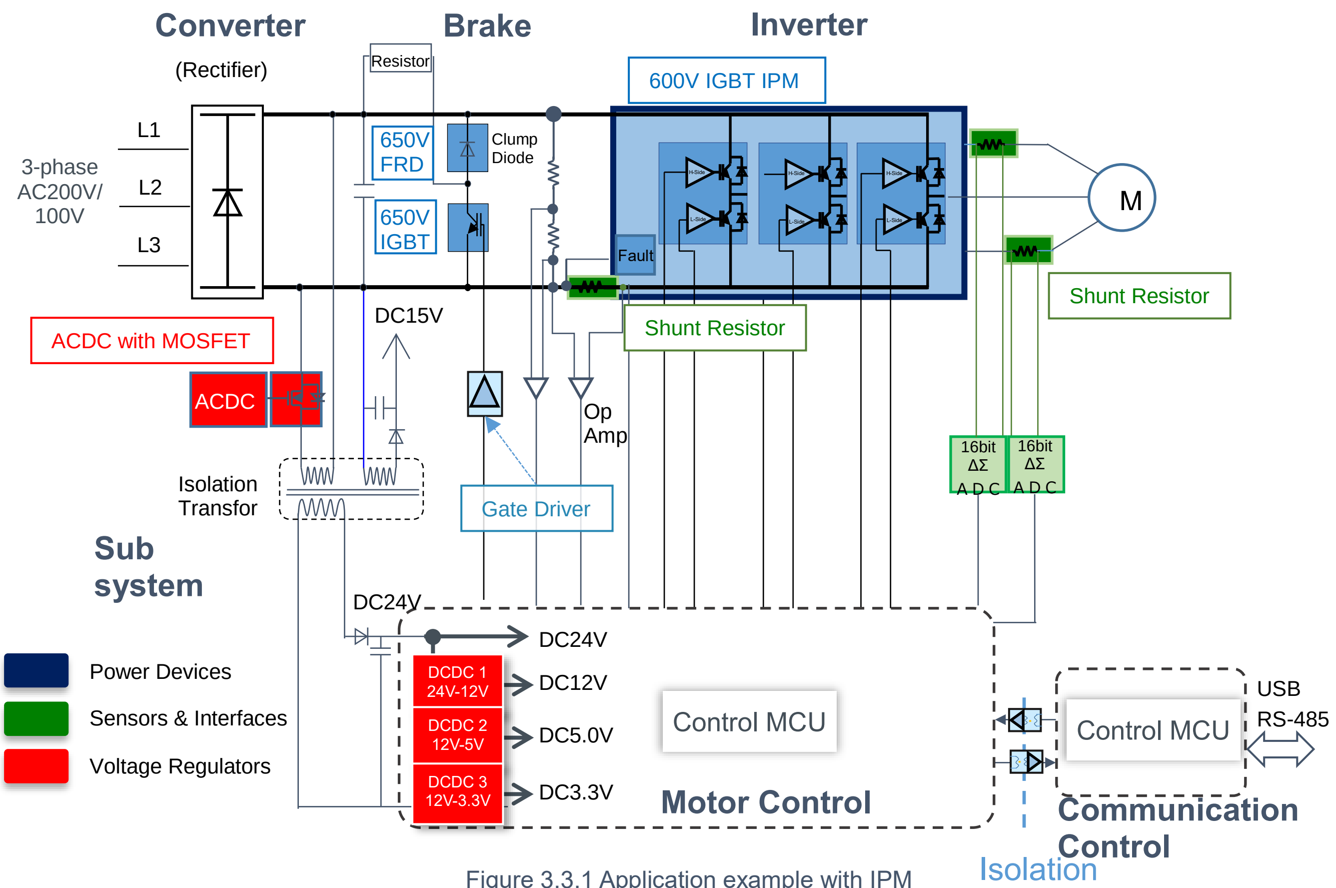


Figure 3.3.1 Application example with IPM

Power Devices

- IGBT IPM — https://www.rohm.com/products/ipm/igbt-ipm
  600V — BM6437xseries
- Fast Recovery Diode — https://www.rohm.com/products/diodes/fast-recovery-diodes
  650V Low V_F Low noise — RFL series
- IGBT discrete — https://www.rohm.com/products/igbt/field-stop-trench-igbt
  SCWT 8μs (min) — RGS series
  SCWT 5μs (min) — RGT series
- Gate Driver — https://www.rohm.com/products/power-management/gate-drivers
  Isolated Simple Gate Driver — BM61M41RFV-C
  Non-isolated Simple Gate Driver — BD2310G

Sensor & Interfaces

- Shunt Resistors — https://www.rohm.com/products/resistors
- 1mΩ to 10mΩ — PMR series (Metal plate type)
  10mΩ to 910mΩ — LTR series (Long terminal type)

Voltage Regulators

For Primary power supply https://www.rohm.com/products/power-management/ac-dc-converters-ics

- ACDC Built-in or external 650V/800V MOSFET
  650V/800V PWM up to 30W — BM2Pxxx (65kHz/100kHz 650V), BM2PxxxEK (65kHz/100kHz/130kHz 800V)
  650V/800V PWM over 30W — BM2P01xT (65kHz 650V)
  650V/800V PWM buck converter — BM2Pxxx (65kHz/100kHz 650V), BM2Pxxx (65kHz/100kHz 800V)
  External FET PWM/QR control IC — BM1PxxFJ (PWM 65kHz/100kHz 650V), BM1QxxFJ (QR 650V), BD762xFJ (QR for SiC MOSFET)

3.4. PCB Layout Guidance

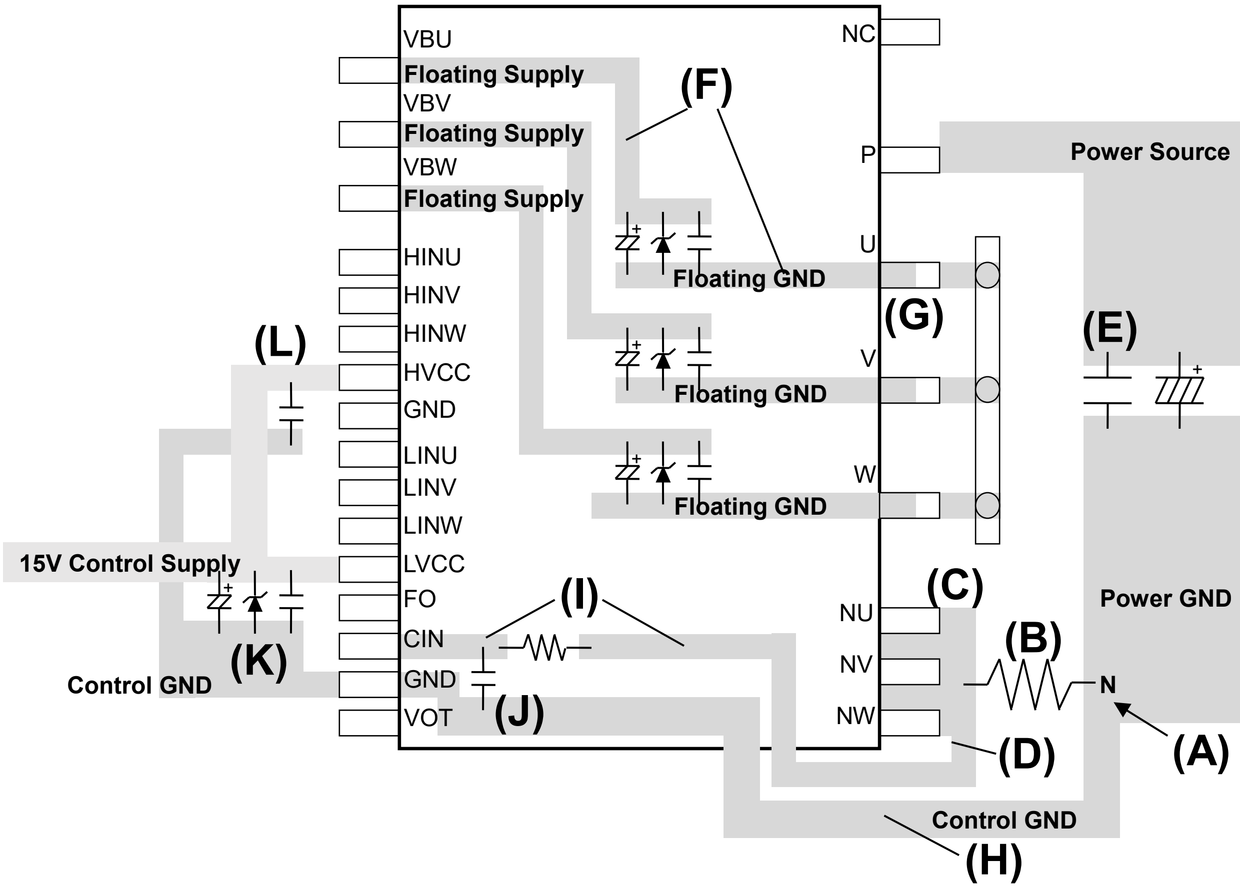


Figure 3.4.1 Precaution of PCB Design

(A) It is recommended to connect control GND and power GND only at one N point.

(B) It is recommended to use the surface mount type resistor with low inductance.

(C) Wiring between the NU, NV, NW pins and the shunt resistor should be as short as possible.

(D) Wiring to the CIN pin should be divided near the shunt resistor terminal and as short as possible.

(E) Place snubber capacitor between the P pin and point N and closely to terminals.

(F) Wiring should be as short as possible. Floating control supply wire potential fluctuates between the P pin and the GND at switching. Therefore, it may cause the malfunction if low potential wires (e.g. control input pin, control supply) are located near or cross these switching wires. Please pay attention particularly when using multi layered PCB.

(G) Bootstrap negative electrodes should be connected to the U, V, W pins directly and separated from the main output wire.

(H) Wiring should be as short and as thick as possible.

(I) Wiring should be as short as possible in order to prevent the malfunction due to noise.

(J) Connect CIN filter’s capacitor to control GND (not to power GND).

(K) Capacitor and Zener diode should be located closely to the LVCC and GND pins.

(L) Capacitor should be located closely to the HVCC pin.

3.5. Snubber Circuit

In order to protect IPM from extra surge, the wiring length between the smoothing capacitor and the P pin-N points (shunt resistor terminal) should be as short as possible. Also, from 0.1μF to 0.22μF snubber capacitor should be mounted in the DC-link and near to the P pin and N points.
There are two positions ((A) or (B)) to mount a snubber capacitor as shown in Figure 3.5.1 Recommended Snubber circuit location.

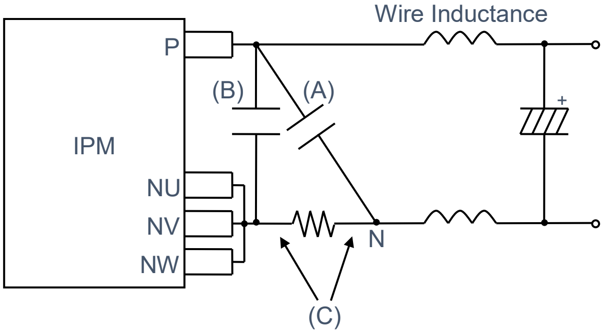


Figure 3.5.1 Recommended Snubber circuit location

The Snubber capacitor should be installed in the position (B) so as to suppress surge voltage effectively. However, the charging and discharging current generated by the wiring inductance and the snubber capacitor will flow through the shunt resistor, which might cause erroneous protection if this current is large enough. In order to suppress the surge voltage maximally, the wiring inductance at (C) (including shunt resistor parasitic inductance) should be as small as possible. A recommended wiring example is shown in location (A).

3.6. Inverter Power Supply and Collector-Emitter Voltage

The surge voltage of inverter power supply and collector-emitter voltage should be within the specified voltage. If the voltage is higher than the specified value, power line inductance should be reduced, and the snubber circuit should be used.

- V_{CES} : Maximum Rating of IGBT Collector-Emitter Voltage, 600V.
- V_P : Supply voltage applied between the P-N pins, 450V.
- $V_{P\,(surge)}$: Total amount of V_P and surge voltage generated by the wiring inductance between the P-N pins and the DC-link capacitor, 500V.
- $V_{P\,(PROT)}$: Self protection supply voltage limit (Short circuit protection capability), 400V.
  Condition VCC=13.5 to 16.5V, Inverter part Tj=125°C, non-repetitive, less than 2μs.

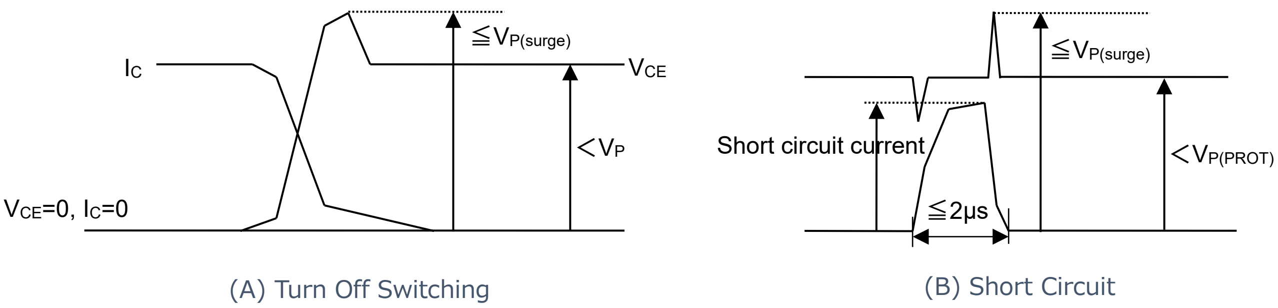


Figure 3.6.1 Waveform(I_C, V_{CE}, V_P) in Turn Off Switching and Short Circuit mode

3.7. Allowable Current Value

Figure 3.7.1 shows the typical motor rms current (I_o) versus carrier frequency (f_c) following inverter operating conditions based on IGBT-IPM. This curves are examples of admissible inverter output rms current under carrier frequency under maximum operating temperature condition (Tf = 100°C, Tj = 125°C).
This characteristic can change depending on control mode, motor types.

Conditions: V_P = 300V, V_{CC} = V_{BS} = 15V, P.F = 0.8, $V_{CE\ (sat)}$ = Typ., Switching loss = Typ., Tj = 125°C, T_f = 100°C
Rth (j-c) = max, 3-phase PWM modulation, fo = 60Hz sine waveform output.

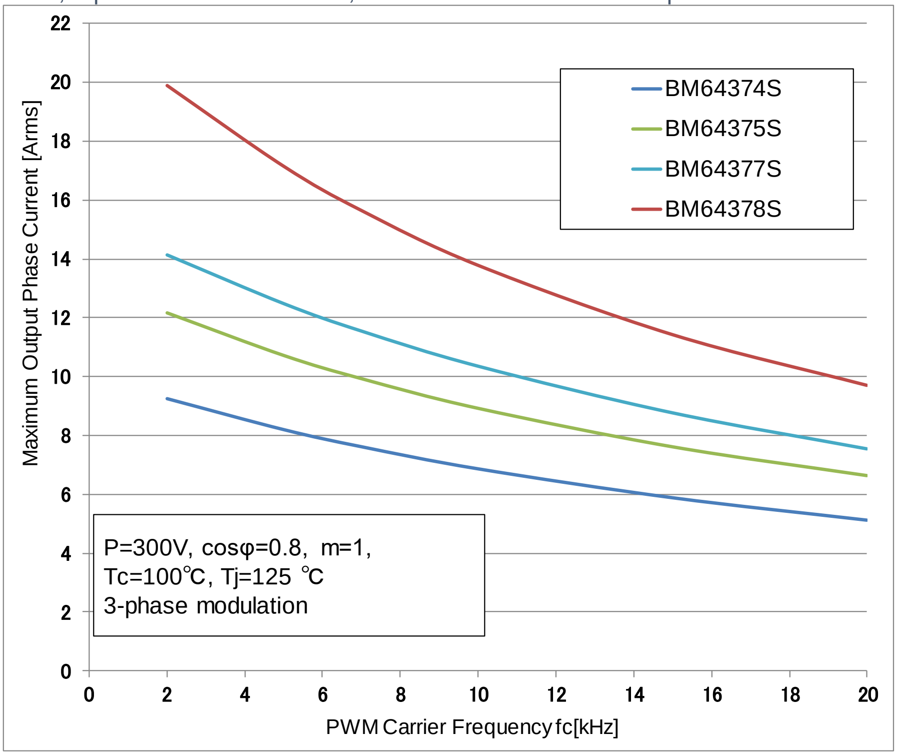


Figure 3.7.1 I_o-carrier frequency characteristics

Loss calculation software can be downloaded at ROHM web site.
URL: https://www.rohm.com/products/ipm

3.8. Short Circuit Safe Operating Area (SCSOA)

Figure 3.8.5 SCSOA main data show the circuits to obtain the SCSOA of Gen.3 IGBT IPM series devices and the SCSOA main data, respectively.

V_{IN} : IGBT gate driving signal on the LINW pin
V_{bus} : IGBT collector voltage: 400V
Tj : The IPM temperature 125°C

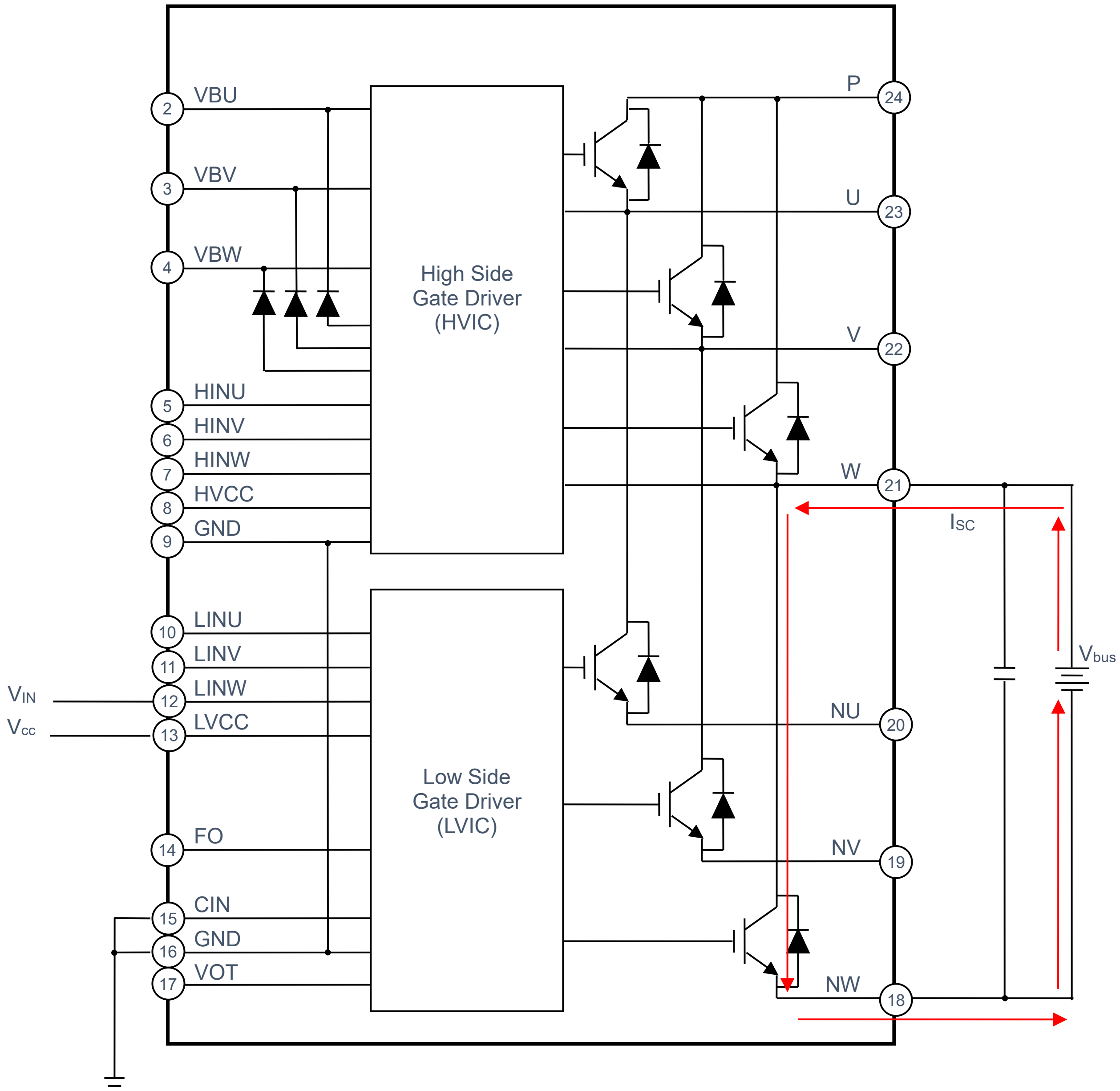


Figure 3.8.1 SCSOA test circuit

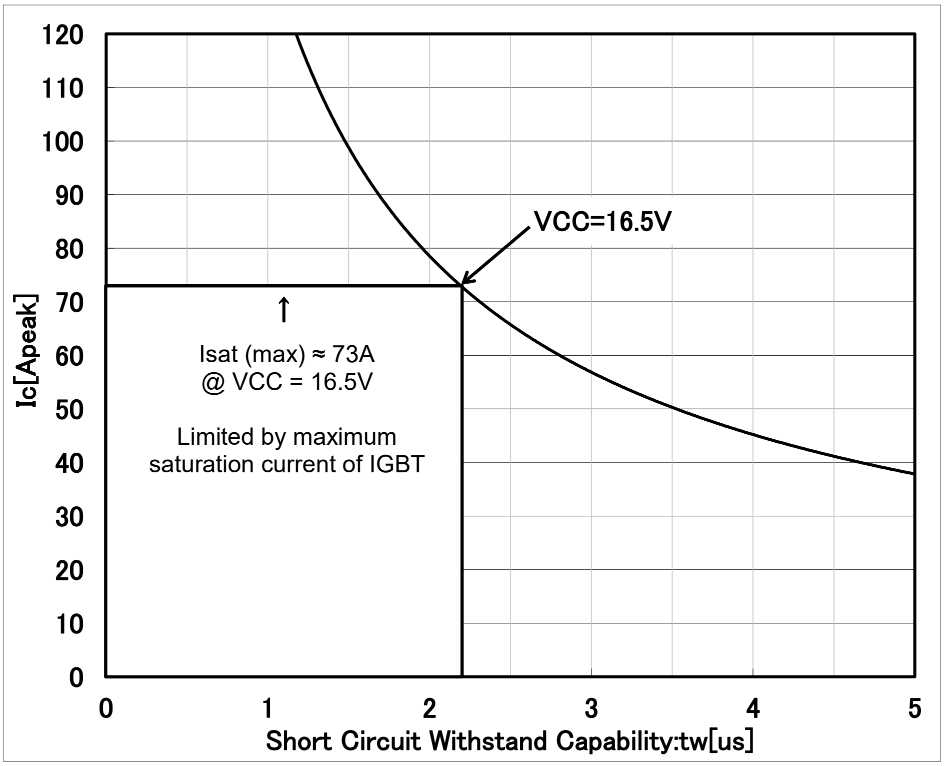


Figure 3.8.2 Typical BM64374S (15A) SCSOA curve

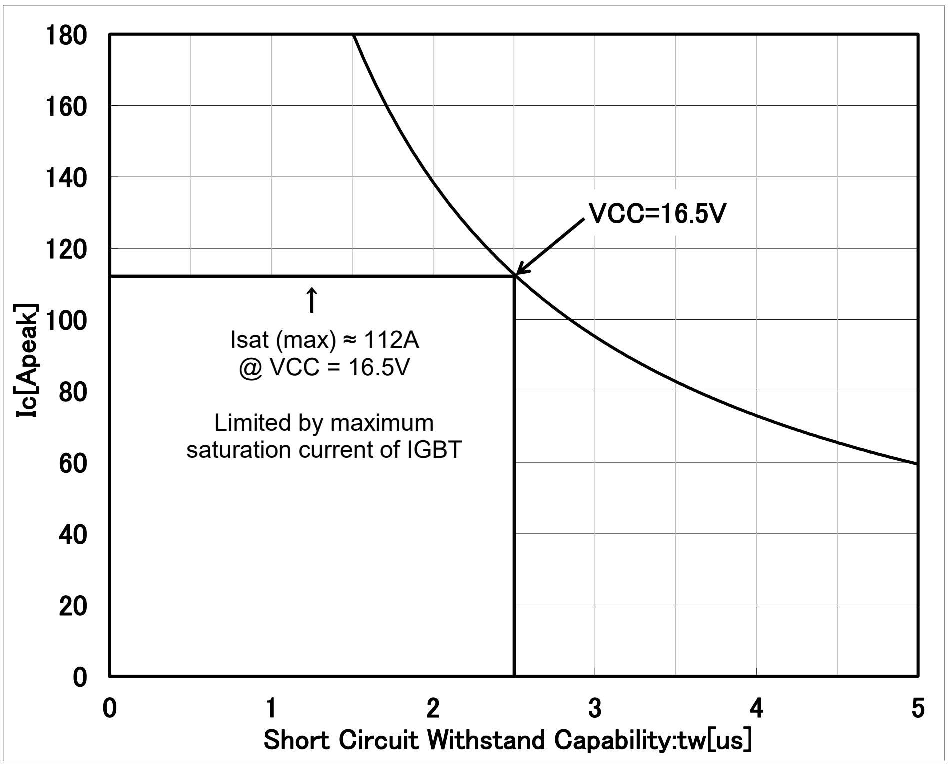


Figure 3.8.3 Typical BM64375S (20A) SCSOA curve

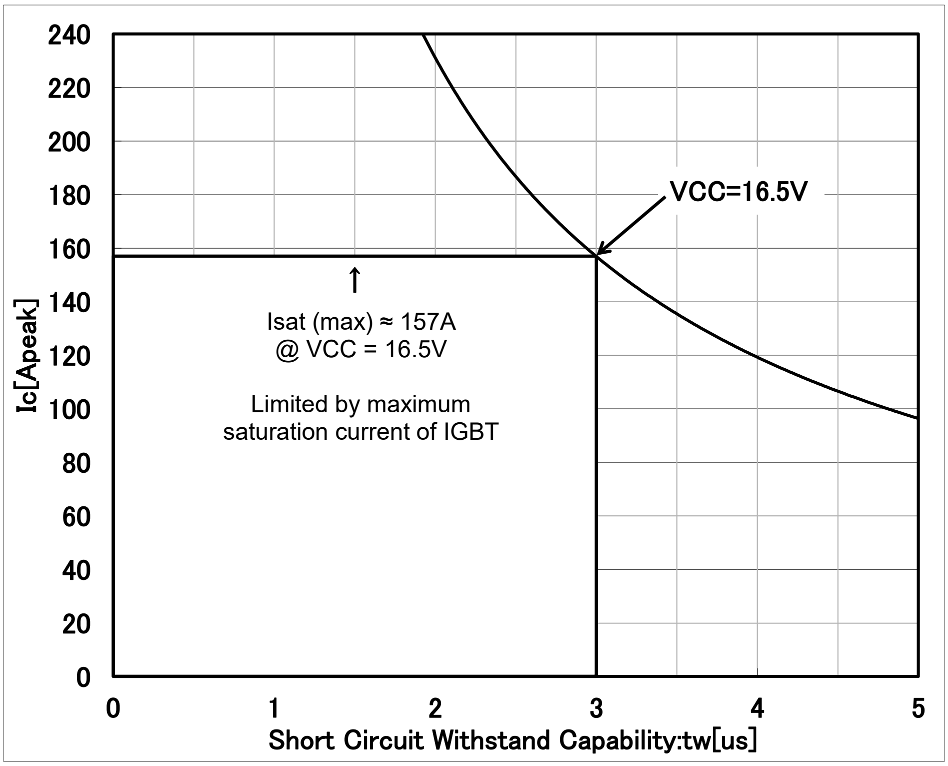


Figure 3.8.4 Typical BM64377S (30A) SCSOA curve

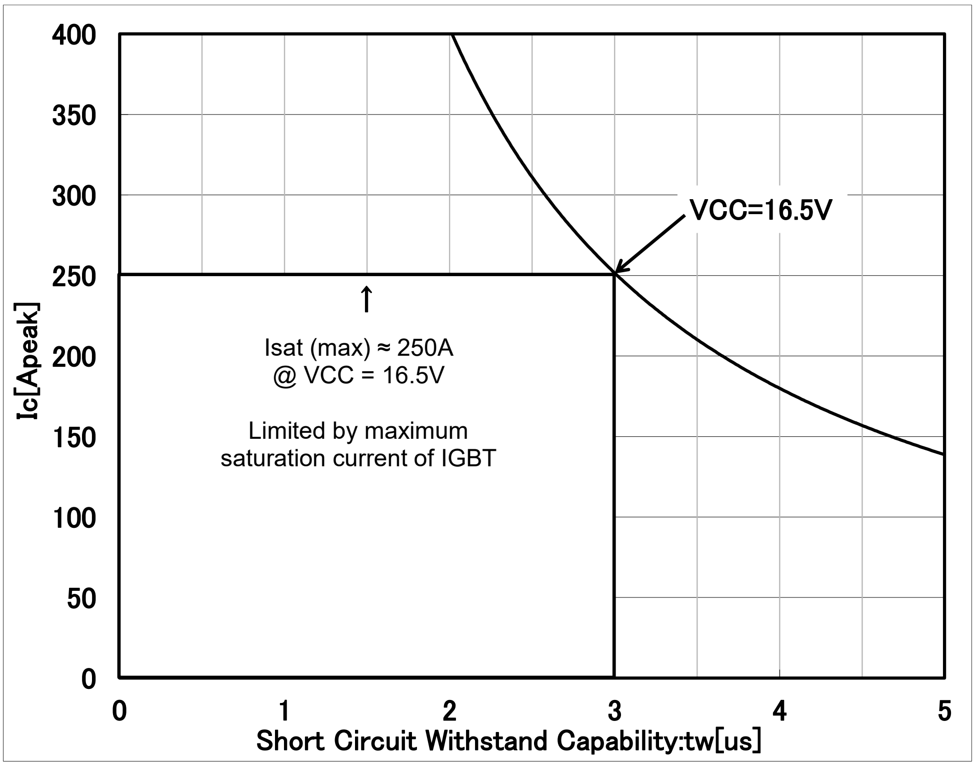


Figure 3.8.5 Typical BM64378S (35A) SCSOA curve

4. Bootstrap Circuit

4.1. Bootstrap Circuit Operation

For three-phase inverter circuit driving, normally four isolated control supplies (three for high side driving and one for low side driving) are necessary. The use of floating control supply with bootstrap circuit can reduce the number of isolated control supplies from 4 to 1 (Low side control 15V supply).

Bootstrap circuit consists in a bootstrap diode (BSD), a bootstrap capacitor (BSC) and a current limiting circuit. This product integrates BSD and current limiting circuit so the bootstrap circuit needs only the outer BSC (Figure 4.1.1).

BSC act as a control supply to drive high side IGBT. It supplies gate charge current and circuit current of HVIC.

Charge consumed by driving circuit is re-charged from Low side control 15V supply to BSC via current limiting circuit and BSD when voltage of output pin(U, V, W) goes down to GND potential in inverter operation. But there is the possibility that enough charge doesn't perform due to the condition such as switching sequence, capacitance of BSC and so on. The BSC voltage drop by deficient charge makes the loss of high side IGBT increasing and might work UVLO. This must be considered during bootstrap circuit design.

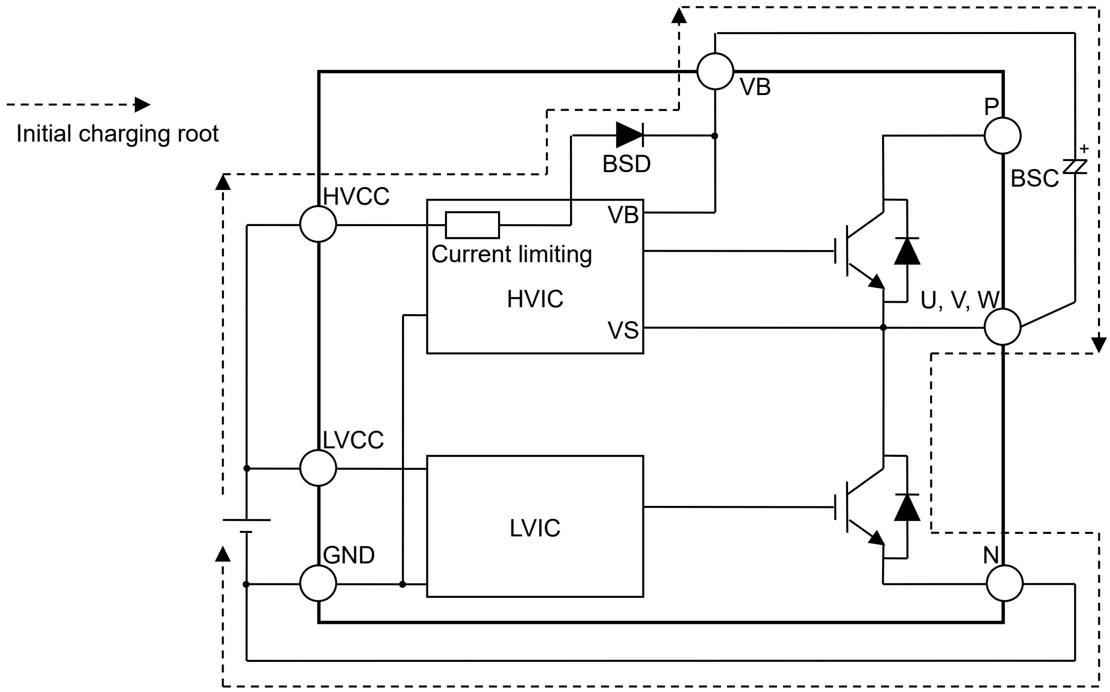


Figure 4.1.1 Bootstrap Circuit

4.2. Initial Charging

In bootstrap circuit, it is necessary to charge to the BSC initially. BSC charging is performed by turning on all low side IGBT normally. When outer load(e.g. motor) is connected to IPM, BSC charging may be performed by turning on only one phase low side IGBT since potential of all output pins will go down to GND level through motor windings. However, its charging efficiency might become lower due to some reason. (e.g. wiring resistance of motor).

There are mainly two procedures for BSC charging. One is performed by one long pulse (Figure 4.2.1), and another is conducted by multiple short pulse (Figure 4.2.2). Multi pulse method is used in case of some restriction like control supply capability. Necessary time of initial charging depends on the capacitance of BSC and current limiting circuit. After a detailed evaluation on the actual application, please secure enough charge time depending on BSC capacitance.

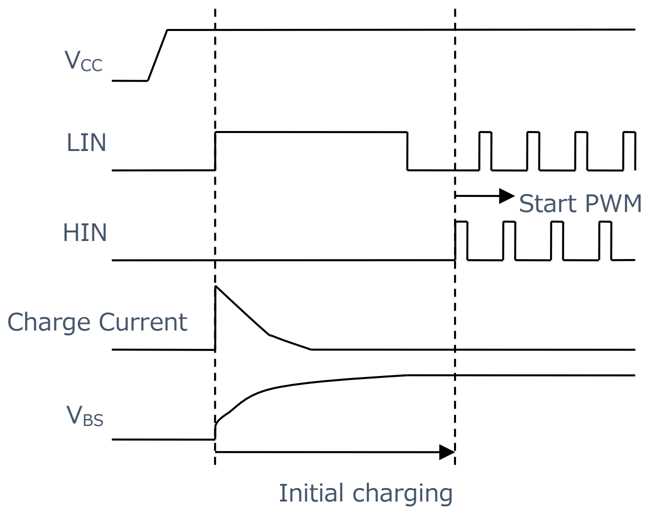


Figure 4.2.1 Waveform by one charging pulse

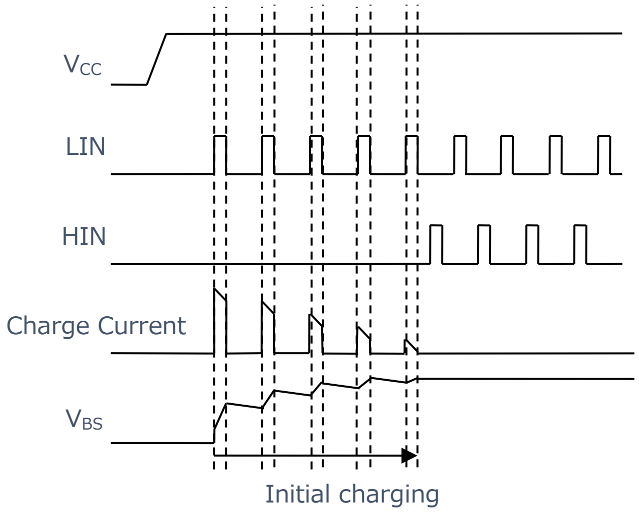


Figure 4.2.2 Waveform by multiple charging pulses

4.3. Bootstrap Diode and Current Limiting Circuit

V_F-I_F properties of built-in bootstrap diode and current limiting circuit (including voltage drop by the current limiting circuit) are shown in Table 4.3.1 and Figure 4.3.1.

The current limiting circuit raises charging efficiency by low resistance during PWM mode and reduces rush current to BSC in high-resistance at charging and reduces a load to 15V control supply.

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Forward voltage	V_{FB1}	0.3	0.6	0.9	V	I_{FB} = 1mA Voltage drop between HVCC-VBX (X = U,V,W)
	V_{FB2}	1.1	2.0	2.9	V	I_{FB} = 100mA Voltage drop between HVCC-VBX (X = U,V,W)

Table 4.3.1 Specification of Bootstrap Diode Part

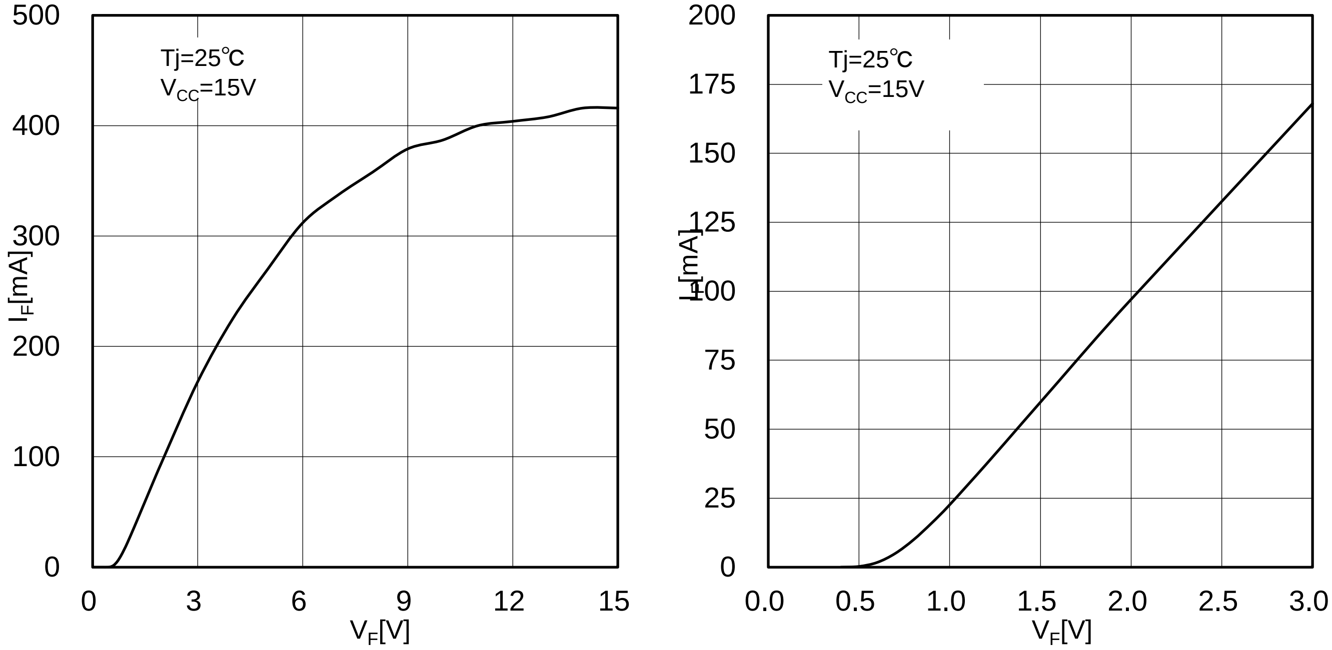


Figure 4.3.1 Characteristic of bootstrap diode V_F-I_F curve
(Between HVCC-VBX terminal (X=U, V, W))

4.4. Bootstrap Circuit Current

Bootstrap supply circuit current I_{BS} at steady state is maximum 0.15mA (Tj = 25°C、V_{CC} = V_{BS} = 15V, Table 4.4.1). In switching state, gate charge and discharge are repeated by high side IGBT switching, the circuit current increases proportional to carrier frequency. Figure 4.4.1 to Figure 4.4.4 show typical I_{BS}-carrier frequency fc at high temperature.

To calculate the BSC, please consider I_{BS} at switching mode. Since the high current rating consume larger circuit current, be careful during the development of the series product to use the same PCB layout.

Item	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
VBS circuit current 1	I_{BS1}	-	0.06	0.15	mA	V_{IN} = 0V
VBS circuit current 2	I_{BS2}	-	0.06	0.15	mA	V_{IN} = 5V

Table 4.4.1 Specification of Bootstrap Circuit Current

Condition : Tj = 125°C、V_{CC} = V_{BS} = 15V、IGBT ON duty = 10、30、50、70、90%

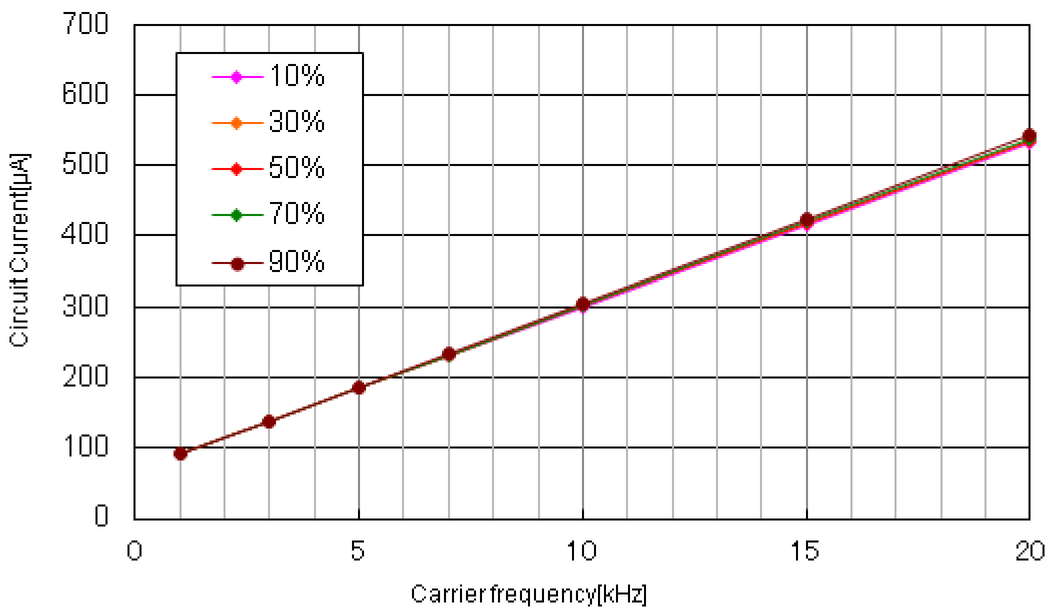


Figure 4.4.1 BM64374S (600V/15A) I_{BS}- Carrier Frequency fc

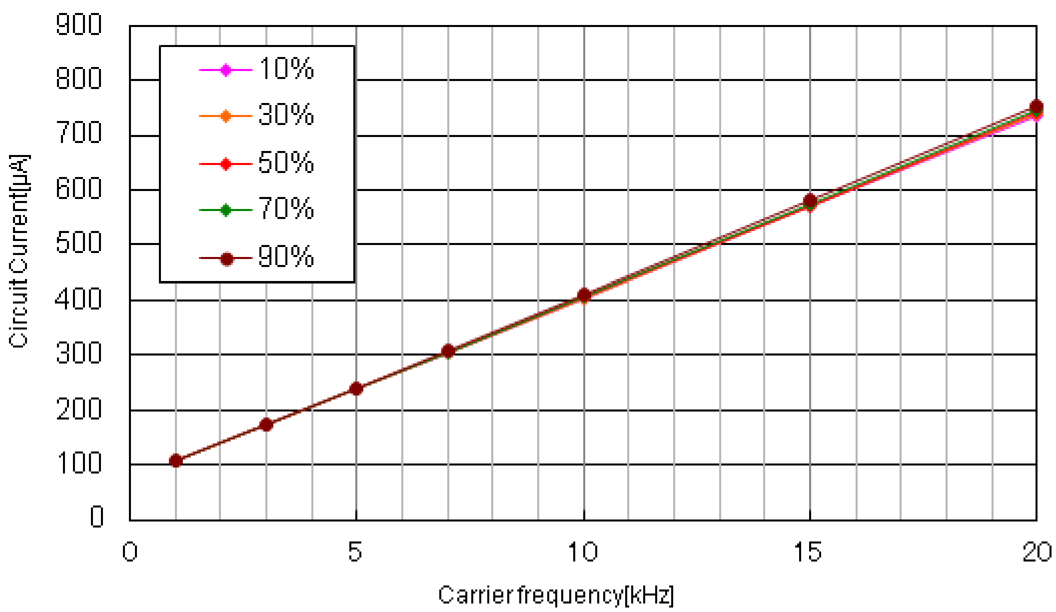


Figure 4.4.2 BM64375S (600V/20A) I_{BS}- Carrier Frequency fc

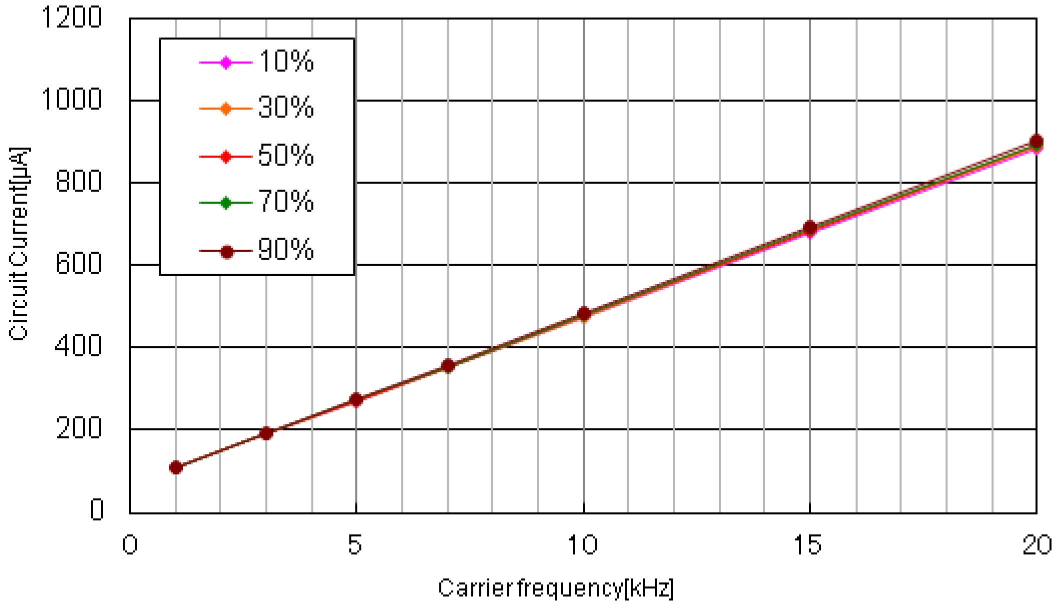


Figure 4.4.3 BM64377S (600V/30A) I_{BS}- Carrier Frequency fc

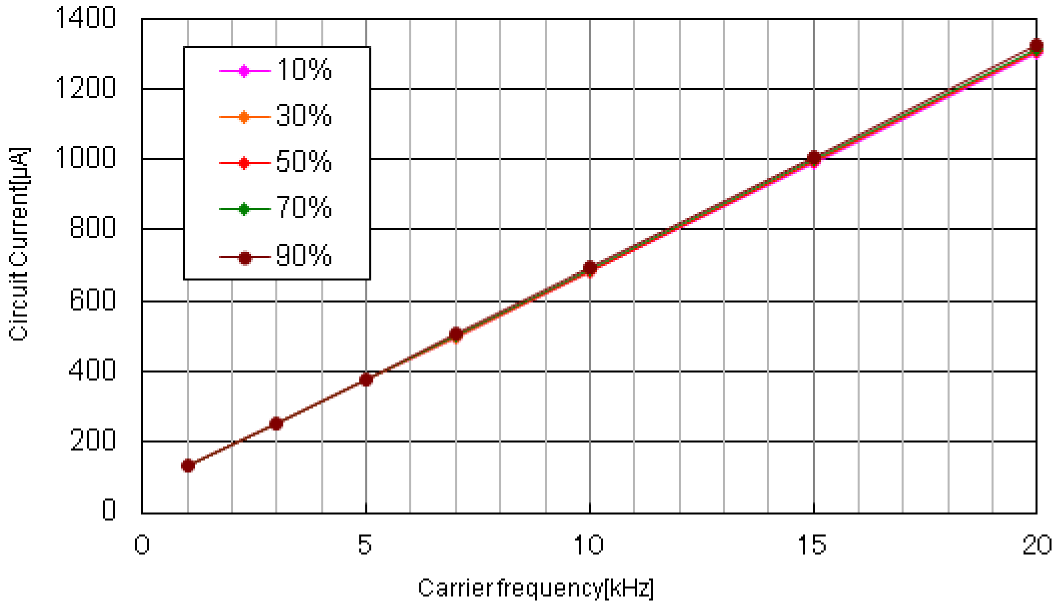


Figure 4.4.4 BM64378S (600V/35A) I_{BS}- Carrier Frequency fc

5. Revision History

Date	Revision	Changes
2020.12.24	001	First release

Notes

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