Design Models

How to Use LTspice[®] Models: Tips for Improving Convergence

An analysis error or unstable result from the LTspice simulation suggests a problem with the convergence. The convergence problem can be avoided by changing the simulator settings. This application note introduces methods for improving the convergence mainly in circuits containing the subcircuit models by changing the LTspice settings. The countermeasures introduced below are not effective to all circuits. Use this application note as reference for avoiding the simulation errors.

How to change the simulator option settings

In case a simulation does not converge, LTspice provides options to change the settings. As shown in Figure 1, you can open the "Control Panel" and then change the settings defined in the "SPICE" tab. In addition, the ".OPTION" command allows you to change the parameters not displayed in the panel, including "itl1" and "itl2".

💯 Control Panel			×
Hacks! Integration Q Sym. & Lib. Search Particular Compression Save Defaults	ths	H Netlist (Wavefo Options	
Default Integration Method[*] O trapezoidal O modified trap O Gear	Gmin: Abstol:	1e-012 1e-012 0.001]
Default DC solve strategy	Reltol: Chgtol: Trtol[*]:	1e-014]
Engine Solver[*]: Normal ~	Volttol: Sstol: MinDeltaGmin:	1e-006 0.001 0.0001]]
Max threads: 6 ~ Matrix Compiler: object code ~ Thread Priority[*]: medium ~	Accept 3K4	as 3.4K[*] 🗹 Bypass[*] 🗹	
[*] Setting remembered betwe Reset to Defau		ions.	
[OK ‡	Fヤンセル	ヘルプ

Figure 1. Option settings defined in the SPICE tab of the "Control Panel"

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Option settings for the device models

Simulations of only the device models used with bipolar transistors, diodes, and LEDs converge using the default settings shown in Figure 1 in most cases, depending on the circuit scale and configuration. Table 1 shows the option parameters defined in the right column of the "Control Panel". If a simulation does not converge with the device model, the convergence can be improved by increasing the default values of the parameters to the upper limits provided in Table 1, thereby relaxing the tolerance of convergence.

Parameter	Default value	Upper limit (Reference)	Summary
Gmin	1e-012 [S]	1e-009	Electrical conductivity added to all PN junctions for facilitating the convergence
Abstol	1e-012 [A]	1e-006	Absolute tolerance of current error
Reltol	0.001	0.01	Tolerance of relative error
Chgtol	1e-014 [C]		Absolute tolerance of charge
Trtol	1	7	Tolerance of temporary error coefficient in transient analysis
Volttol	1e-006 [V]	1e-003	Absolute tolerance of voltage error
Sstol	0.001		Relative error for detecting steady state
MinDeltaGmin	0.0001		Setting a limit for the end of the adaptive Gmin stepping

Table 1. Option parameters defined in the right column of the "Control Panel"

Option settings of the subcircuit models

For MOSFET with a macro model used in the subcircuit model, SiC power devices with a behavior model, and IGBT, performing simulations with the default settings causes problems including errors and incorrect display of the plot waveform as described below.

- "Analysis: Time step too small ..." error occurs and stops the simulation.
- The plot waveform is not displayed, or stops being displayed during the simulation.
- The waveform fluctuates to an excessive value during the simulation.

These errors occur if variation in the waveform is abrupt. The simulation is stopped if the time step required for calculating the abrupt variation is too small. In addition, the waveform cannot be displayed if the variation is too abrupt to perform the calculation correctly.

The abrupt variation in the waveform cannot be avoided in the SMPS (Switched Mode Power Supply) circuits. Therefore, use the following methods to avoid errors. Contrary to the countermeasures for the device models, the convergence can be improved by decreasing errors in the simulation values, thereby increasing the calculation precision.

Method 1: Solver setting

In "Control Panel", set "SPICE > Engine > Solver" to "Alternate" (Figure 2). According to the LTspice XVII manual, changing the setting from "Normal" to "Alternate" increases the internal precision 1,000 times.



Figure 2. Set "Solver" defined in the SPICE tab of the "Control Panel" to "Alternate"

Method 2: Maximum Timestep setting

In the simulation setting, set "Maximum Timestep" of the transient analysis to 10 nsec or 1 nsec. This setting improves the convergence by decreasing the amount of variation within one step of the calculation.

😕 Edit Simulation Command	\times
Transient AC Analysis DC sweep Noise DC Transfer DC op pnt	
Perform a non-linear, time-domain simulation.	
Stop time: 20m	
Time to start saving data:	
Maximum Timestep: 10n	
Start external DC supply voltages at 0V:	1
Stop simulating if steady state is detected:	
Don't reset T=0 when steady state is detected:	
Step the load current source:	
Skip initial operating point solution: 🔲	
Syntax .tran <tprint> <tstop> [<tstart> [<tmaxstep>]] [<option> [<option>]]</option></option></tmaxstep></tstart></tstop></tprint>	
.tran 0 20m 0 10n	
Cancel OK	

Figure 3. Set "Maximum Timestep" of the transient analysis

Method 3: Option parameters setting

Change the option parameters defined in the right column of the "Control Panel" (Figure 1). The recommended values are shown in Table 2. Change the values of "Reltol" and/or "Trtol" to the recommended values. Determine a suitable combination by repeating the simulation.

Parameter	Default value	Recommended value
Gmin	1e-012 [S]	
Abstol	1e-012 [A]	
Reltol	0.001	0.0001
Chgtol	1e-014 [C]	
Trtol	1	0.1
Volttol	1e-006 [V]	
Sstol	0.001	
MinDeltaGmin	0.0001	

Table 2. Recommended values for the option parameters

Method 4: Sloped start of the power supply

If the simulation is stopped immediately after starting, provide a slope for the rise of the voltage source to avoid the problem. Figure 4 shows a typical voltage source. Since the setting voltage is generated as soon as the simulation is started, the voltage variation is abrupt in the components on the circuit. Set the rise time to slow the voltage variation. Click "Advanced" to open the setting window as shown in Figure 5. Although details may depend on the circuits, select "PULSE" and provide an adequate time for the "Trise" parameter.

Vin		· · · · · · · · · · · · · · · · · · ·
V1	🎔 Voltage Source - V1	×
800V	DC value[V]: 800V Series Resistance[Ω]:	OK Cancel
· · · · · · · · · · · · · · · · · · ·		Advanced

Figure 4. Setting for a typical voltage source

Independent Voltage Source - V1	×
Functions (none) PULSE(V1 V2 Tdelay Trise Tfall Ton Period Ncycles) SINE(Voffset Vamp Freq Td Theta Phi Ncycles) EXP(V1 V2 Td1 Tau1 Td2 Tau2) SFFM(Voff Vamp Fcar MDI Fsig) PWL(t1 v1 t2 v2) PWL FILE: Vinitial[V]: 0 Von[V]: 800 Tdelay[s]: 0 Tfall[s]: 0 Ton[s]: 1 Ncycles:	DC Value DC value: Make this information visible on schematic: ✓ Small signal AC analysis(AC) AC Amplitude: AC Phase: Make this information visible on schematic: ✓ Parasitic Properties Series Resistance[Ω]: Parallel Capacitance[F]: Make this information visible on schematic: ✓ V1 V1 PUIL SE(0 800 0 1000 0 1)
Additional PWL Points Make this information visible on schematic: 🗹	

Figure 5. Set the rise time in the advanced settings window for the voltage source

Other problems and countermeasures

Ideal passive elements

Inductors, transformers, and capacitors available as general symbols of the LTspice are ideal elements. Therefore, their impedance is infinite in the LC parallel resonance and zero in the serial resonance. This may prevent the convergence of the calculation.

Inductor

The default value for the inductors is $1m\Omega$ in the LTspice even if no serial resistance is set, mitigating the problem of extreme impedance. If $1m\Omega$ is still too small for the serial resistance, set the values individually.

· · · · · · · · · · · · · · · · · · ·	🎦 Inductor - L1 🛛 🕹 🗙
	Manufacturer: OK Part Number: Cancel
	Select Inductor Show Phase Dot
ο 200μ	Inductance[H]: 200µ
· · · · · · · · · · · · · · · · · · ·	Peak Current[A]:
· · · · · · · · · · · · · · · · · · ·	Parallel Resistance[Ω]:
· · · · · · · · · · · · · · · · · · ·	(Series resistance defaults to 1mΩ)
· · · · · · · · · · · · · · · · · · ·	

Figure 6. Set the serial resistance for the inductors. Default value is $1m\Omega$

Transformer

A transformer is created by combining the inductors. Although the serial resistance is set to $1m\Omega$ for the inductors by default, it becomes zero in the transformer configuration. Therefore, set "Series Resistance" to $1m\Omega$ or a greater value.

	🎦 Transformer Winding - L1 🛛 🗙
K1 L1 L2 0.999	Manufacturer: OK Part Number: Cancel
	Select Inductor Show Phase Dot 🗹
100µ 🌍 😓 10µ	Inductor Properties Inductance[H]: 100µ
	Peak Current[A]:
	Series Resistance[Ω]: 1m Parallel Resistance[Ω]:
	Parallel Capacitance[F]:
· · · · · · · · · · · · · · · · · · ·	



Capacitor

Since the serial resistance is zero by default, set "Equiv. Series Resistance" to $1m\Omega$ or a greater value.

	🔑 Capacitor - C1 🛛 💦 🗙
· · · · · · · · · · · · · · · · · · ·	Manufacturer: OK
· · · · · · · · · · · ·	Type: Cancel
	Select Capacitor
	Select Capacitor
C1	Capacitor Properties
· · · · ·	Capacitance[F]: 10µ
	Voltage Rating[V]:
	RMS Current Rating[A]:
	Equiv. Series Resistance[Ω]: 1m
	Equiv. Series Inductance[H]:
	Equiv. Parallel Resistance[Ω]:
	Equiv. Parallel Capacitance[F]:

Figure 8. Set the equivalent serial resistance for capacitor

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