Power Device

Calculation of Power Dissipation in Switching Circuit

In the power circuit design, it is important to confirm that the allowable loss for each device is not exceeded. Failing to do so may result in thermal breakdown of the devices. This application note describes how to calculate the power dissipation that occurs in a SiC MOSFET in a switching circuit using the SiC MOSFET during switching operations.

Loss measurement circuit

The double pulse test is one of the standard methods to measure the switching parameters of power devices. The measurement circuit is shown in Figure 1. The double pulse test is performed with the inductive load and the power supply. Since inductors are often used for the load in switching elements, an inductor is also used in the test circuit to achieve the same condition. The power supply is used to supply the voltage to the inductor. The signal generator (G) is used to output the pulses that drive the gate of the SiC MOSFET (Q1). The bulk capacitor (C1) is used to supply a large temporal current abruptly. This is intended to compensate for the responsiveness of the power supply.

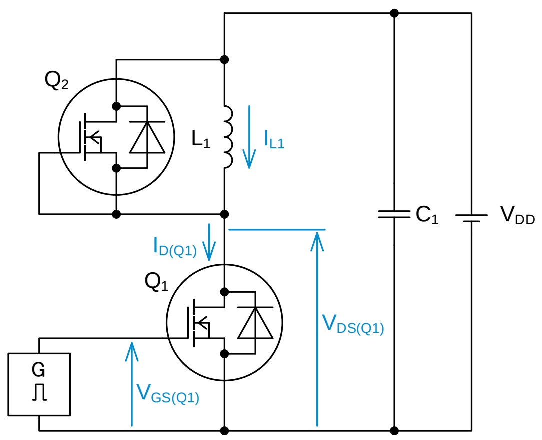

Figure 1. Double pulse test circuit

Figure 2 shows typical waveforms in the double pulse test. The top waveform shows the gate driving pulses. The turn OFF parameters are measured with the falling edge of the first pulse, while the turn ON parameters are measured with the rising edge of the second pulse.

Figure 3 shows the details of the turn OFF section. Turn OFF time t_{off} is defined as the time after V_{GS} is decreased to 90% until V_{DS} reaches 10% lower than V_{DD}. In addition, during this time frame, delay time $t_{d(off)}$ is defined as the time for V_{DS} to reach 90% lower than V_{DD}, and fall time t_f is defined as the time for V_{DS} to vary from 90% lower to 10% lower than V_{DD}. (Note: The description of 10% and 90% for V_{DS} is reversed compared with IEC60747-8.)

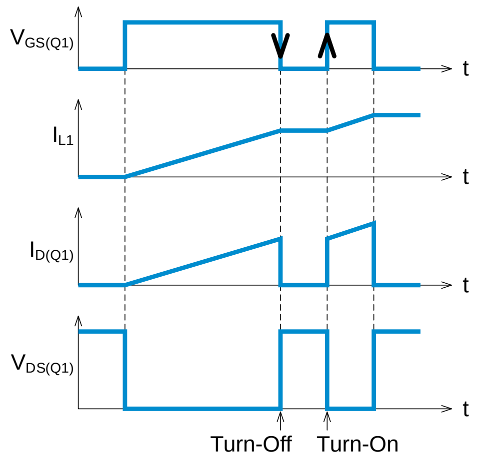

Figure 2. Waveforms of double pulse test

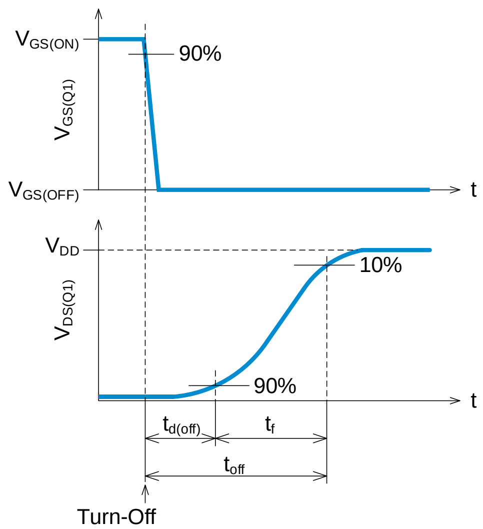

Figure 3. Definition of turn OFF time

Figure 4 shows the details of the turn ON section. Turn ON time t_{on} is defined as the time after V_{GS} is increased to 10% until V_{DS} reaches 90% lower than V_{DD}. In addition, during this time frame, delay time $t_{d(on)}$ is defined as the time for V_{DS} to reach 10% lower than V_{DD}, and rise time t_r is defined as the time for V_{DS} to vary from 10% lower to 90% lower than V_{DD}. (Note: The description of 10% and 90% for V_{DS} is reversed compared with IEC60747-8.)

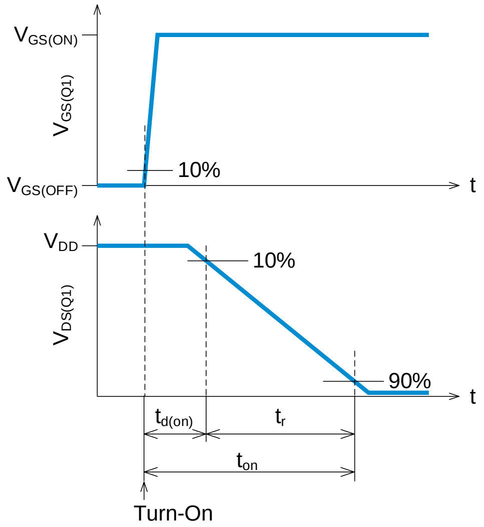

Figure 4. Definition of turn ON time

Next, the current flow in each step of the double pulse test is explained with reference to Figure 5.

Step 1: The first step is the first turn ON section. When low-side SiC MOSFET Q1 is turned ON, the current is supplied from the power supply to the inductor. At this time, as the current that flows to the inductor produces a magnetic field, the electric energy is converted to magnetic energy and stored in the inductor. Since the inductor current is increased in proportion to time, adjust the pulse width within this section so that the target test current (I_D) can be obtained.

Step 2: The second step is the first turn OFF section. When Q1 is turned OFF, the magnetic energy stored in the inductor is released as a current. The current is refluxed to the inductor via the flywheel diode again. In this case, the flywheel diode is the body diode of high-side SiC MOSFET Q2. Set the pulse width in this section as short as possible, so that the load current is kept constant as much as possible. However, an appropriate time should be secured to ensure that Q1 is turned OFF. Therefore, set a time that satisfies both of the conditions.

Step 3: The third step is the second turn ON section. An overshoot is observed in the I_D waveform immediately after Q1 is turned ON. Until just before then, the forward current is conducted in the body diode of Q2. When the state is switched to the reverse blocking, the reverse recovery current is conducted in the reverse direction temporarily, causing the overshoot. This is measured in the $I_{D(Q2)}$ of the high-side SiC MOSFET. When Q1 is turned ON, the current is supplied from the power supply to the inductor again. Then, I_D is increased again from the current value that is refluxed in step 2. Set the pulse width shorter than the first pulse to prevent the over current or heat from causing the destruction of the device. However, a certain time should be secured to ensure that Q1 is turned ON. Therefore, set the time that satisfies both of the conditions.

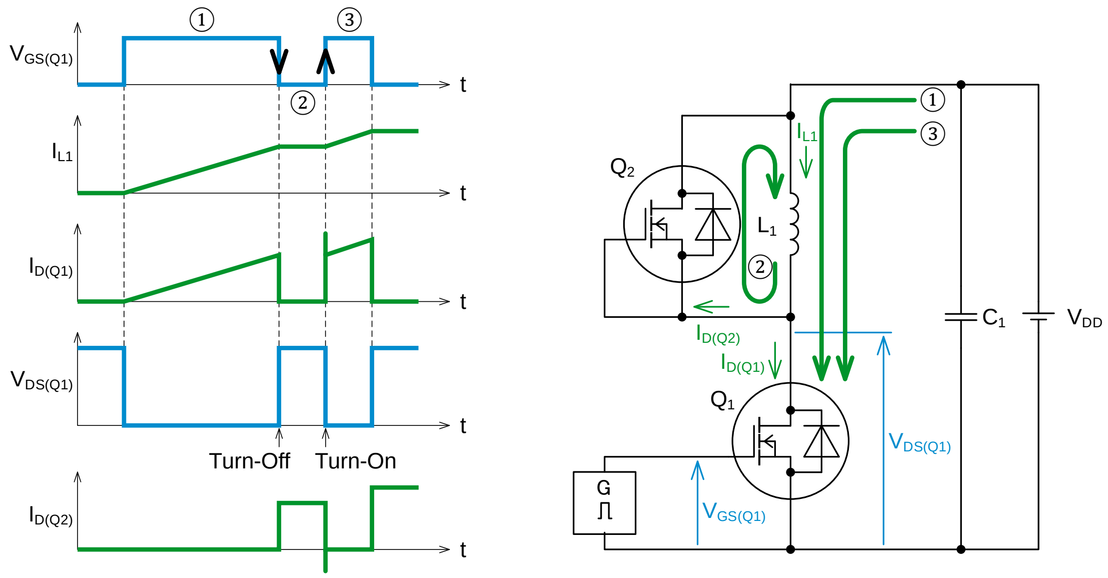

Figure 5. Current flow in each step of double pulse test

Calculation of loss

For the test circuit in Figure 1, the loss that occurs in the low-side SiC MOSFET includes the switching and conduction losses. In an ideal switching waveform, $V_{DS(Q1)}$ and $I_{D(Q1)}$ vary vertically without delay as shown in Figure 5. In this condition, no loss occurs because neither extra voltage nor extra current is generated. In actual cases, a delay is caused due to the parasitic resistance or capacitance. Therefore, the voltage and current waveforms vary, with slopes having t_{on} and t_{off} as shown in Figure 6. In this section with slopes, the area where the voltage and the current overlap causes the switching loss.

In actual circuits, the voltage and the current vary exponentially in the transition periods during the turn ON and the turn OFF. However, since it is difficult to express them with exponential functions from the observed waveforms, the calculations are performed using linear approximations.

From the waveforms in Figure 6, calculate the amount of power consumed in Q1 for each section separately. First, the amount of power W_{SW} consumed in turn ON time t_{on} and turn OFF time t_{off} (the switching time) can be approximated with Equation (1).

$$\begin{aligned} W_{SW} \approx & \frac{1}{2} V_{DS1(on)}\, I_{D2(on)}\, t_{on1} \\ & + \frac{1}{6} V_{DS1(on)} \left(2\, I_{D2(on)} + I_{D3(on)}\right) t_{on2} \\ & + \frac{1}{6}\, V_{DS2(off)} \left(I_{D1(off)} + 2\, I_{D2(off)}\right) t_{off1} \\ & + \frac{1}{2} V_{DS2(off)}\, I_{D2(off)}\, t_{off2} \quad [J] \end{aligned} \tag{1}$$

Next, calculate the amount of power consumed during the conduction. In Figure 6, since Q1 is conducting in the T_{ON} period, V_{DS} is the product of the on-resistance of Q1 and I_D. Refer to the data sheet for the value of the on-resistance. The amount of power W_{ON} can be approximated with Equation (2).

$$W_{ON} \approx \frac{1}{3} R_{ON(Q1)} \left(I_{D3(on)}^2 + I_{D3(on)} I_{D1(off)} + I_{D1(off)}^2\right) T_{ON} \quad [J] \tag{2}$$

where, $R_{on(Q1)}$: On-resistance of Q1 [Ω]

T_{ON}: ON time of Q1 [s]

Next is the amount of power while Q1 is turned OFF. This corresponds to the T_{OFF} period in Figure 6. Since I_D is zero while Q1 is turned OFF, the amount of power W_{OFF} is zero (Equation 3).

$$W_{OFF} = 0 \quad [J] \tag{3}$$

The total amount of power of Q1 can be obtained with Equation (4), being the summation from Equations (1) to (3).

$$W = W_{SW} + W_{ON} + W_{OFF} \quad [J] \tag{4}$$

Furthermore, the power dissipation in Q1 can be obtained with Equation (5).

$$P = \frac{W_{SW} + W_{ON} + W_{OFF}}{T} = (W_{SW} + W_{ON} + W_{OFF})\, f \quad [W] \tag{5}$$

where, T: Switching period [s]

f: Switching frequency [Hz]

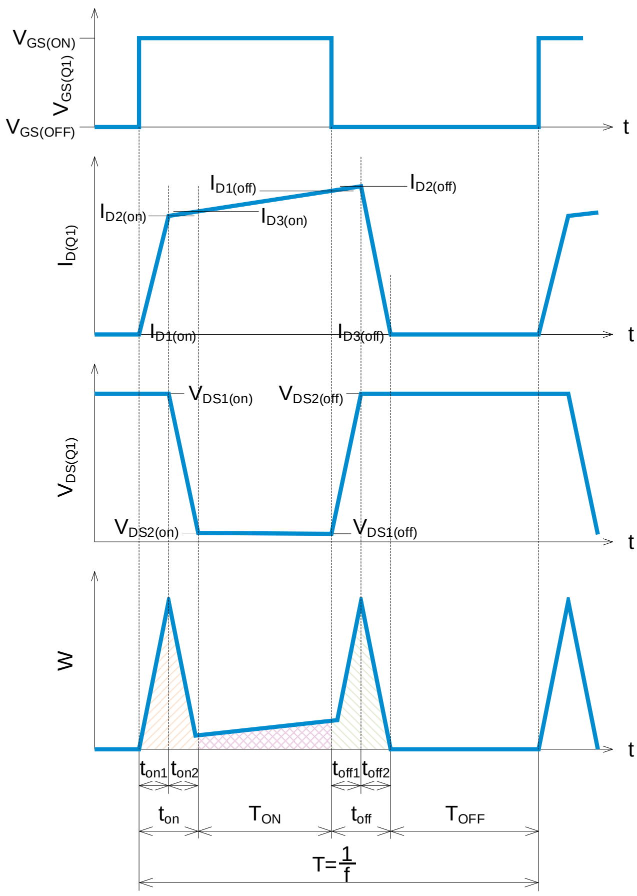

Figure 6. Example of waveforms for loss calculation

As described above, the loss is obtained with the integral approximation of the area where the voltage and the current overlap. However, different equations may appear in other materials. For example, the calculation can be further simplified by using equations to obtain areas of triangles or trapezoids for the overlapped area. These methods are used in cases where the error in calculation results remains small even after the simplification.

References

[1] IEC60747-8:2010, *Semiconductor devices – Discrete devices – Part 8: Field-effect transistors*

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