This document provides measurement test report of the RPT62-EVK001 board, which includes electrical characteristics, EMC noise and thermal measurement results. The RPT62-EVK001 is a power tree solution reference board developed for infotainment devices such as automotive clusters, center information displays, and ADAS ECUs. The power system that can support functional safety is integrated on a single board, realizing an optimal configuration as a power tree. It has good EMC performance that meets CISPR25 Class 5 test standard even when all power supplies are operating. Heat dissipation of each device is reduced by distributing high-efficiency DCDC. In addition, two voltage monitoring ICs with self-diagnosis functions can monitor the output of all systems, which contributes to a higher level of functional safety.

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System Block Diagram

System Block Diagram of RPT62-EVK001 is shown below.

![System Block Diagram](image)

**Figure 1 RPT62-EVK001 Automotive Power Tree Solution Board Block Diagram**

In this document, to distinguish between multiple products mounted on a board, the following symbol names are used hereinafter.

**Table 1 Symbol Name of Products Mounted on RPT62-EVK001**

<table>
<thead>
<tr>
<th>Symbol Name</th>
<th>Product Name</th>
<th>Input Voltage (typ) [V]</th>
<th>Output Voltage (typ) [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCDC_P5V</td>
<td>BD9P105EFV-C</td>
<td>12.0</td>
<td>5.0</td>
</tr>
<tr>
<td>DCDC_P5V_S1V25</td>
<td>BD9S201NUX-C</td>
<td>5.0</td>
<td>1.3</td>
</tr>
<tr>
<td>LDO_P5V_S3V3</td>
<td>BD001A5MEFJ-M</td>
<td>5.0</td>
<td>3.3</td>
</tr>
<tr>
<td>DCDC_P3V</td>
<td>BD9P205EFV-C</td>
<td>12.0</td>
<td>3.3</td>
</tr>
<tr>
<td>DCDC_P3V_S1V0</td>
<td>BD9S400MUF-C</td>
<td>3.3</td>
<td>1.0</td>
</tr>
<tr>
<td>DCDC_P3V_S1V5</td>
<td>BD9S300MUF-C</td>
<td>3.3</td>
<td>1.5</td>
</tr>
<tr>
<td>DCDC_P3V_S1V8</td>
<td>BD9S201NUX-C</td>
<td>3.3</td>
<td>1.8</td>
</tr>
<tr>
<td>DCDC_P3V_PSW</td>
<td>RV4C20ZPHZG</td>
<td>3.3</td>
<td>3.3</td>
</tr>
</tbody>
</table>
Operating Conditions

Operating condition of RPT62-EVK001 is shown in Table 2

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol in Power Tree</th>
<th>Limit</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>+B</td>
<td>9.0</td>
<td>12.0</td>
<td>16.0 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Breakdown Voltage=42V</td>
</tr>
<tr>
<td>Output Current*</td>
<td>DCDC_P5V</td>
<td>-</td>
<td>-</td>
<td>1.0 A</td>
</tr>
<tr>
<td></td>
<td>DCDC_P5V_S1V25</td>
<td>-</td>
<td>-</td>
<td>1.25 A</td>
</tr>
<tr>
<td></td>
<td>LDO_P5V_S3V3</td>
<td>-</td>
<td>-</td>
<td>0.2 A</td>
</tr>
<tr>
<td></td>
<td>DCDC_P3V</td>
<td>-</td>
<td>-</td>
<td>2.0 A</td>
</tr>
<tr>
<td></td>
<td>DCDC_P3V_S1V0</td>
<td>-</td>
<td>-</td>
<td>1.5 A</td>
</tr>
<tr>
<td></td>
<td>DCDC_P3V_S1V5</td>
<td>-</td>
<td>-</td>
<td>1.0 A</td>
</tr>
<tr>
<td></td>
<td>DCDC_P3V_S1V8</td>
<td>-</td>
<td>-</td>
<td>0.5 A</td>
</tr>
<tr>
<td></td>
<td>DCDC_P3V_PSW</td>
<td>-</td>
<td>-</td>
<td>0.15 A</td>
</tr>
</tbody>
</table>

*Output current specification with consideration of heat generated by the current load of each power supply IC.
List of Evaluation Items

List of evaluation items of RPT62-EVK001 is shown in Table 3. For more details on the specification of each power supply ICs, please refer to each datasheet.

<table>
<thead>
<tr>
<th>Chapter No.</th>
<th>Items</th>
<th>X-axis</th>
<th>Y-axis</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1</td>
<td>Output ripple waveform</td>
<td>Time</td>
<td>Output voltage</td>
<td></td>
</tr>
<tr>
<td>1.2</td>
<td>Conversion efficiency</td>
<td>Output current</td>
<td>Efficiency</td>
<td>VIN=12V</td>
</tr>
<tr>
<td>1.3</td>
<td>Load regulation</td>
<td>Output current</td>
<td>Output voltage</td>
<td>VIN=12V</td>
</tr>
<tr>
<td>1.4</td>
<td>Line regulation</td>
<td>Input voltage</td>
<td>Output voltage</td>
<td>VIN=8 ~18V</td>
</tr>
<tr>
<td>1.5</td>
<td>Shutdown current</td>
<td>Input voltage</td>
<td>Input current</td>
<td>VIN=1~18V</td>
</tr>
<tr>
<td>1.6</td>
<td>Load response</td>
<td>Output current</td>
<td>Output voltage</td>
<td>VIN=12V</td>
</tr>
<tr>
<td>1.7</td>
<td>Phase margin</td>
<td>Frequency</td>
<td>Gain, Phase</td>
<td>VIN=12V</td>
</tr>
<tr>
<td>1.8</td>
<td>Start-up waveform</td>
<td>Time</td>
<td>Output voltage</td>
<td>VIN=12V</td>
</tr>
<tr>
<td>1.9</td>
<td>Shutdown waveform</td>
<td>Time</td>
<td>Output voltage</td>
<td>VIN=12V</td>
</tr>
<tr>
<td>1.10</td>
<td>Switching node waveform</td>
<td>Time</td>
<td>Output voltage</td>
<td>VIN=12V</td>
</tr>
<tr>
<td>2</td>
<td>EMC performance</td>
<td>Frequency</td>
<td>Power</td>
<td>CISPR25 conductive, emission</td>
</tr>
<tr>
<td>3</td>
<td>Thermal measurement</td>
<td>---</td>
<td>---</td>
<td>Tjmax</td>
</tr>
</tbody>
</table>
1. Electrical Characteristics

1.1. Output Ripple Waveform

1.1.1 Measurement Setup

Measurement setup of output ripple waveform for each power supply ICs is shown below. Those ICs that are not measured are disabled by controlling the Enable pin.

![Measurement Setup Diagram]

Figure 2 Measurement Setup of Output Ripple Waveform
1.1.2 Waveforms
Measurement results of output ripple waveform for each power supply ICs are shown in Figure 3 to Figure 8.

Figure 3 Output Ripple Waveform of DCDC_P5V

Figure 4 Output Ripple Waveform of DCDC_P5V_S1V25

Figure 5 Output Ripple Waveform of DCDC_P3V
Figure 6  Output Ripple Waveform of DCDC_P3V_S1V0

Figure 7  Output Ripple Waveform of DCDC_P3V_S1V5

Figure 8  Output Ripple Waveform of DCDC_P3V_S1V8
1.2. Conversion Efficiency

1.2.1 Measurement Setup (for DCDC_P5V, DCDC_P3V)

Measurement setup of conversion efficiency for DCDC_P5V and DCDC_P3V is shown below. LEDs and supervisor ICs are removed from board under test while measuring efficiency.

![Diagram](image)

Figure 9 Measurement Setup of Conversion Efficiency and Load Regulation for DCDC_P5V, DCDC_P3V
1.2.2 Measurement Result (for DCDC_P5V, DCDC_P3V)

Measurement results of conversion efficiency for DCDC_P5V and DCDC_P3V are shown in Figure 10 and Figure 11 respectively. ICs are set up as “forced PWM” mode during the measurement.

Figure 10 Efficiency of DCDC_P5V

Figure 11 Efficiency of DCDC_P3V
1.2.3 Measurement Setup (for Secondary Power Supply ICs)

Measurement setup of conversion efficiency for secondary power supplies such as DCDC_P5V_S1V25, DCDC_P3V_S1V0 is shown below. LEDs and supervisor ICs are removed from board under test while measuring efficiency.

Figure 12 Measurement Setup of Conversion Efficiency and Load Regulation for Secondary Power Supply ICs.
1.2.4 Measurement Result (for Secondary Power Supply ICs)

Measurement results of conversion efficiency for secondary power supply ICs are shown in Figure 13 to Figure 17.

**Figure 13** Efficiency of DCDC_P5V_S1V25

**Figure 14** Efficiency of LDO_P5V_S3V3
Figure 15 Efficiency of DCDC_P3V_S1V0

Figure 16 Efficiency of DCDC_P3V_S1V5
Figure 17 Efficiency of DCDC_P3V_S1V8
1.3. Load Regulation

1.3.1 Measurement Setup (for DCDC_P5V, DCDC_P3V)

Measurement setup of load regulation for DCDC_P5V and DCDC_P3V is the same as conversion efficiency. Please refer to Figure 9.

1.3.2 Measurement Result (for DCDC_P5V, DCDC_P3V)

Measurement results of load regulation for DCDC_P5V and DCDC_P3V are shown in Figure 18 and Figure 19 respectively.

![Figure 18 Load Regulation of DCDC_P5V](image)

![Figure 19 Load Regulation of DCDC_P3V](image)
1.3.3 Measurement Setup (for Secondary Power Supply ICs)

Measurement setup of load regulation for secondary power supply ICs such as DCDC_P5V_S1V25 and DCDC_P3V_S1V0 etc. is the same as conversion efficiency. Please refer to Figure 12.

1.3.4 Measurement Result (for Secondary Power Supply ICs)

Measurement results of load regulation for power supply ICs are shown in Figure 20 and Figure 24.

![Figure 20 Load Regulation of DCDC_P5V_S1V25](image1)

![Figure 21 Load Regulation of LDO_P5V_S3V3](image2)
Figure 22 Load Regulation of DCDC_P3V_S1V0

Figure 23 Load Regulation of DCDC_P3V_S1V5
Figure 24 Load Regulation of DCDC_P3V_S1V8
1.4. Line Regulation

1.4.1 Measurement Setup

Measurement setup of line regulation is shown below.

![Diagram of Measurement Setup](image)

**Figure 25 Measurement Setup of Line Regulation**
1.4.2 Measurement Result

Measurement results of line regulation are shown in Figure 26 and Figure 27.

![Figure 26 Line Regulation of DCDC_P5V](image)

![Figure 27 Line Regulation of DCDC_P3V](image)
1.5. Shutdown Current

Shutdown current measures the input current while varying the input voltage. All power supply ICs are disabled by controlling the Enable terminal.

![Shutdown Current Graph](image)

*Figure 28 Shutdown Current (Entire board)*
1.6. Load Response

1.6.1 Measurement Setup (for DCDC_P5V, DCDC_P3V)

Measurement setup of load response for DCDC_P5V and DCDC_P3V is shown in Figure 29.

![Figure 29 Measurement Setup of Load Response for DCDC_P5V and DCDC_P3V](image)
1.6.2 Measurement Result (for DCDC_P5V, DCDC_P3V)

Measurement results of load response for DCDC_P5V and DCDC_P3V are shown in Figure 30 and Figure 31 respectively.

![Figure 30 Load Response of DCDC_P5V](image)

![Figure 31 Load Response of DCDC_P3V](image)
1.6.3 Measurement Setup (for Secondary Power Supply ICs)

Measurement setup of load response for secondary power supply ICs is shown in Figure 32.

![Diagram](Image)

**Figure 32 Measurement Setup of Load Response for Secondary Power Supply ICs**
1.6.4 Measurement Result (for Secondary Power Supply ICs)

Measurement results of load response for secondary power supply ICs are shown in Figure 33 to Figure 38.

**Figure 33 Load Response of DCDC_P5V_S1V25**

**Figure 34 Load Response of LDO_P5V_S3V3**

**Figure 35 Load Response of DCDC_P3V_S1V0**
Figure 36 Load Response of DCDC_P3V_S1V5

Figure 37 Load Response of DCDC_P3V_S1V8

Figure 38 Load Response of DCDC_P3V_PSW
1.7. Phase Margin

1.7.1 Measurement Setup (for DCDC_P5V, DCDC_P3V)

Measurement setup of phase margin for DCDC_P5V and DCDC_P3V is shown in Figure 39.

![Figure 39 Measurement Setup of Phase Margin for DCDC_P5V and DCDC_P3V](image)
1.7.2 Measurement Result (for DCDC_P5V, DCDC_P3V)

Measurement results of phase margin for DCDC_P5V and DCDC_P3V are shown in Figure 40 and Figure 41 respectively.

![Figure 40 Phase Margin of DCDC_P5V](image1)

![Figure 41 Phase Margin of DCDC_P3V](image2)
1.7.3 Measurement Setup (for Secondary Power Supply ICs)

Measurement setup of phase margin for secondary power supply ICs is shown in Figure 42.

![Measurement Setup Diagram]

**Figure 42 Measurement Setup of Phase Margin for Secondary Power Supply ICs**

1.7.4 Measurement Result (for Secondary Power Supply ICs)

**Measurement results of phase margin for secondary power supply ICs are shown in Figure 43 to Figure 47.**

![Phase Margin Diagram]

**Figure 43 Phase Margin of DCDC_P5V_S1V25**
Figure 44 Phase Margin of LDO_P5V_S3V3

Figure 45 Phase Margin of DCDC_P3V_S1V0

Figure 46 Phase Margin of DCDC_P3V_S1V5
Figure 47 Phase Margin of DCDC_P3V_S1V8
1.8. Start-up Waveform

1.8.1 Measurement Setup (for DCDC_P5V, DCDC_P3V)
Measurement setup of start-up waveform and shutdown waveform is shown in Figure 48.

![Figure 48 Measurement Setup of Start-up Waveform and Shutdown Waveform for DCDC_P5V and DCDC_P3V](image)

1.8.2 Measurement Result (for DCDC_P5V, DCDC_P3V)
Measurement results of start-up waveform for DCDC_P5V and DCDC_P3V are shown in Figure 49 and Figure 50 respectively.

![Figure 49 DCDC_P5V Start-up Waveform](image)
Figure 50 DCDC_P3V Start-up Waveform
1.8.3 Measurement Setup (for Secondary Power Supply ICs)

Measurement setup of start-up waveform and shutdown waveform for secondary power supply ICs is shown in Figure 51.

![Measurement Setup Diagram]

**Figure 51  Measurement Setup of Start-up Waveform and Shutdown Waveform for Secondary Power Supply ICs**

1.8.4 Measurement Result (for Secondary Power Supply ICs)

Measurement results of start-up waveform for secondary power supply ICs are shown in Figure 52 to Figure 57.

![Start-up Waveform Graph]

**Figure 52 DCDC_P5V_S1V25 Start-up Waveform**
Figure 53 LDO_P5V_S3V3 Start-up Waveform

Figure 54 DCDC_P3V_S1V0 Start-up Waveform

Figure 55 DCDC_P3V_S1V5 Start-up Waveform
Figure 56 DCDC_P3V_S1V8 Start-up Waveform

Figure 57 DCDC_P3V_PSW Start-up Waveform
1.9. Shutdown Waveform

1.9.1 Measurement Setup (for DCDC_P5V, DCDC_P3V)
Measurement setup of shutdown waveform for DCDC_P5V and DCDC_P3V is shown in Figure 48.

1.9.2 Measurement Result (for DCDC_P5V, DCDC_P3V)
Measurement results of shutdown waveform for DCDC_P5V and DCDC_P3V are shown in Figure 58 and Figure 59 respectively.

---

Figure 58 DCDC_P5V Shutdown Waveform

![DCDC_P5V Shutdown Waveform](image1)

Figure 59 DCDC_P3V Shutdown Waveform

![DCDC_P3V Shutdown Waveform](image2)
1.9.3 Measurement Setup (for Secondary Power Supply ICs)
Measurement setup of shutdown waveform for secondary power supply ICs is shown in Figure 51. There is no load applied in the output of each power supply.

1.9.4 Measurement Result (for Secondary Power Supply ICs)
Measurement results of shutdown waveform for secondary power supply ICs are shown in Figure 60 to Figure 65.

Figure 60 DCDC_P5V_S1V25 Shutdown Waveform

Figure 61 LDO_P5V_S3V3 Shutdown Waveform
Figure 62 DCDC_P3V_S1V0 Shutdown Waveform

Figure 63 DCDC_P3V_S1V5 Shutdown Waveform

Figure 64 DCDC_P3V_S1V8 Shutdown Waveform
Figure 65 DCDC_P3V_PSW Shutdown Waveform
1.10. Switching Node Waveform

1.10.1 Measurement Setup (for DCDC_P5V, DCDC_P3V)
Measurement setup of switching node waveform for DCDC_P5V and DCDC_P3V is shown in Figure 66.

![Figure 66 Measurement Setup of Switching Node Waveform for DCDC_P5V and DCDC_P3V](image-url)
1.10.2 Measurement Result (for DCDC_P5V, DCDC_P3V)

Measurement results of switching node waveform for DCDC_P5V and DCDC_P3V are shown in Figure 67 and Figure 68 respectively.

![Figure 67 DCDC_P5V Switching Node Waveform](image)

![Figure 68 DCDC_P3V Switching Node Waveform](image)
1.10.3 Measurement Setup (for Secondary Power Supply ICs)

Measurement setup of switching node waveform for secondary power supply ICs is shown in Figure 69.

![Figure 69 Measurement Setup of Switching Node Waveform for Secondary Power Supply ICs](image)
1.10.4 Measurement Result (for Secondary Power Supply ICs)

Measurement results of switching node waveform for secondary power supply ICs are shown in Figure 70 to Figure 73.

Figure 70 DCDC_P5V_S1V25 Switching Node Waveform

Figure 71 DCDC_P3V_S1V0 Switching Node Waveform
Figure 72 DCDC_P3V_S1V5 Switching Node Waveform

Figure 73 DCDC_P3V_S1V8 Switching Node Waveform
2. EMC Performance

RPT62-EVK001 is able to meet CISPR25 Class5 EMC test standard. In testing, CISPR standard is cleared without a common mode noise filter.

2.1. Operating Condition during EMC Measurement

Operating condition of each power supply IC during EMC measurement is shown in Table 4.

<table>
<thead>
<tr>
<th>Symbol Name</th>
<th>Output Loads</th>
<th>Operating Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCDC_P5V</td>
<td>Vout=5.02V, Iout=0.3V</td>
<td>Enabled, SSCG ON, Forced PWM mode</td>
</tr>
<tr>
<td>DCDC_P5V_S1V25</td>
<td>Vout=1.25V, Iout=1.32A</td>
<td>Enabled</td>
</tr>
<tr>
<td>LDO_P5V_S3V3</td>
<td>Vout=3.33V, Iout=0.26A</td>
<td>Enabled</td>
</tr>
<tr>
<td>DCDC_P3V</td>
<td>Secondary DCDCs, PSW</td>
<td>Enabled, SSCG ON, Forced PWM mode</td>
</tr>
<tr>
<td>DCDC_P3V_S1V0</td>
<td>Vout=1.01V, Iout=2.2A</td>
<td>Enabled, Forced PWM mode</td>
</tr>
<tr>
<td>DCDC_P3V_S1V5</td>
<td>Vout=1.52V, Iout=1.49A</td>
<td>Enabled, Forced PWM mode</td>
</tr>
<tr>
<td>DCDC_P3V_S1V8</td>
<td>Vout=1.80V, Iout=1.22A</td>
<td>Enabled</td>
</tr>
<tr>
<td>DCDC_P3V_PSW</td>
<td>Vout=3.23V, Iout=0.38A</td>
<td>On</td>
</tr>
</tbody>
</table>
2.2. EMC Measurement Result

2.2.1 Conductive Noise Measurement Result

Conductive noise measurement result of RPT62-EVK001 is shown in Figure 74.

![Conductive Noise Emission of RPT62-EVK001](image)

**Figure 74 Conductive Noise Emission of RPT62-EVK001**

2.2.2 Radiated Noise (Antenna Face in Horizontal Direction) Measurement Result

Measurement result of radiated noise (antenna face in horizontal direction) of PRT62-EVK001 is shown in Figure 75.

![Radiated Noise Emission (Antenna Horizontal) of RPT62-EVK001](image)

**Figure 75 Radiated Noise Emission (Antenna Horizontal) of RPT62-EVK001**
2.2.3 Radiated Noise (Antenna Face in Vertical Direction) Measurement Result

Measurement result of radiated noise (antenna face in vertical direction) of PRT62-EVK001 is shown in Figure 76.

![Figure 76 Radiated Noise Emission (Antenna Vertical) of RPT62-EVK001](image-url)
3. Thermal Measurement

The following section shows the thermal measurement results of RPT62-EVK001 under the specified load conditions.

3.1. Measurement Setup

In the thermal measurement of RPT62-EVK001, measurement is performed with the following setup.

![Thermography Diagram]

Figure 77 Measurement Setup of RPT62-EVK001 during Thermal Measurement
3.2. Measurement Result

Thermal measurement result of RPT62-EVK001 is shown below. Measurement result is shown as the difference from room temperature.

Figure 78 Thermal Measurement Result of RPT62-EVK001
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More detail product informations and catalogs are available, please contact us.

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