Diode

PCB Layout for TVS Diodes

Transient voltage suppressor (TVS) diodes have been developed as specialized products showing high performance in protecting semiconductor devices from static electricity and unexpected surge voltage. However, if the PCB layout is inappropriate, the TVS diodes cannot deliver their performance and their protective function is impaired. This application note explains how to determine an appropriate PCB layout for the TVS diodes.

Example of breakdown and countermeasures

There are cases where an analysis of an IC returned by a customer as a defective item found a breakdown due to electrostatic discharge (ESD). Figures 1 and 2 show the circuit diagram and the PCB layout, respectively.

As shown in the circuit diagram, the TVS diodes are placed between the connector exposed to the outside of the chassis and the IC so that the TVS diodes can absorb the energy of ESD entering from the connector. Next, as shown in the PCB layout, although the connection is electrically the same as the circuit diagram, the TVS diodes are placed on a corner of the board. This could happen when the importance of the countermeasures against ESD is not appreciated. In this case, the TVS diodes were placed in an empty area after the main circuit was laid out preferentially.

The equivalent circuit in Figure 3 is obtained by applying the parasitic inductance generated by the wiring to this PCB layout. Parasitic inductances L_{P1} and L_{P2} are placed between the diode cathodes and the wiring to be protected. The anode sides are connected to the ground plane with a low impedance.

Figure 4 shows a current waveform when a direct contact discharge is generated at 8 kV according to the IEC 61000-4-2 electrostatic testing standard. Since the ESD waveform is an instantaneous pulse, a large overshoot occurs in the clamping voltage of the TVS diodes due to the parasitic inductance.

If the current propagating the wiring with parasitic inductance L [H] is varied by i [A] during time t [s], the voltage in Equation (1) occurs at both ends of the print pattern. From this equation, it can be seen that the voltage is increased as the L value is increased.

$$|V| = L \times \frac{di}{dt} \ [V] \qquad (1)$$

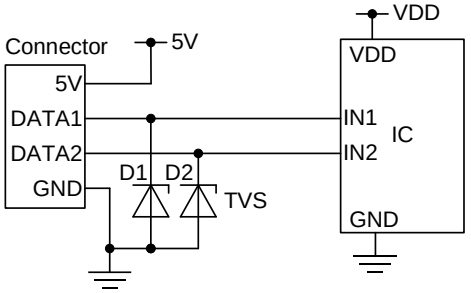

Figure 1. Circuit diagram in which the IC input terminals are protected with the TVS diodes

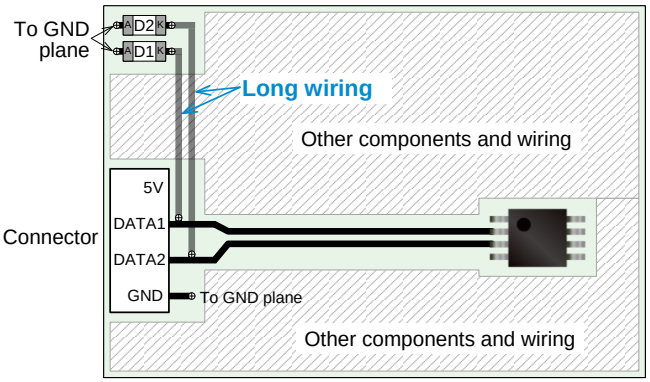

Figure 2. PCB layout in which ESD caused a breakdown of the IC

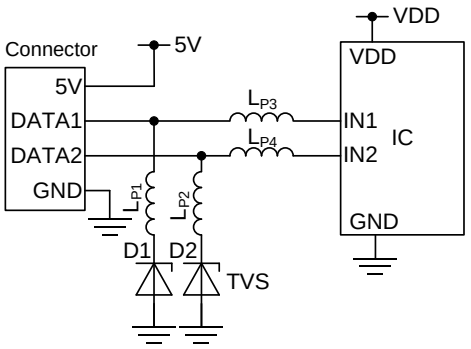

Figure 3. Equivalent circuit diagram taking parasitic inductance of wiring into consideration

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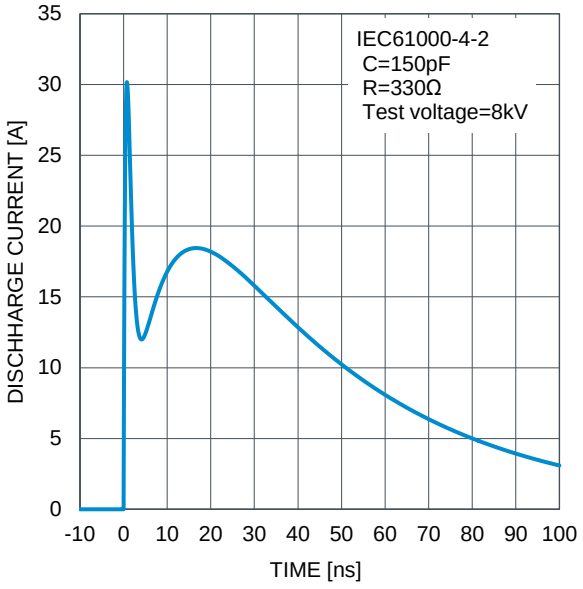

Figure 4. Current waveform of direct contact discharge

The inductance value of the copper foil wiring can be estimated with Equation (2). Typical calculation results are shown in Figure 5.

$$L = 0.2\,l\left(\ln\frac{2\,l}{w+t} + 0.2235\frac{w+t}{l} + 0.5\right) \quad [nH] \qquad (2)$$

l : Conductor length $[mm]$
w : Conductor width $[mm]$
t : Copper foil thickness $[mm]$

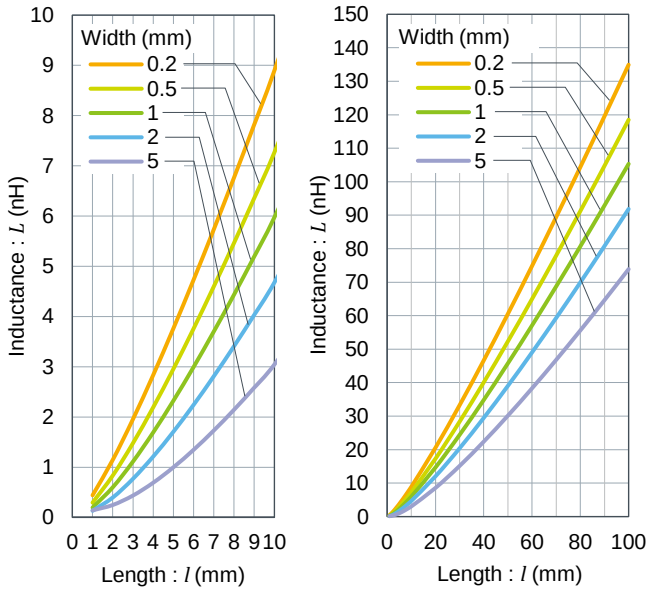

Figure 5. Inductance of copper foil wiring
t = 0.035 mm

For example, the parasitic inductance is 52 nH between the connector and D1 in the layout in Figure 2 if a wiring length of 50 mm and wiring width of 0.5 mm are assumed. The parasitic inductance between the connector and the IC is 91 nH if a wiring length of 80 mm and wiring width of 0.5 mm are assumed.

Figure 6 shows the simulation circuit under these conditions. The left end is an equivalent model of ESD gun. SW1 triggers a direct contact discharge in the direction of the IC.

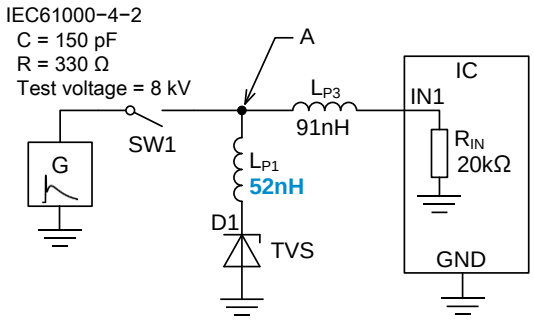

Figure 6. Simulation circuit for direct contact discharge test including parasitic inductance of wiring

Figure 7 shows the simulation result for the voltage waveform at point A on the wiring to be protected. It can be seen that the electricity generated due to the parasitic inductance increases the first peak voltage up to 3.4 kV and the voltage is not clamped by the TVS diode. This indicates that the features of the TVS diode is not functioning at all.

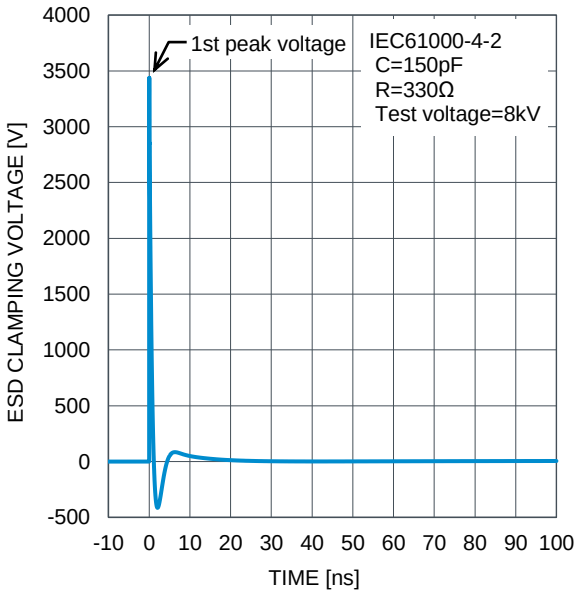

Figure 7. Simulation result for ESD clamping voltage when the parasitic inductance value is large

Next, Figure 8 shows an appropriate PCB layout. The layout minimizes the distance between the wiring to be protected and the cathode of the TVS diode in order to reduce the parasitic inductance.

Since the diode is placed directly above the wiring to be protected in this layout, the parasitic inductance is assumed to be 1 nH for performing the simulation. Figures 9 and 10 show the simulation circuit and the result, respectively. The first peak voltage is suppressed down to 107 V and the subsequent part is also suppressed with the clamping voltage.

Thus, it is obviously very important to reduce the parasitic inductance of the wiring in the layout.

These simulations are different from the actual waveforms because the simulations are intended to show how the difference in the parasitic inductances of the wiring changes the clamping performance.

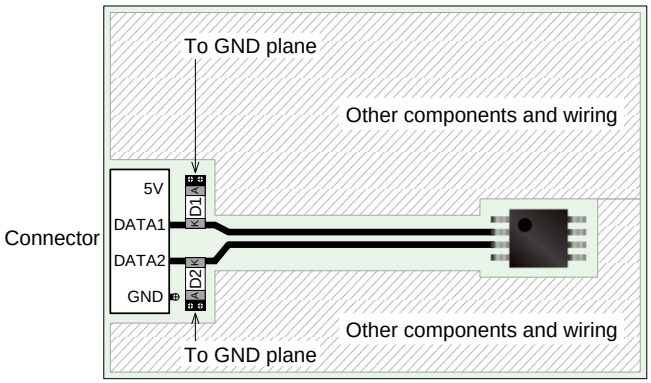

Figure 8. Appropriate layout for TVS diodes
Reduce the parasitic inductance between the wiring to be protected and the diode cathode as much as possible.

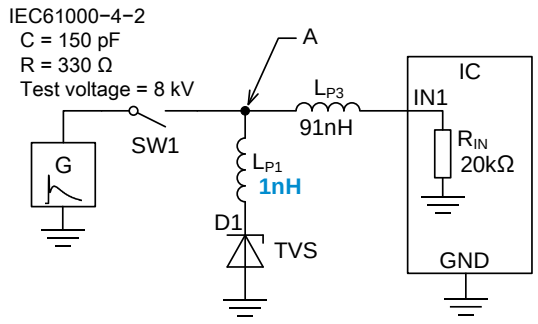

Figure 9. Simulation circuit for direct contact discharge test when the parasitic inductance of wiring is minimized

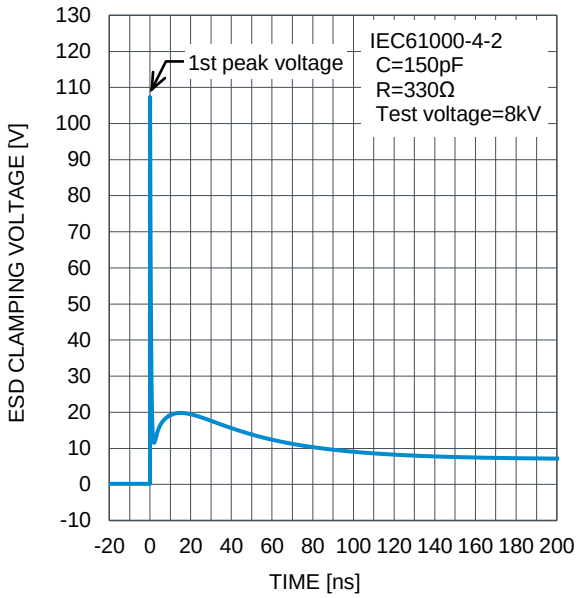

Figure 10. Simulation result for ESD clamping voltage when the parasitic inductance value is small

Although the explanation above is for the cathode side of the diode, the same measures are required on the anode side. It is recommended to connect the anode to the ground plane with a low impedance. However, if the ground plane is not located directly below the diode, the wiring from the anode to the ground plane is extended as shown in Figure 11. As a result, the surge voltage cannot be clamped as is the case for the extended wiring on the cathode side. Determine the layout so that the ground plane is preferentially located directly below the diode.

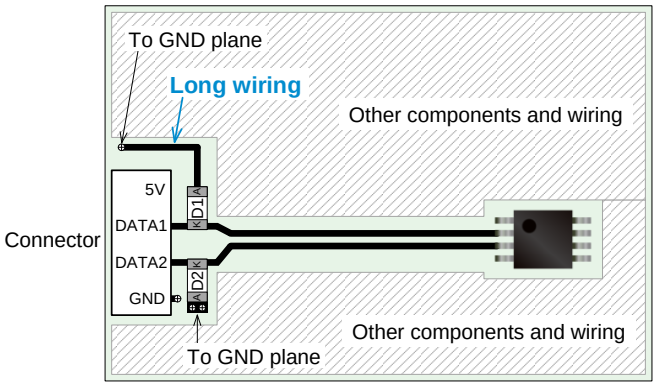

Figure 11. Inappropriate PCB layout with extended wiring on anode side

Guidelines for PCB layout

The following guidelines for PCBs are recommended in order to deliver the surge suppressive performance of the TVS diodes, with consideration of breakdown examples.

1. Minimize the parasitic inductance due to the PCB wiring (trace).

2. Place the TVS diode close to the ESD entry source.

3. Connect the TVS diode to the ground of the power supply or chassis.

1. Minimize the parasitic inductance due to the PCB wiring (trace)

As explained for the breakdown example in the previous section, it is necessary to minimize the parasitic inductance by decreasing the distances between the cathode of the TVS diode and the wiring to be protected as well as between the anode and the ground plane.

Figure 12 shows an example of appropriate PCB layout. The parasitic inductance is minimized with the layout in which the wiring distances between the diode cathode and the wiring to be protected as well as between the anode and the ground plane are minimized. Figures 13 and 14 show inappropriate examples. The parasitic inductance affecting the surge suppression is applied because of a long distance between the diode cathode and the wiring to be protected (Figure 13) or between the anode and the ground plane (Figure 14).

Since even a few nH of parasitic inductance can have an impact, refer to Equation (2) and Figure 5 for the value. Increasing the wiring width is also an effective method to decrease the value.

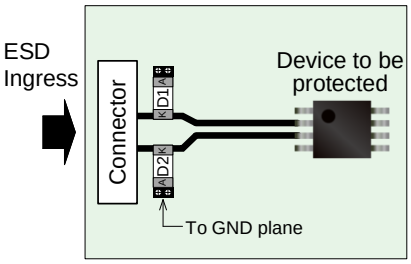

Figure 12. Appropriate PCB layout

In this layout, the wiring distances between the diode cathode and the wiring to be protected as well as between the anode and the ground plane are minimized.

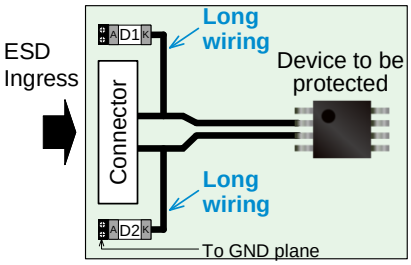

Figure 13. Inappropriate PCB layout

The parasitic inductance affecting the surge suppression is applied because of a long distance between the diode cathode and the wiring to be protected.

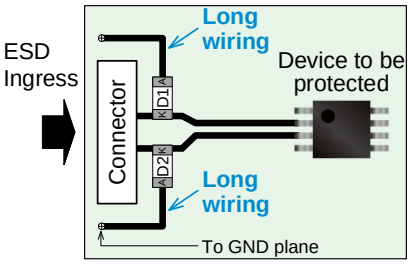

Figure 14. Inappropriate PCB layout

The parasitic inductance affecting the surge suppression is applied because of a long distance between the diode anode and the ground plane.

The anode side of the diode is connected to the ground plane through the via. However, the via also has a parasitic inductance. The inductance value can be estimated with Equation (3). Typical calculation results are shown in Figure 15. The value can be decreased by arranging several vias.

$$L = 0.2\,h\left(\ln\frac{4\,h}{d} + 1\right) \quad [nH] \qquad (3)$$

h : Via height $[mm]$
d : Via diameter $[mm]$

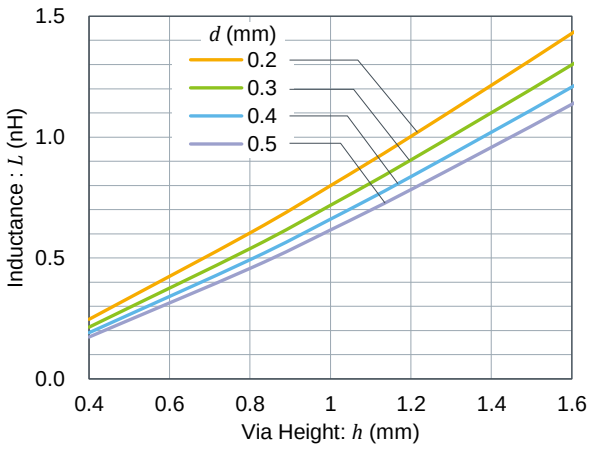

Figure 15. Via inductance

2. Place the TVS diode close to the ESD entry source

In many applications, ESD enters through the I/O connector. Therefore, the TVS diode must be placed as close to the ESD entry source as possible. Figure 16 shows an example of appropriate PCB layout in which the TVS diode is placed immediately next to the connector. The surge pulse voltage is clamped at the position of the TVS diode and prevented from entering the inside further.

Figure 17 shows an example of inappropriate PCB layout. Since the TVS diode is placed away from the connector, the ESD pulse enters the inside of the PCB. If the wiring (trace) is placed nearby, the surge pulse may enter other circuits through the capacitive coupling, causing an adverse effect. In addition, a TVS diode with a higher performance is required because the peak voltage of the surge pulse is increased by the parasitic inductance between the connector and the TVS diode.

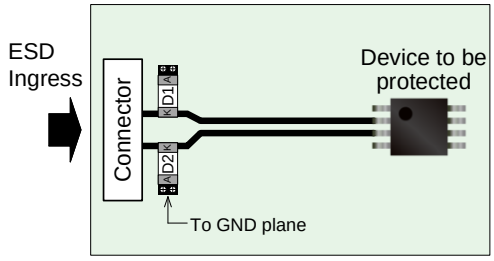

Figure 16. Appropriate PCB layout

The surge pulse can be prevented from entering the inside further by placing the TVS diode immediately next to the connector.

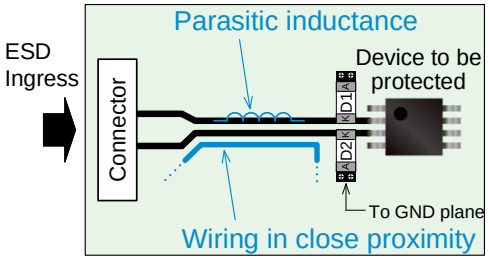

Figure 17. Inappropriate PCB layout

The surge pulse may enter the inside of the PCB, causing an adverse effect on adjacent circuits.

3. Connect the TVS diode to the ground of the power supply or chassis

It is recommended to connect the ground side of the TVS diode to the ground of the power supply or chassis with a low impedance (Figure 18).

Since the ground of the signal processing IC often has a narrow wiring width, a large current may flow due to the ESD pulse if the TVS diode is connected to this ground. As a result, the ground potential is varied (ground bounce occurs) due to the common impedance, causing a communication error (Figure 19).

For single layer boards, it is necessary to minimize the ground impedance by using a broad wiring width because there is no ground plane.

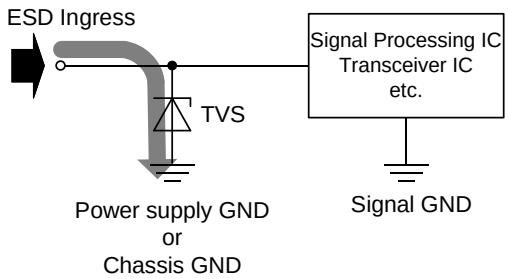

Figure 18. Appropriate design technique

It is recommended to connect the ground side of the TVS diode to the ground of the power supply or chassis with a low impedance.

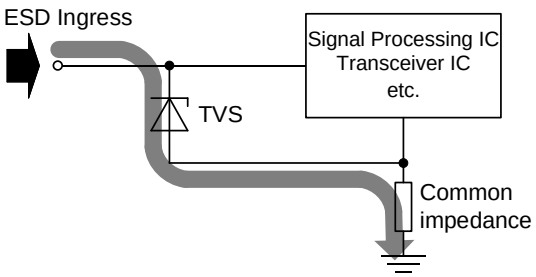

Figure 19. Inappropriate design technique

If the TVS diode is connected to a ground with a narrow wiring width, the ground potential of the IC is varied due to the common impedance, causing an adverse effect on the IC functions.

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