Application Note

SiC MOSFET

5 kW High-Efficiency Fan-less Inverter

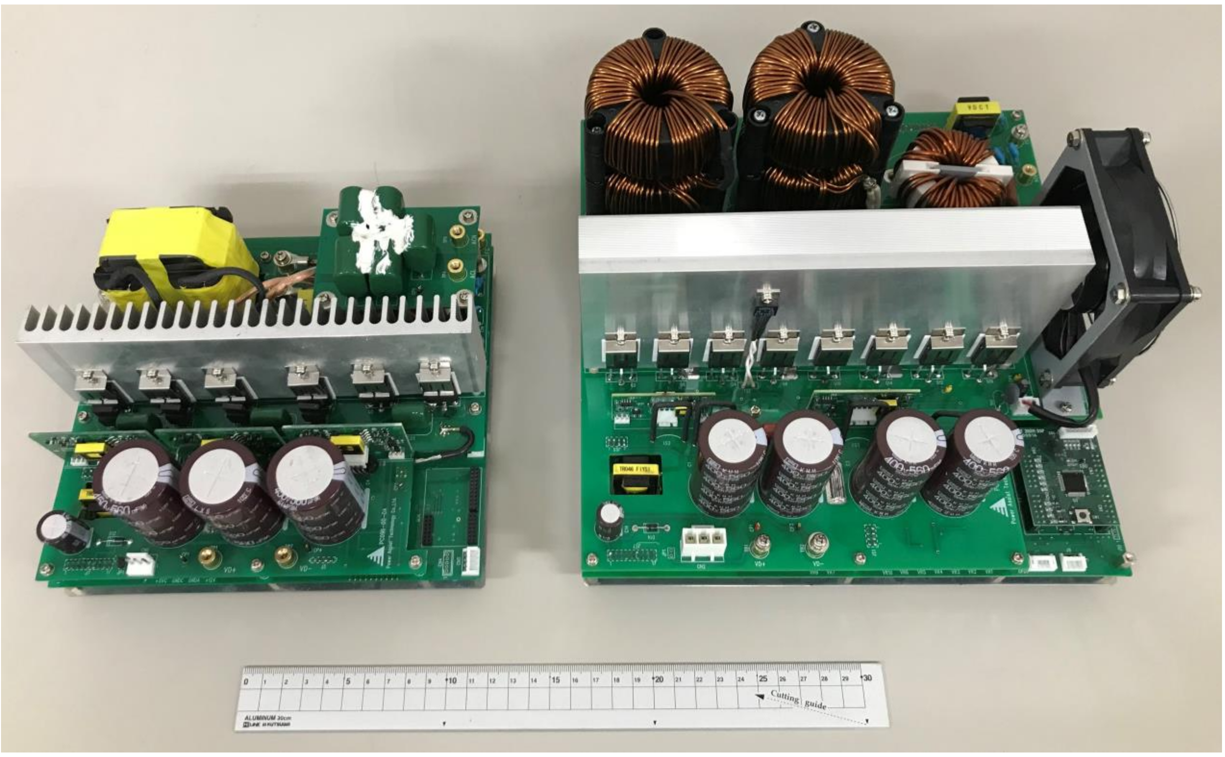
We employ trans-linked interleaved circuits as inverter circuits that utilize the high frequency switching performance of silicon carbide (SiC) MOSFET(1), achieving a power conversion efficiency of 99% or more at 5 kW. Since this circuit topology allows a reduction in the inductance of the smoothing reactor, the high efficiency is achieved by reducing the number of windings of the reactor to dramatically reduce the copper loss. This document introduces an example of this novel inverter design.

These novel inverter circuits have been developed jointly with Power Assist Technology Ltd. (https://www.power-assist-tech.co.jp/)

Comparison with conventional circuit

Figure 1 shows a comparison of the full bridge type with conventional circuit configuration (conventional type) and the trans-linked interleaved type (interleaved type) introduced in this document. The output power of both types is 5 kW.

Although the conventional type is configured with two IGBT (STGW60H65DFB) as switching devices in parallel, its efficiency of 97.4% at 5 kW (total loss 133 W) requires a cooling fan. In contrast, since the interleaved type using SiC MOSFET (SCT3017AL, SCT3030AL) has an efficiency of 99.0% (total loss 51 W), heat generation is reduced, and the circuit can be cooled with downsized heat radiation fins without using a cooling fan. Furthermore, since the apparent switching frequency is doubled for the interleaved type, the smoothing filter is downsized by a factor of 2 in its size and weight.



(a) Trans-linked interleaved type (b) Full bridge type (conventional)

Figure 1. Comparison with conventional circuit configuration

Circuit configuration

Figure 2 shows a diagram of the circuit configuration for the interleaved type.

This inverter circuit has three half bridges (B1, B2, and B3). Each half bridge contains two transistors (Q_{Hk} and Q_{Lk}, k = 1, 2, and 3). A Schottky barrier diode (SBD) is connected with the transistors in parallel as a free wheeling diode. B2 and B3 are operated in the PWM mode with their phases inverted by 180° relative to each other. B1 is operated as a low frequency switching bridge with Q_{H1} and Q_{L1} alternately switched at 50 Hz. The output lines of B2 and B3 interact with each other via the coupling reactor (L_c), and the currents are added after flowing through L_c. The output lines of B2 and B3 and the middle point of B1 are connected to the output capacitor (C_o).

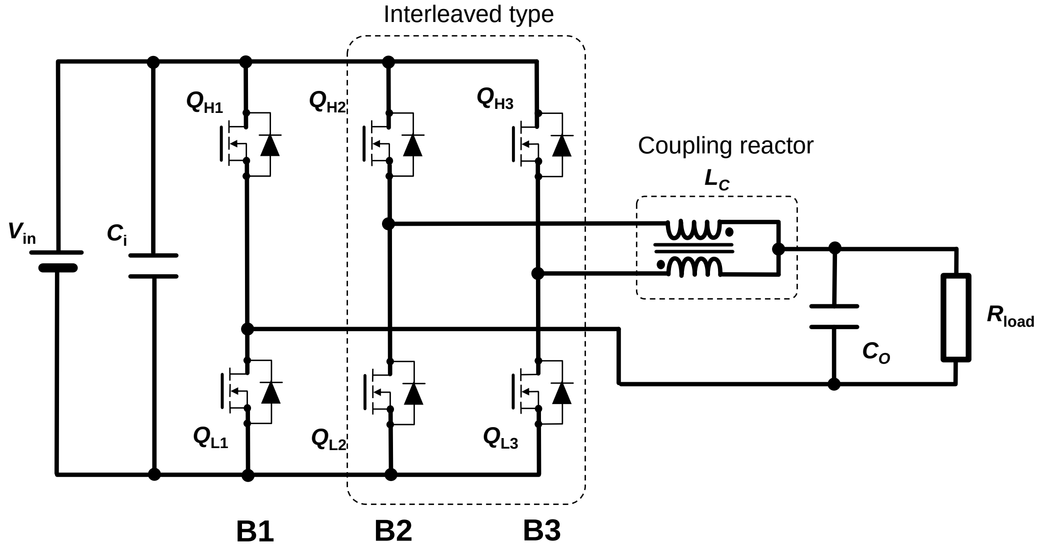


Figure 2. Trans-linked interleaved inverter circuit

Figure 3 shows an equivalent circuit to the coupling reactor.

The coupling reactor can be divided into two leakage inductances (L_1 and L_2), a magnetizing inductance (L_m), and an ideal reverse polarity transformer. V_{L1}, V_{L2}, V_1, and V_2 represent self-induced electromotive forces of the respective inductances shown in Figure 3. i_{L1}, i_{L2}, i_1, i_2, and i_m are currents defined in Figure 3. Assume that the PWM part is operated with duty ratio d when Q_{H2} is ON. Because of the inverter operation, d varies with time. For the sake of convenience, assume that L_1 and L_2 have the same inductance represented with L. Except for the dead time period, all half bridges in the inverter are operated with synchronous rectification.

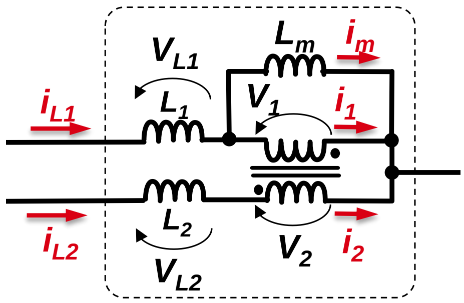


Figure 3. Equivalent circuit to coupling reactor (L_c)

The relationship between V_{in} and V_{out} is represented with Equation (1), similarly to the relationship for normal buck converters.

$$V_{\text{out}} = dV_{\text{in}} \qquad (1)$$

Theoretical analyses of the interleaved buck converters have already been discussed in various publications (*4) to (*6). The same calculations are applied to this trans-linked type as well.

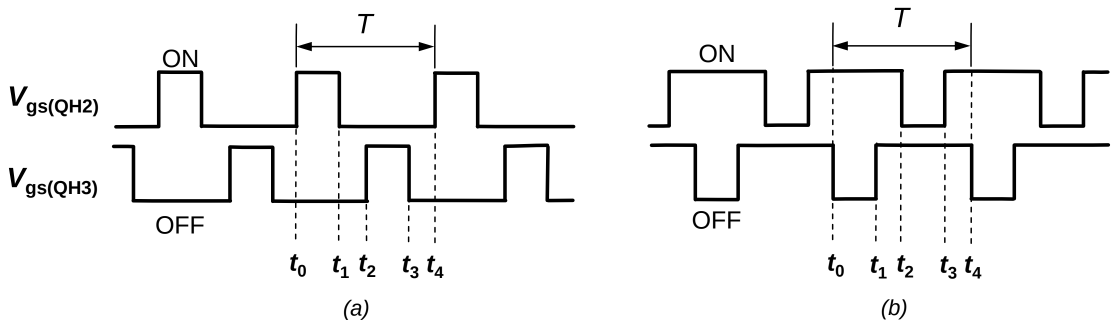


Figure 4. Timing charts for Q_{H2} and Q_{H3}
(a) $d < 0.5$ (b) $d \geq 0.5$

Figure 4 shows the timing charts for Q_{H2} and Q_{H3}. Gate-source voltages $V_{gs(QH2)}$ and $V_{gs(QH3)}$ indicate the ON and OFF states, and t_j (j = 0 to 4) indicates the time when the transistor is switched. As shown in Figure 4, Q_{H2} and Q_{H3} can be simultaneously OFF when (a) $d < 0.5$, while they cannot be simultaneously OFF if (b) $d \geq 0.5$. Therefore, it is necessary to analyze the circuit operations separately for (a) $d < 0.5$ and (b) $d \geq 0.5$.

(a) If $d < 0.5$, the time sequence of terms 1, 2, 3, and 4 are defined as follows.

Term 1 (from t_0 to t_1): Q_{H2} is turned ON at t_0, and Q_{H3} remains OFF
Term 2 (from t_1 to t_2): Q_{H2} is turned OFF at t_1, and Q_{H3} remains OFF
Term 3 (from t_2 to t_3): Q_{H2} remains OFF, and Q_{H3} is turned ON at t_2
Term 4 (from t_3 to t_4): Q_{H2} remains OFF, and Q_{H3} is turned OFF at t_3

Since one cycle is time T, terms 1 and 3 are d * T, and terms 2 and 4 are (0.5 - d) * T.

(b) If $d \geq 0.5$, the sequence is similarly defined as follows.

Term 1 (from t_0 to t_1): Q_{H2} remains ON, and Q_{H3} is turned OFF at t_0
Term 2 (from t_1 to t_2): Q_{H2} remains ON, and Q_{H3} is turned ON at t_1
Term 3 (from t_2 to t_3): Q_{H2} is turned OFF at t_2, and Q_{H3} remains ON
Term 4 (from t_3 to t_4): Q_{H2} is turned ON at t_3, and Q_{H3} remains ON

Therefore, terms 1 and 3 are (1 - d) * T, and terms 2 and 4 are (d - 0.5) * T.

For both cases where (a) $d < 0.5$ or (b) $d \geq 0.5$, Q_{L2} and Q_{L3} are switched mutually with Q_{H2} and Q_{H3}, respectively, leading to the following relational expressions.

$$V_1 = -V_2 \qquad (2)$$
$$i_{L1} = i_m + i_1 \qquad (3)$$
$$i_{L2} = i_2 \qquad (4)$$
$$i_1 = i_2 \qquad (5)$$

From Equations (2) to (5), i_m and its ripple component Δi_m are calculated as follows.

$$i_m = i_{L1} - i_{L2} \qquad (6)$$
$$\Delta i_m = \Delta i_{L1} - \Delta i_{L2} \qquad (7)$$

From the basic formulas for induced electromotive force of $V = -L\mathrm{d}i/\mathrm{d}t$, the formulas for Δi_{L1} and Δi_{L2} are derived as shown in Table 1. As shown in Equations (8) to (9), the sum of i_{L1} and i_{L2} equals output current I_{out}, and the sum of Δi_{L1} and Δi_{L2} equals output current ripple I_{out_pp}.

$$I_{out} = i_{L1} + i_{L2} \qquad (8)$$
$$I_{out\_pp} = \Delta i_{L1} + \Delta i_{L2} \qquad (9)$$

Table 1. Δi_{L1} and Δi_{L2} for each term (1 to 4)

(a) $d < 0.5$

Term	Δi_{L1}	Δi_{L2}
1	$\frac{dV_{\mathrm{in}}}{L}\left(1-\frac{L_m}{L+2L_{\mathrm{m}}}-d\right)T$	$\frac{dV_{\mathrm{in}}}{L}\left(\frac{L_m}{L+2L_{\mathrm{m}}}-d\right)T$
2	$-\frac{(0.5-d)dV_{\mathrm{in}}}{L}T$	$-\frac{(0.5-d)dV_{\mathrm{in}}}{L}T$
3	$\frac{dV_{\mathrm{in}}}{L}\left(\frac{L_m}{L+2L_m}-d\right)T$	$\frac{dV_{\mathrm{in}}}{L}\left(1-\frac{L_m}{L+2L_m}-d\right)T$
4	$-\frac{(0.5-d)dV_{\mathrm{in}}}{L}T$	$-\frac{(0.5-d)dV_{\mathrm{in}}}{L}T$

(b) $d \geq 0.5$

Term	Δi_{L1}	Δi_{L2}
1	$\frac{(1-d)V_{\mathrm{in}}}{L}\left(1-\frac{L_m}{L+2L_m}-d\right)T$	$\frac{(1-d)V_{\mathrm{in}}}{L}\left(\frac{L_m}{L+2L_m}-d\right)T$
2	$\frac{(d-0.5)(1-d)V_{\mathrm{in}}}{L}T$	$\frac{(d-0.5)(1-d)V_{\mathrm{in}}}{L}T$
3	$\frac{(1-d)V_{\mathrm{in}}}{L}\left(\frac{L_m}{L+2L_m}-d\right)T$	$\frac{(1-d)V_{\mathrm{in}}}{L}\left(1-\frac{L_m}{L+2L_m}-d\right)T$
4	$\frac{(d-0.5)(1-d)V_{\mathrm{in}}}{L}T$	$\frac{(d-0.5)(1-d)V_{\mathrm{in}}}{L}T$

Advantages of trans-linked topology

The trans-linked topology can significantly reduce the copper loss of the reactor by using the coupling reactor connected with the output lines. The reasons are as follows. (*2)~(*3)

- Since the output current is divided into two phases, the loss due to Joule heating is reduced by 50%
- The inductance required for smoothing can be reduced

One cycle of the current ripple in the reactor is reduced by a factor of 2 with the trans-linked part, which is designed to be operated in the reverse phase so that the current is divided into two. In addition, these reverse currents alternately magnetize the coupling reactor and prevent magnetic saturation. Therefore, materials with a high saturation magnetic flux density (B_S) are not required and materials with a high magnetic permeability (low B_S), such as ferrite, can be used. As a result, the number of windings (N) of the reactor is reduced, resulting in the reduction of the copper loss.

Design of coupling reactor

As shown in Figure 5, the coupling reactor is composed of two magnetic elements referred to as the “outer leg” and the “center leg”. Since the reactor is a reverse polarity transformer, the magnetic fluxes produced by i_{L1} and i_{L2} are canceled out by each other in the outer leg. This means that it is not necessary for the magnetic material of the outer leg to have a high B_S.

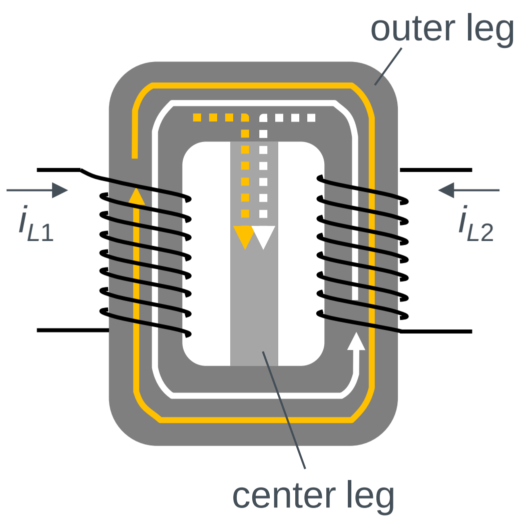


Figure 5. Schematic diagram of coupling reactor

In contrast, the magnetic fluxes flow in the same direction and are intensified in the center leg. At the same time, since the phases of i_{L1} and i_{L2} are shifted relative to each other by 180°, the vibration frequency of the total magnetic flux is doubled. Therefore, it is necessary for the magnetic material used for the center leg to have a high B_S and good characteristics for high frequency operation. Accordingly, ferrite MB3 [JFE FERRITE (*8)] is employed for the outer leg material, and Liqualloy™ [ALPS ELECTRIC (*9), (*10): currently ALPS ALPINE] is employed for the center leg.

The most important factors to be considered in designing the coupling reactor are L and L_m. These two parameters determine the ripple waveform of I_{out} and the magnetic flux density. As explained in detail below, the maximum value of $|I_{out\_pp}|$ is determined by L. From Table 1 and Equation (9), $|I_{out\_pp}|$ for each term is expressed as Equation (10).

$$|I_{out\_pp}| = \begin{cases} \dfrac{d(1-2d)V_{\mathrm{in}}T}{L} & (for\ d < 0.5) \\ \dfrac{(1-d)(2d-1)V_{\mathrm{in}}T}{L} & (for\ d \geq 0.5) \end{cases} \tag{10}$$

At d = 0.25 and 0.75, $|I_{out\_pp}|$ reaches its maximum and the value of $|I_{out\_pp}|_{max}$ is expressed as Equation (11).

$$|I_{out\_pp}|_{max} = \frac{V_{\mathrm{in}}T}{8L} \tag{11}$$

From Table 1, Δi_m for terms 1 and 3 is expressed as follows based on Equation (7).

$$\Delta i_m = \begin{cases} \pm\dfrac{dV_{\mathrm{in}}T}{L+2L_m} & (for\ d < 0.5) \\ \pm\dfrac{(1-d)V_{\mathrm{in}}T}{L+2L_m} & (for\ d \geq 0.5) \end{cases} \tag{12}$$

Δi_m is positive for term 1, negative for term 3, and 0 for terms 2 and 4. Since the circuit configuration is symmetric, the average values of i_{L1} and i_{L2} over one cycle T are $I_{out}/2$ as calculated with Equation (8). As a result, the average value of i_m expressed with

Equation (6) must be zero. This result and Equation (12) lead to the following equation for d < 0.5.

$$\begin{cases} i_{m1} - i_{m0} = \frac{dV_{\mathrm{in}}T}{L+2L_m} \\ i_{m2} - i_{m1} = 0 \\ i_{m3} - i_{m2} = -\frac{dV_{\mathrm{in}}T}{L+2L_m} \\ i_{m4} - i_{m3} = 0 \\ \frac{i_{m0}+i_{m1}}{2}d + i_{m1}(0.5-d) + \frac{i_{m2}+i_{m3}}{2}d + i_{m3}(0.5-d) = 0 \end{cases} \tag{13}$$

i_{mj} (j = 0 to 4) represents i_m at t_j. In the fifth equation in (13), the left term represents the average value of i_m. From Equation (13), i_{mj} can be calculated as follows.

$$\begin{cases} i_{m0} = i_{m3} = i_{m4} = -\frac{dV_{\mathrm{in}}T}{2(L+2L_m)} \\ i_{m1} = i_{m2} = \frac{dV_{\mathrm{in}}T}{2(L+2L_m)} \end{cases} \tag{14}$$

The same calculation method shows i_{mj} for $d \geq 0.5$ as well.

$$\begin{cases} i_{m0} = i_{m3} = i_{m4} = -\frac{(1-d)V_{\mathrm{in}}T}{2(L+2L_m)} \\ i_{m1} = i_{m2} = \frac{(1-d)V_{\mathrm{in}}T}{2(L+2L_m)} \end{cases} \tag{15}$$

Therefore, $|i_m|_{max}$, the maximum value of $|i_m|$, is expressed as follows at d = 0.5.

$$|i_m|_{max} = \frac{V_{\mathrm{in}}T}{4(L+2L_m)} \tag{16}$$

In addition, magnetic flux density B_m of the outer leg can be calculated as follows.

$$B_m = \frac{i_m L_m}{NA_e} \tag{17}$$

A_e represents the effective area of the ferrite core of the outer leg.

Input and output specifications of inverter

The input and output specifications of the inverter designed here are shown below.

- V_{in} = 320 V
- V_{out} = AC 200 V
- I_{out} = AC 25A
- f_{sw} = 40 kHz
- $I_{out\ pp}/I_{out\ peak}$ < 0.2
- $B_{m\ max}$ < 0.15 T

$I_{out\ pp}/I_{out\ peak}$ is the setting for reducing the C_o loss. $B_{m\ max}$ is the condition for avoiding the risk of magnetic saturation [approximately less than a third of B_S of MB3 (*8)].

From Equation (11) and the relationship between $I_{out\ pp}/I_{out\ peak}$ and L, it is necessary for L to exceed 100√2 μH. For this core, L = 170 μH when N = 19. This design employs 2.2 mH for L_m and 378 mm^2 for A_e of the outer leg. From Equations (16) and (17), it can also be seen that these parameters satisfy $B_{m\ max}$ < 0.15 T.

Figure 6 shows the appearance of the coupling reactor containing a copper winding made with 40 litz wires of 0.35 mm in diameter. The measured resistance of the copper wire was 18mΩ. A ferrite core with magnetic flux density B_S of 0.45 T and permeability of 2,500 is employed (*8) to reduce the copper wire resistance by reducing the number of windings N. A material with a high B_S is essential for the center leg. Liqualloy™ (*9) is suitable for the center leg material, achieving a gapless configuration thanks to its high B_S value of 1.3 T.

Table 2 Δi_{L1} and Δi_{L2} for each term (1 to 4)

	Trans-linked interleaved type	Full bridge type
Dimensions	6.5 cm x 4.8 cm x 6.2 cm	φ8 cm × L4 cm × 4 in series
Volume	193 cm^3	905 cm^3
Volume ratio	1	4.68

(a) Trans-linked type reactor (b) Conventional reactor

Figure 6. Developed coupling reactor and conventional reactor

Efficiency evaluation

The performance is compared for a trans-linked interleaved inverter using SiC MOSFET (inverter A), conventional full bridge inverter using Si IGBT (inverter B), and conventional full bridge inverter using SiC MOSFET (inverter C).

Figure 7 shows the circuit diagram of inverters B and C. Table 3 shows the circuit constants of these two types of inverters.

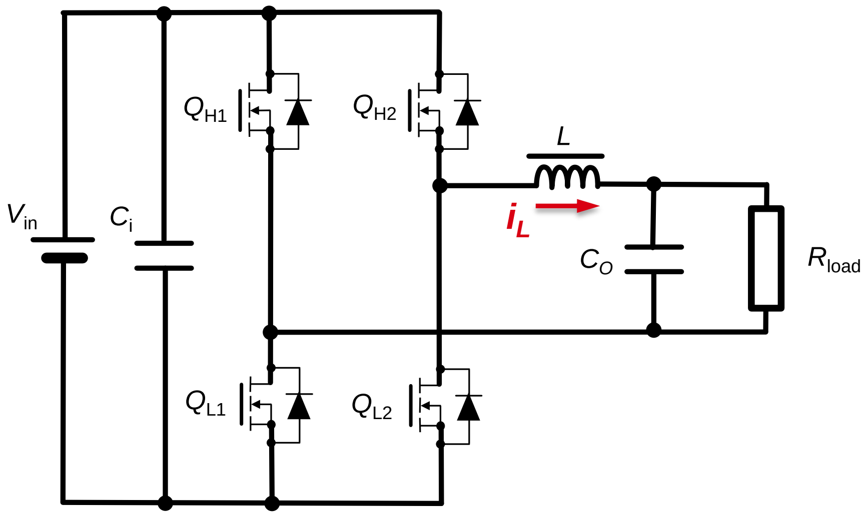


Figure 7. Block diagram of conventional inverter circuit (inverters B, C)

In this figure, i_L represents the current flowing through the smoothing reactor in inverters B and C. As shown in Table 3, the trans-linked type can reduce the necessary capacitance value by reducing the current passing through the MOSFET by a factor of 2 and increasing the frequency of the current ripple. As a result, the number of transistors and capacitors can be reduced.

Table 3 Constants of parts used for inverter circuits

	Inverter A	Inverter B	Inverter C
Input voltage (V_{in})	DC 320 V		
Input capacitance (C_i)	560 μF × 3	560 μF × 4	
Low frequency switches	SiC MOSFET (SCT3017AL)	-	
High frequency switches	SiC MOSFET (SCT3030AL)	Si IGBT × 2pcs/arm (STGW60H65DFB)	SiC MOSFET × 2pcs/arm (SCT3030AL)
Switching frequency (f_{sw})	40 kHz	20 kHz	
Free wheeling diode (D)	SiC SBD (SCS212AM)	-	
Magnetizing inductance (L_m)	2.2 mH	-	
Leakage / Smoothing inductance (L)	170 μH	300 μH × 4 (BCH61-35150)	
Copper wire resistance of the reactor	18 mΩ	20 mΩ × 4	
Output capacitance (C_o)	1 μF × 4	1 μF × 8	
Output voltage (V_{out})	AC 200 V		

Figure 8 shows efficiency η of inverters A, B, and C taking output power P_{out} as the horizontal axis. In this figure, efficiency η is calculated as a ratio of P_{out} against input power P_{in}. However, the total power loss ($P_{total} = P_{in} - P_{out}$) does not include the gate drive loss in the MOSFET.

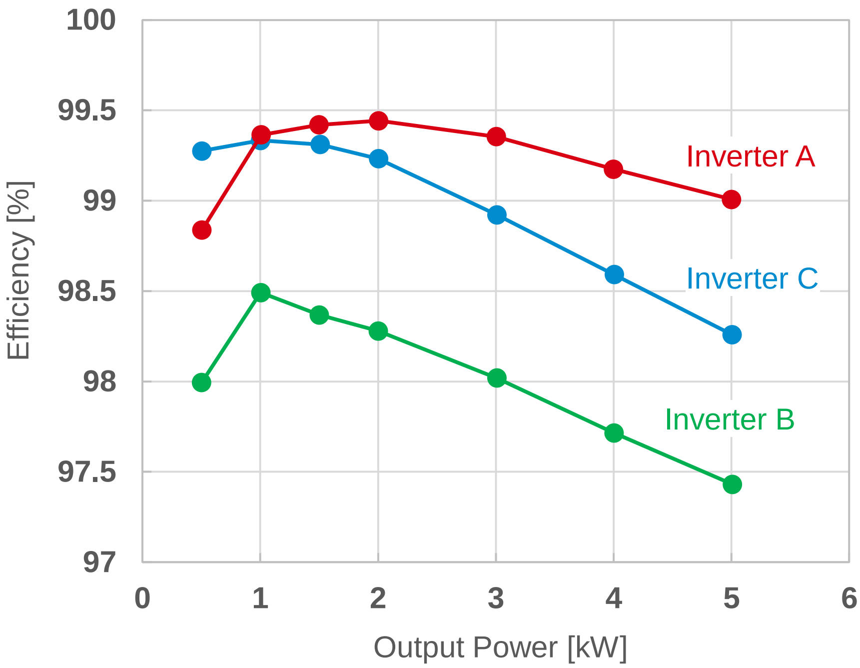


Figure 8. Efficiency of inverters A, B, and C taking Pout as indicator

If the Si IGBT is replaced with a SiC MOSFET (from inverter B to inverter C), efficiency η is improved over the entire range of P_{out}. However, efficiency η is monotonically decreased in the P_{out} range above 1 kW, and falls below 99% in the P_{out} range above 3 kW mainly due to increase in the conduction loss in the transistor and the copper loss in the wiring. In contrast, efficiency η of inverter A exceeds 99% in the entire P_{out} range from 1 kW to 5 kW, reaching a high efficiency of 99.4% at 2 kW.

Analysis of Total Loss Power (P_{total})

The pie chart in Figure 9 shows a breakdown of the total loss power (P_{total}) of inverter A (trans-linked type) when the inverter is operated at P_{out} = 5 kW. This loss analysis calculation is based on the on-resistance (R_{ON}) at 125°C. The details are explained below.

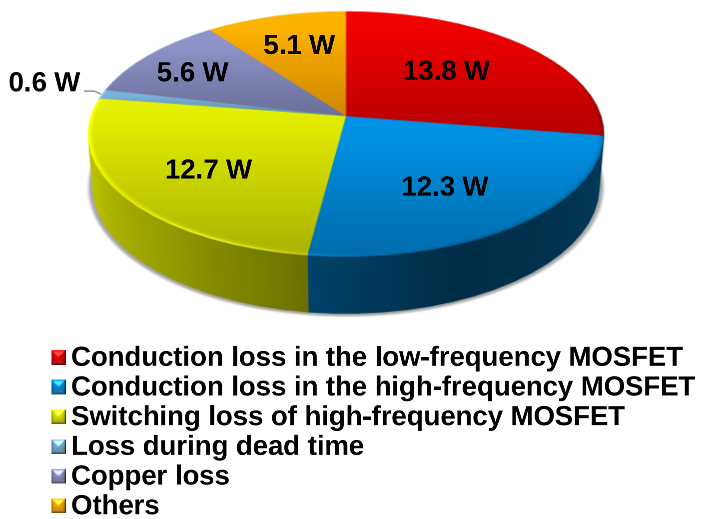


Figure 9. Analysis of P_{total} in inverter A at 5 kW

1) Conduction loss in MOSFET of half bridge B1:

Each MOSFET of B1 (SCT3017AL, ROHM) has R_{ON} of 22mΩ at 125°C. The effective current is 25 Arms and the total conduction loss in these MOSFET is (25 Arms)^2 * 22mΩ = 13.8 W. Since f_{SW} of B1 is 50 Hz, the dead time loss and switching loss E_{loss_SW} in these MOSFET are negligible.

2) Conduction loss in MOSFET of half bridges B2 and B3 (PWM part):

Each MOSFET in B2 and B3 (SCT3030AL, ROHM) has R_{ON} of 40mΩ at 125°C. The effective current flowing in each phase of the coupling reactor is 12.5 Arms. Since the high side MOSFET (Q_{H2} and Q_{H3}) and the low side MOSFET (Q_{L2} and Q_{L3}) are operated with synchronous rectification, either of the high or low side MOSFET remain ON except for the dead time (DT) of 220 ns. Since one cycle of the MOSFET is 25 µs, the conduction loss in the MOSFET of the PWM parts is (12.5 Arms)^2 * 40mΩ * (1 - (220 ns * 2)/25 µs) * 2 phases = 12.3 W.

3) Switching loss in MOSFET of half bridges B2 and B3 (PWM part):

Figure 10 shows the E_{loss_SW} curve of the SiC MOSFET used in the PWM part as a function of drain current I_d.

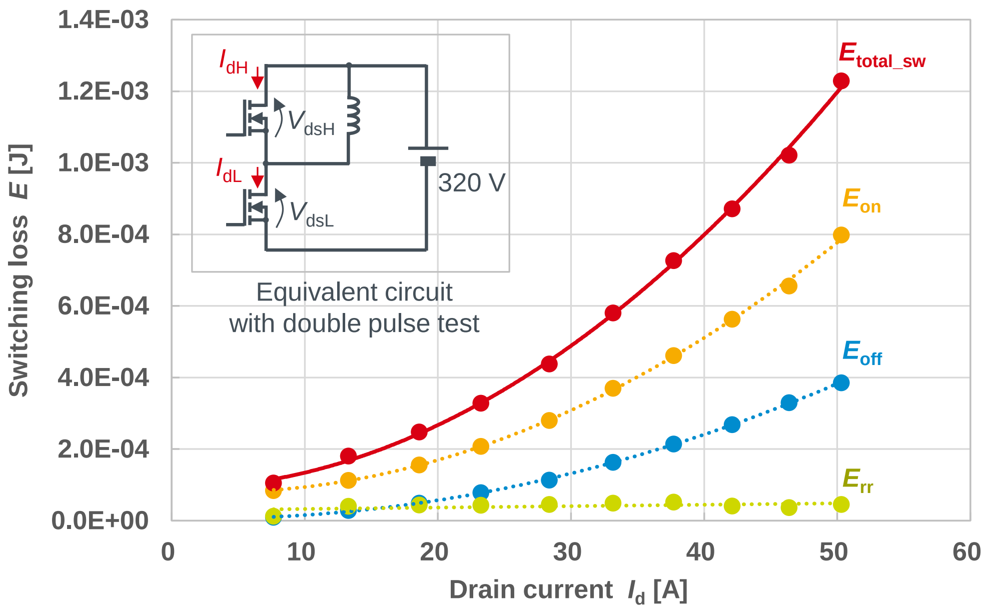


Figure 10. E_{total_sw}, E_{on}, E_{off}, and E_{rr} of SCT3030AL and circuit for double pulse test

The total energy of switching loss in MOSFET (E_{total_SW}) is mainly composed of the energy of turn ON loss (E_{on}), energy of turn OFF loss (E_{off}), and energy of reverse recovery loss (E_{rr}). These loss energies were measured with the double pulse test (*11), and the measurement circuit used for this test is shown as an inset in Figure 10. V_{dsH} and I_{dH} represent the drain-source voltage and the drain current of the high side MOSFET, respectively, while V_{dsL} and I_{dL} represent the corresponding values for the low side. E_{on} and E_{off} can be calculated by multiplying V_{dsL} and I_{dL} during the switching transient periods for turning ON and OFF the low side MOSFET, respectively. E_{rr} can be calculated from V_{dsH} and I_{dH} during the switching transient period for turning ON the low side MOSFET. The average current flowing through L_1 or L_2 at the point of phase angle θ is expressed as Equation (20). Therefore, the average P_{sw} of the MOSFET in the PWM part is the integrated value of E_{total_sw} * f_{sw} over the entire period, and the integration can be calculated with averaging Equation (21).

$$I = \sqrt{2} \cdot 12.5 \cdot \sin\theta \qquad (A) \qquad (20)$$

$$P_{SW} = \frac{1}{T}\int_0^T E_{total\_sw}\, f_{sw} dt \cdot 2phase = \ 12.7W \qquad (21)$$

4) Power loss during DT period:

For inverter A, DT is set to 220 ns. During this period, the current flows into the free wheeling SBD (SCS212AM, ROHM). The average current flowing through the diode can also be expressed with Equation (20). As with P_{sw}, the power loss during the DT period (P_{DT}) is calculated according to the following equation.

$$P_{DT} = \frac{1}{T}\int_{0}^{T} V_F\, I_F f_{sw} \cdot 2DT dt \cdot 2pcs. \qquad (22)$$

V_F and I_F represent the forward voltage and current of the SBD, respectively. Calculation based on the V_F-I_F characteristics on the data sheet of SCS212AM used (*12) results in P_{DT} = 0.3 W * 2 pcs = 0.6 W.

5) Copper loss:

The measured resistance was 18mΩ for the copper wire wound around one side of the outer leg. Since the effective current is 12.5 Arms, the total copper loss is $(12.5\ \text{Arms})^2$ * 18mΩ * 2 wires = 5.6 W.

6) Others:

The power losses other than those described above are approximately 5.1 W, including the core loss in the coupling reactor, C_i, C_o, and the conduction loss in the wiring parts of the circuit board. From the core loss data for ferrite MB3 (*8) and Liqualloy™ (*9), the total power loss in this inverter core is calculated to be approximately 2.5 W.

From these loss analyses, the sum of power losses in Q_{H2}, Q_{H3}, Q_{L2}, and Q_{L3} is approximately 25 W.

Since this loss is small, the cooling system can be simplified. In inverter A, a heat sink with a thermal resistance (R_{th}) of 5°C/W is attached to all SiC MOSFET via a thermal sheet with R_{th} of 1.7°C/W. It is estimated that the fin temperature on the contact surface of the SiC MOSFET is low (approximately 80°C) and the junction temperature (T_j) is lower than 130°C. Since this level is lower than the maximum rating for T_j of the SiC MOSFET, the fan-less cooling is feasible.

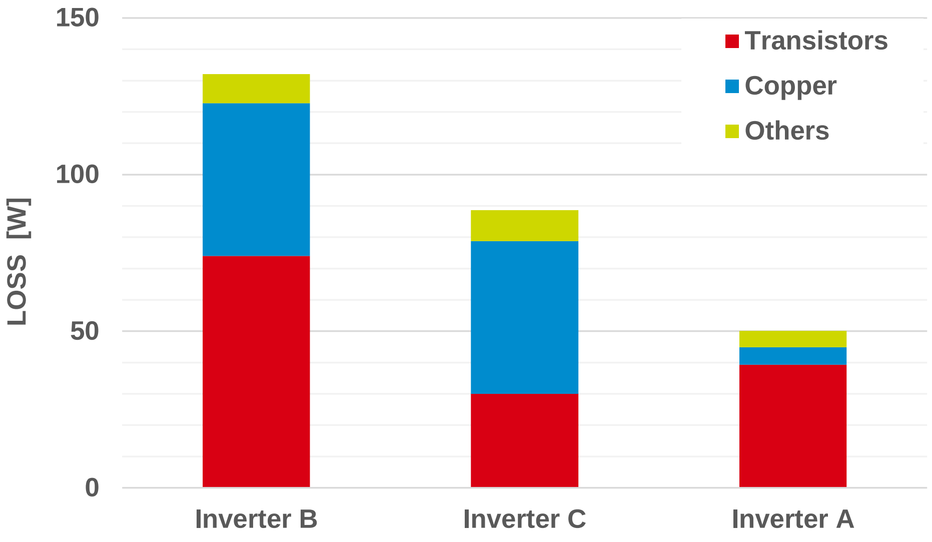


Figure 11. Comparison of breakdown of P_{total} of inverters at 5 kW

For P_{total} of inverters B and C at 5 kW, breakdowns are calculated with a similar method. The breakdowns of P_{total} of inverters A, B, and C are compared in Figure 11. The loss in the transistors is reduced by a factor of 2 or greater by replacing the Si IGBT with the SiC MOSFET, making fan-less operations feasible even for inverter C. Since the actual surface temperature of the cooling fins was also 80°C for inverter C operated at 5 kW, the fan-less operations were feasible. However, due to the copper loss in the smoothing reactor, efficiency η of 99% at 5 kW cannot be achieved for inverter C. The copper loss in the coupling reactor is significantly smaller for inverter A compared with inverter C. The reason is that the coupling reactor reduces the number of windings, effectively reducing the copper loss.

Table 4 summarizes the performances of inverters A, B, and C. If inverter A is employed instead of inverter B, efficiency η is improved by 1.6%, P_{total} is reduced by 62%, and the size and the weight are reduced by 56% and 50%, respectively. In addition, compared with inverter C, efficiency η of inverter A is 0.7% better and P_{total} is also improved by 41%. The differences between inverter A and inverter B or C are also evident in Figure 1.

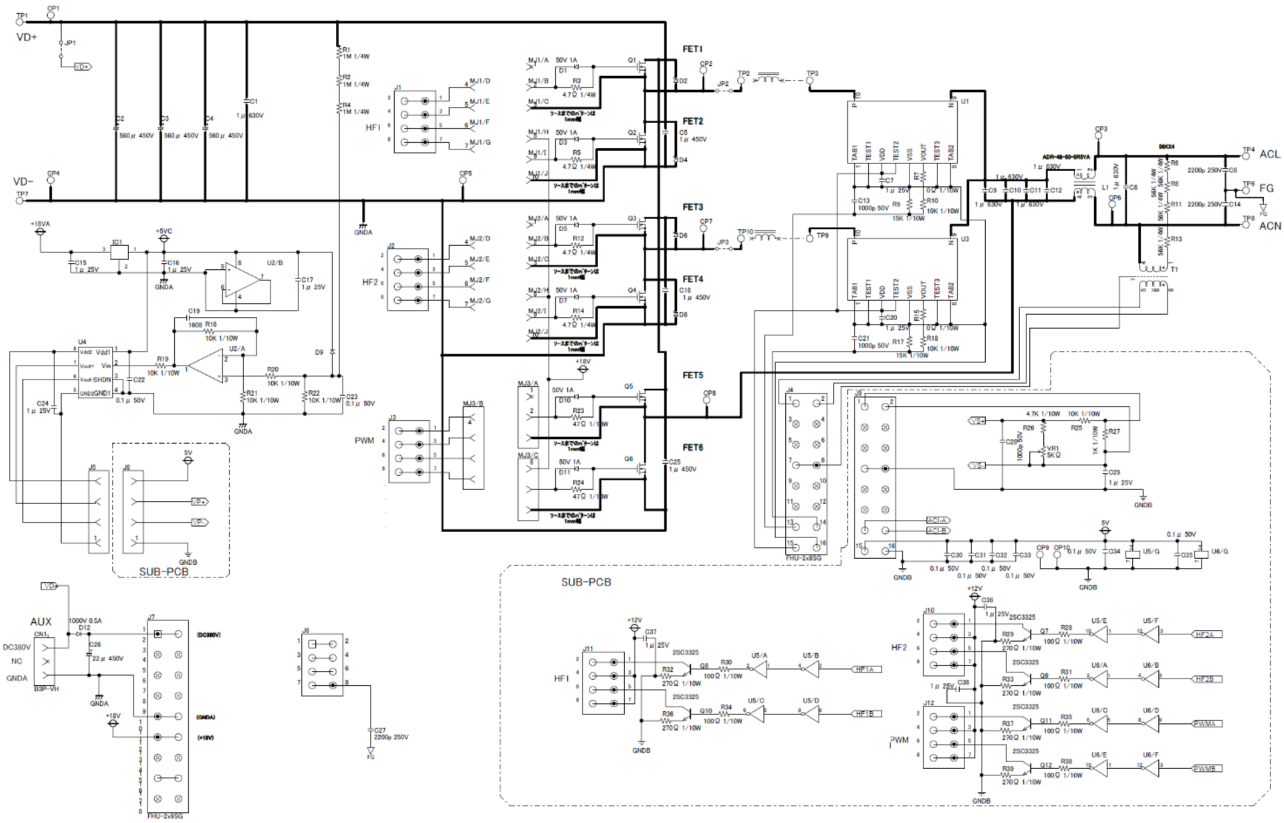
Table 4 Comparison of performance of inverter circuits

	Inverter A	Inverter B	Inverter C
Switching transistors	SiC MOSFETs	Si IGBTs	SiC MOSFETs
Conversion efficiency (@5 kW)	99.0%	97.4%	98.3%
Total loss (@5 kW)	51 W	133 W	85 W
Size	4180 cm^3	9480 cm^3	
Weight	2.5 kg	5.0 kg	

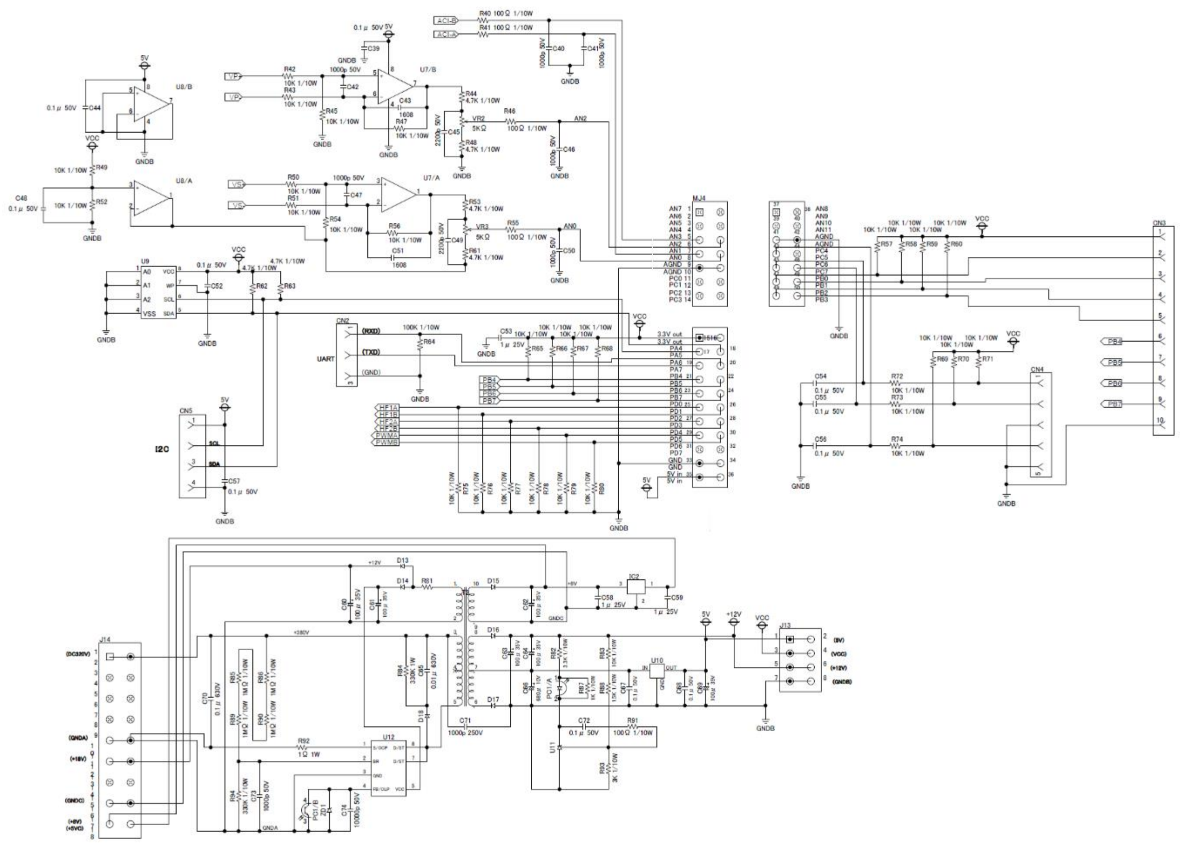
Summary

We developed trans-linked interleaved 5 kW inverters that use SiC MOSFET as switching devices. The SiC MOSFET show an excellent switching performance compared with that of Si IGBT. This enables higher switching operations and downsizing of the entire system. Furthermore, when the trans-linked interleaved circuit topology that employs a reverse polarity coupling reactor is operated at a switching frequency of 40 kHz, the number of windings is reduced, leading to a significant reduction in the copper loss. As a result, a high efficiency of 99.0% at an output power of 5 kW is achieved, enabling fan-less operations.

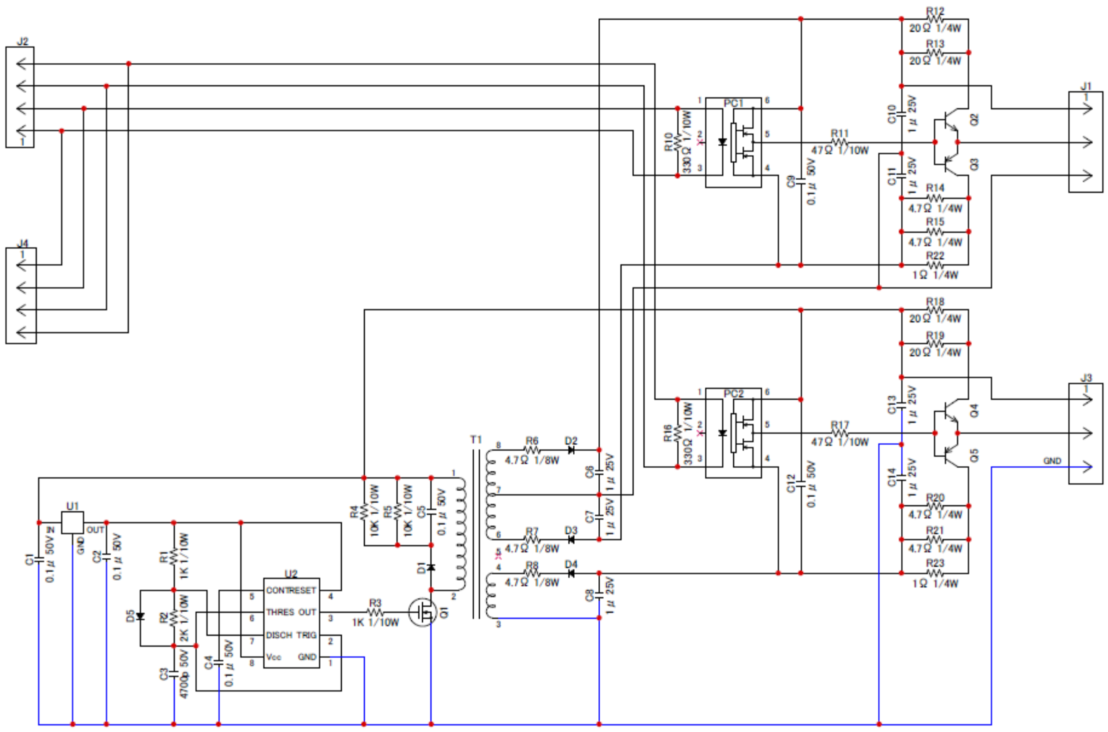
■ Inverter A circuit diagram (Schematics)



(a) Power PCB and Sub PCB



(b) Control PCB


J2
J4
J1
J3
PC1
PC2
U1
U2
T1
Q1
Q2
Q3
Q4
Q5
GND
CONT RESET
THRES OUT
DISCH TRIG
Vcc GND

(c) driver PCB

■ Inverter A parts list (BOM List)

(a),(b) Power PCB, Sub PCB, Control PCB(Continued)

Device	Symbol	Parts Number	Values	Manufacture	Package Size [mm]
Film Capacitor	C1,C8,C9,C10,C11,C12	BFC233920105	1μF, 630V ±20%	Vishay	26x10x19.5
Al-E Capacitor	C2,C3,C4	ELXS451VSN561MA50S	560μF, 450V ±20%	Nippon chemi-con	D35x50
Film Capacitor	C5,C18,C25	450MPH105J	1μF, 450V ±5%	RUBYCON	18.5x15x23
Capacitor	C6,C14,C27	DE1E3KX222MA4BN01	2200pF, 250Vac±20%	MURATA	9x7x12
Capacitor	C7,C20,C29,C36,C37,C38	GRM188R71E105KA12	1μF, 25V ±10%	MURATA	1608
Capacitor	C15,C16,C17,C24,C53,C58,C59	GRM185B31E105MA12	1μF, 25V ±20%	MURATA	1608
Capacitor	C13,C21,C28,C40,C41,C42, C46,C47,C50,C73,	GRM188B11H102KA01	1000pF, 50V ±10%	MURATA	1608
Capacitor	C22, C30,C31,C32,C33, C34,C35,C39,C44,C48,C52, C54,C55,C56,C57	GRM188B31H104KA92	0.1μF, 50V ±10%	MURATA	1608
Capacitor	C67,C68,C72	GRM188R71E104KA01	0.1μF, 25V ±10%	MURATA	1608
Capacitor	C23	GRM188R11H104KA93	0.1μF, 50V ±10%	MURATA	1608
AL-E Capacitor	C26	UCS2W220MHD	22μF, 450V ±20%	Nichicon	D16x20
Capacitor	C45,C49	GRM1851X1H222JA44	2200pF, 50V ±5%	MURATA	1608
Capacitor	C19,C43,C51	TBD	TBD	MURATA	1608
AL-E Capacitor	C60,C61,C62,C63,C64,C69	ELXZ350ELL101MF15D	100μF, 35V ±20%	Nippon chemi-con	D6.3x15
AL-E Capacitor	C66	ELXZ100ELL681MF15D	680μF, 10V ±20%	Nippon chemi-con	D8x11.5
Film Capacitor	C65	ECQE6103KF	0.01μF, 630V ±10%	Panasonic	12x4.5x7.5
Film Capacitor	C70	ECQE6104KF	0.1μF, 630V ±10%	Panasonic	18.5x6.3x14
Capacitor	C71	DE1E3KX102MA4BN01	1000pF, 250Vac ±20%	MURATA	6x4x9
Capacitor	C74	GRM188B11H103KA01	10000pF, 50V ±10%	MURATA	1608
Diode	D1,D3,D5,D7,D10,D11	ES1A	50V,1A	Fairchild	DO-214AC
Diode	D2,D4,D6,D8	SCS212AM	650V 12A	ROHM	10.16x4.7x19
Diode	D9	1SS355	90V 225mA	ROHM	2.5x1.25x0.7
Diode	D12,D18	EG01C	1000V, 0.5A	SANKEN	φ2.7x5L
Diode	D13,D14,D15,D16,D17	SBR1U150SA-13	150V, 1A	DIODES	4.3x2.6x2.2
Zener Diode	ZD1	UDZS5.1B	5.1V, 5mA	ROHM	SC-90
Photocoupler	PC1	PS2501L-1	1ch, 80V,50mA	NEC	6.5x4.6x3.6
Transistor	Q1,Q2,Q3,Q4	SCT3030AL	Nch, 650V, 30mΩ	ROHM	TO-247N
Transistor	Q5,Q6	SCT3017AL	Nch, 650V, 17mΩ	ROHM	TO-247N
Transistor	Q7,Q8,Q9,Q110,Q11,Q12	2SC3325	50V,0.5A	TOSHIBA	SC-59
Potemtiometer	VR1,VR2,VR3	CT-6E-P5KΩ	5kΩ, 1/2W ±1%	COPAL	7x7x.8
Resistor	R1,R2,R4	RK73B2BTTD105J	1MΩ, 1/4W ±5%	KOA	3216
Resistor	R85,R86,R89,R90	MCR10EZPJ105	1MΩ, 1/10W ±5%	ROHM	1608
Resistor	R3,R5,R12,R14	RK73B2BTTD4R7J	4.7Ω, 1/4W ±5%	KOA	3216
Resistor	R6,R8,R11,R13	RK73B2BTTD563J	56kΩ, 1/4W ±5%	KOA	3216
Resistor	R7,R15	RK73B1JTTD000J	0Ω	KOA	1608
Resistor	R9,R17	RK73B1JTTD153J	15kΩ, 1/10W ±5%	KOA	1608
Resistor	R10,R16,R18,R19,R20,R21, R22,R25,R42,R43,R45,R47, R49,R50,R51,R52,R54,R56, R57,R58,R59,R60,R65,R66,R67, R68,R69,R70,R71,R72,R73,'74, R75,R76,R77,R78,R79,R80	RK73B1JTTD103J	10kΩ, 1/10W ±5%	KOA	1608
Resistor	R23,R24	RK73B1JTTD470J	47Ω, 1/10W ±5%	KOA	1608
Resistor	R26,R44,R48,R53,R61,R62,R63	RK73B1JTTD472J	4.7kΩ, 1/10W ±5%	KOA	1608
Resistor	R27	RK73B1JTTD102J	1kΩ, 1/10W ±5%	KOA	1608
Resistor	R28,R30,R31,R34,R35,R38, R40,R41,R46,R55	RK73B1JTTD101J	100Ω, 1/10W ±5%	KOA	1608
Resistor	R29,R32,R33,R36,R37,R39	RK73B1JTTD271J	270Ω, 1/10W ±5%	KOA	1608
Resistor	R64	RK73B1JTTD104J	100kΩ, 1/10W ±5%	KOA	1608
Resistor	R82	MCR03EZPJ332	3.3kΩ, 1/10W ±5%	ROHM	1608
Resistor	R93	MCR03ERTJ302	3kΩ, 1/10W ±5%	ROHM	1608
Resistor	R88	MCR03EZPJ152	1.5kΩ, 1/10W ±5%	ROHM	1608
Resistor	R81,R92	MOSX1C1R0J	1Ω, 1W ±1%	KOA	φ3x9L
Resistor	R84	MOSX1C334J	330kΩ, 1W ±5%	KOA	φ3x9L
Resistor	R83	MCR03EZPJ103	10kΩ, 1/10W ±5%	ROHM	1608
Resistor	R87	MCR03EZPJ102	1kΩ, 1/10W ±5%	ROHM	1608
Resistor	R91	MCR03EZPJ101	100Ω, 1/10W ±5%	ROHM	1608
Resistor	R94	MCR03EZPJ334	330kΩ, 1/10W ±5%	ROHM	1608
Transformer	T1	VDCT	6mA, 67:1	NIHON PULSE	24.5x21x22
Transformer	T2	TR10P	--	PAT	---
Line filter	L1	ADR-48-50-0R5YA	0.5mH, 50A	UENO	65x60x40
Current Sensor	U1,U3	CQ-3303	±20A 60mV/A	AsahiKASEI	7.9x5.6x1.3
IC	U2,U7,U8	NJM2732M	Dual RtoR OP-amp	NJRC	SOP-8
IC	U4	ACPL-C87AT	Isolation AMP	AVAGO	5.85x6.8x3.2
IC	U5,U6	TC4069UBF	6 CMOS Inverter	TOSHIBA	DIP-14
IC	IC1,IC2	NJM78L05UA	5V 500mA	NJRC	SOT-89
IC	U9	24LC64SN	EEPROM	MICROCHIP	SOP-8
IC	U10	TA48M05F	5V, 0.5A LDO	TOSHIBA	6.5x9.5x2.3
IC	U11	NJM431U	150mA Shunt regulator	NJRC	SOT-89
IC	U12	STR-A6079M	Flybuck controller 800V, 1.2A	SANKEN	DIP-8

(a),(b) Power PCB, Sub PCB, Control PCB(Continued)

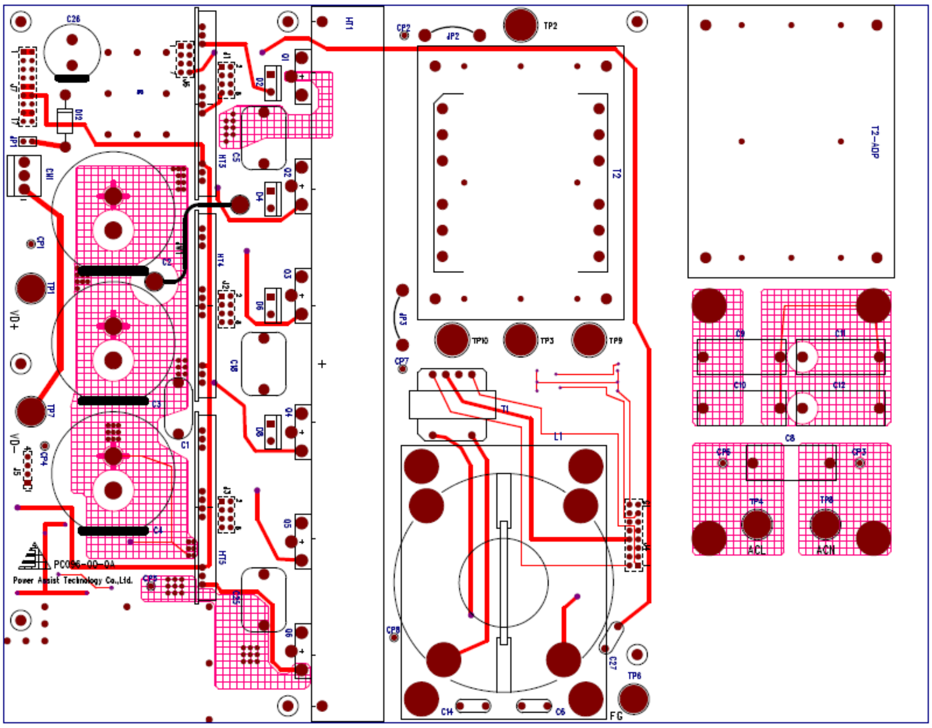
Device	Symbol	Parts Number	Values	Manufacture	Package Size [mm]
Connector	J1,J2,J3,J6,J10,J11,J12	FHU-2×4SG	3A, 8pin,female	Useconn	10.16x5.08x8.5
Connector	J4	FHU-2x8SG	3A, 16pin, female	Useconn	20.8x5x8.5
Connector	J5,J8	PH-1x04SG	Pin header 1x4P	Useconn	10.16x2.54x8.5
Connector	J7	FHU-2x9SG	3A, 18pin, female	Useconn	23.4x5x8.5
Connector	J9	PH-2x08SG	Pin header 2x8P	Useconn	20.8x5x8.5
Connector	J13	PH-2x04SG	Pin header 2x4P	Useconn	10.16x5.08x8.5
Connector	J14	PH-2x09SG	Pin header 2x9P	Useconn	22.86x5.08x8.5
Connector	CN1	B3P-VH	10A, 3pin	JST	13.8x9.7x11
Connector	CN2	S3B-EH	3A, 3pin	JST	10x3.8x6
Connector	CN3	PH-1x10RG2	10pin, Side	Useconn	25.4x10.61x2.54
Connector	CN4	B5B-PH-K-S	5pin	JST	11.9x4.5x6
Connector	CN5	S4B-EH	4pin	JST	12.5x3.8x6
FET-2 Module	MJ1,MJ2	PC092-01-00	10pin	PAT	56x13x38
FET Module	MJ3	PC045-00-00	10pin	PAT	---
CPU Module	MJ4	PC089-01-00-50P	36pin	PAT	28x40x28
Test Point	TP1,TP2,TP3,TP4,TP6,TP7, TP8,TP9,TP10	KRB-408	Screw, internal	HIROSUGI	φ8x8
Check Pin	CP1,CP2,CP3,CP4,CP5,CP6,CP7, CP8CP9,CP10,CP11,CP12	HOT-2608B	Black	HIROSUGI	2.5x1.75

(c) Driver PCB

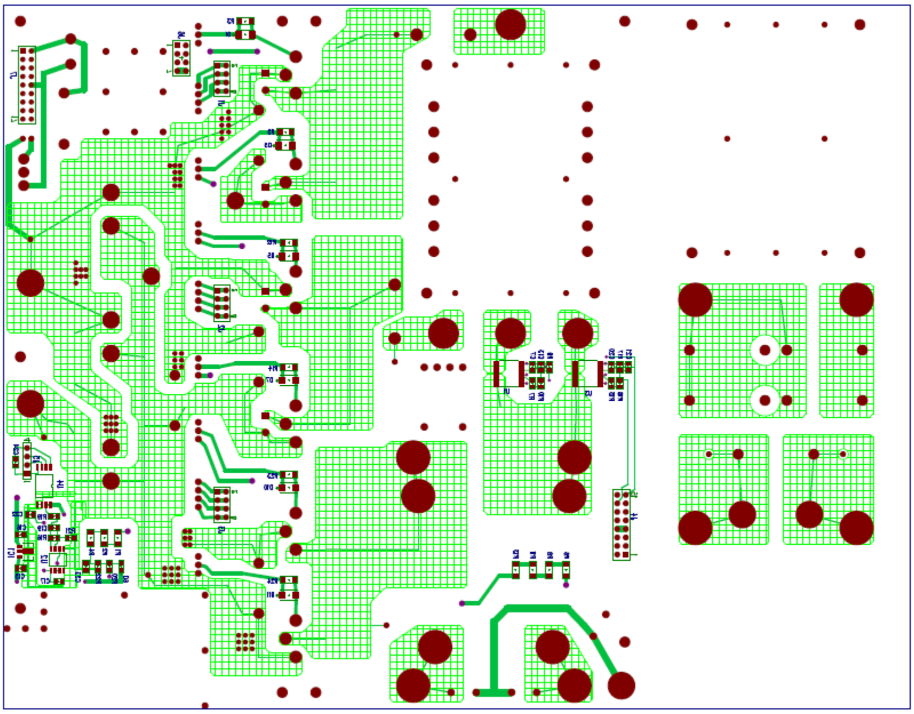
Device	Symbol	Parts Number	Values	Manufacture	Package Size [mm]
Capacitor	C1,C2,C4,C5,C9,C12	GRM188B31H104KA92	0.1μF 50V ±10%	MURATA	1608
Capacitor	C3	GRM1851X1H472JA44	4700pF 50V ±20%	MURATA	1608
Capacitor	C6,C7,C8,C10,C11,C13,C14	GRM21BR71E105KA99	1μF 25V ±10%	MURATA	2012
Diode	D1,D2,D3,D4	1SS355	90V 225mA	ROHM	2.5x1.25x0.7
Diode	D5	RB751S-40	30V 30mA	ROHM	1608
Connector	J1,J3	MB3P-90	250V 3A	JST	7.5x2.4x5.3
Connector	J2	MB4P-90	250V 3A	JST	10x2.4x5.3
Connector	J4	B4B-XH-A	250V 3A	JST	12.4x5.75x7
Photocoupler	PC1,PC2	TLP700A	35V 3mA	TOSHIBA	4.6x6.8x4
Transistor	Q1	SSM3K318T	60V 2.5A	TOSHIBA	2.9x1.6x0.7
Transistor	Q2,Q4	2SCR542P	30V 5A	ROHM	4.6x2.6x1.5
Transistor	Q3,Q5	2SAR542P	30V 5A	ROHM	4.6x2.6x1.5
Resistor	R1,R3	MCR03ERTJ102	1kΩ 1/10W ±5%	ROHM	1608
Resistor	R2	MCR03ERTJ202	10Ω 1/10W ±5%	ROHM	1608
Resistor	R4,R5	MCR03ERTJ103	10kΩ 1/10W ±5%	ROHM	1608
Resistor	R6,R7,R8	MCR10ERTJ4R7	4.7Ω 1/8W ±5%	ROHM	2012
Resistor	R10,R16	MCR03ERTJ331	330Ω 1/10W ±5%	ROHM	1608
Resistor	R11,R17	MCR03ERTJ470	47Ω 1/10W ±5%	ROHM	1608
Resistor	R12,R13,R18,R19	MCR18ERTJ200	20Ω 1/4W ±5%	ROHM	3216
Resistor	R14,R15,R20,R21	MCR18ERTJ4R7	4.7Ω 1/4W ±5%	ROHM	3216
Resistor	R22,R23	MCR18ERTJ1R0	1Ω 1/4W ±5%	ROHM	3216
Transformer	T1	TR008A	---	Shinsei denki	8x13x8
IC	U1	NJM78L05UA	5V 20mA	JRC	4.5x2.5x1.5
IC	U2	NE555D	18V 225mA	TI	DIP-8

■ Inverter A PCB layout

(1) Power PCB

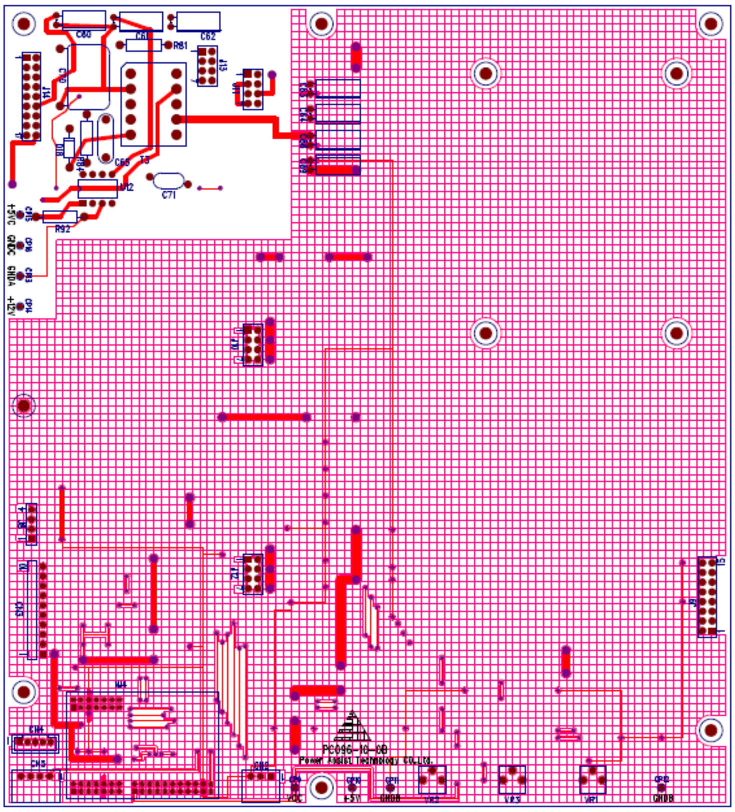


(a) top

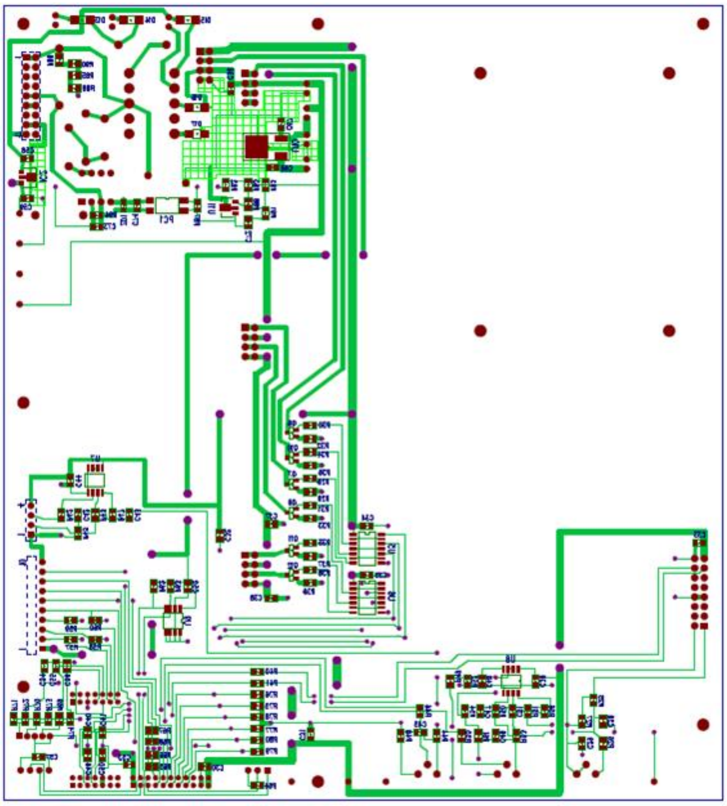


(b) bottom

(2) Control PCB

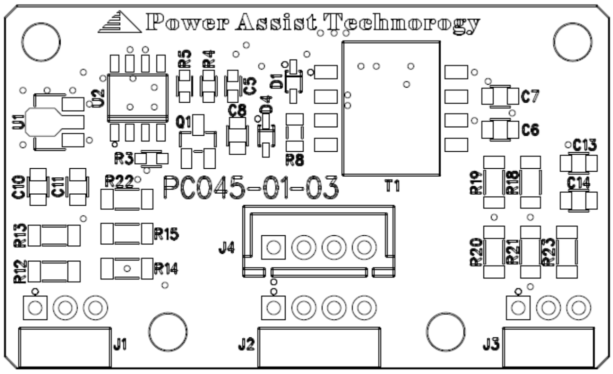


(a) top

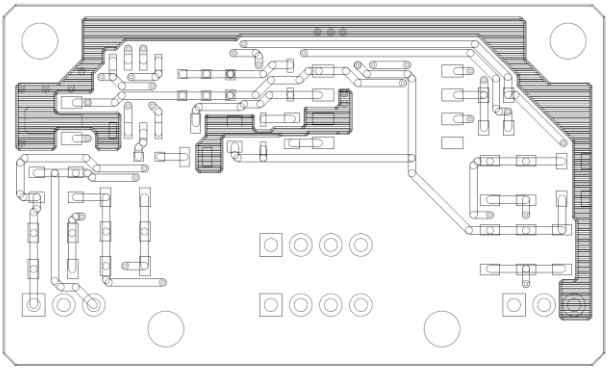


(b) bottom

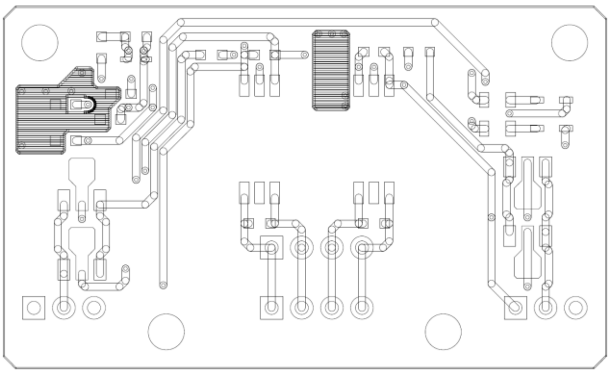
(3) Driver PCB



(a) Top Silk



(b) top



(c) bottom

References:

*1 P. L. Wong, P. Xu, B. Yang, and F. C. Lee, “Performance improvements of interleaving VRMs with coupling inductors,” *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 499–507, Jul. 2001.

*2 T. Kawashima, S. Funabiki, M. Yamamoto, H. Asuke, H. Terui, and S. Takano, “Characteristic analysis and evaluation about mutual coupling inductor of multi-phase trans-linked boost chopper circuit,” *J. Jpn. Inst. Power Electron.*, vol. 35, pp. 136–145, 2010.

*3 M. Yamamoto and H. Horii, “Trans-linked single phase interleaved PFC converter,” *IEEJ Trans. Ind. Appl.*, vol. 130, no. 6, pp. 828–829, 2010.

*4 P. S. Krishna, E. P. Jubin, and K. R. Hari, “Study and analysis of conventional and modified interleaved buck converter,” *Int. J. Eng. Res. Gen.Sci.*, vol. 3, no. 6, pp. 957–964, 2015.

*5 I. O. Lee, S. Y. Cho, and G.W. Moon, “Interleaved buck converter having low switching losses and improved step-down conversion ratio,” *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3664–3675, Aug. 2012.

*6 M. Esteki, B. Poorali, E. Adib, and H. Farzanehfard, “Interleaved buck converter with continuous input current, extremely low output current ripple, low switching losses and improved step-down conversion ratio,” *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4769–4776, Aug. 2015.

*7 J. Imaoka, S.Kimura,W. Martinez, andM.Yamamoto, “A novel integrated magnetic core structure suitable for transformer-linked interleaved boost chopper circuit,” *IEEJ J. Ind. Appl.*, vol. 3, no. 5, pp. 395–404, 2014.

*8 “Ferrite materials for power supply,” *Datasheet*, JFE Ferrite Corporation, 2007.
[Online]. Available: http://www.jfe-frt.com/products/pdf/003.pdf

*9 “Liqualloy toroidal coil technical data sheet,” *Datasheet*, ALPS Electric Co. Ltd., 2017.
[Online]. Available: http://www.alps.com/prod/info/J/HTML/Toroidal/Toroidal/GLT1/datasheet_GLT1.pdf

*10 H. Koshiba, Y. Naito, T. Mizushima, and A. Inoue, “Development of the Fe-based glassy alloy “Liqualloy” and its application to powder core,” *Materia Japan*, vol. 47, no. 1, pp. 39–41, 2008.

*11 F. Krismer and J. W. Kolar, “Accurate power loss model derivation of a high-current dual active bridge converter for an automotive application,” *IEEE Trans. Ind. Electron.*, vol. 57, no. 3, pp. 881–891, Mar.2010.

*12 “SCS212AM SiC Schottky barrier diode,” *Datasheet*, Rohm Co. Ltd., 2015.
[Online]. Available: http://www.rohm.co.jp/web/japan /datasheet/SCS212AM/scs212am-e

*13 T. Miyazaki, H. Otake, Y. Nakakohara, M. Tsuruya, and K. Nakahara, “A fanless operating trans-linked interleaved 5 kW inverter using SiC MOSFETs to achieve 99% power conversion efficiency” *IEEE Trans. Ind. Electron.*, vol. 65, no. 12, pp. 9429–9437, Dec.2018.
[Online]. Available: https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=8320313

Notes

1) The information contained herein is subject to change without notice.

2) Before you use our Products, please contact our sales representative and verify the latest specifications :

3) Although ROHM is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors.
Therefore, in order to prevent personal injury or fire arising from failure, please take safety measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. ROHM shall have no responsibility for any damages arising out of the use of our Poducts beyond the rating specified by ROHM.

4) Examples of application circuits, circuit constants and any other information contained herein are provided only to illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

5) The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM or any other parties. ROHM shall have no responsibility whatsoever for any dispute arising out of the use of such technical information.

6) The Products specified in this document are not designed to be radiation tolerant.

7) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a ROHM representative : transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.

8) Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters.

9) ROHM shall have no responsibility for any damages or injury arising from non-compliance with the recommended usage conditions and specifications contained herein.

10) ROHM has used reasonable care to ensure the accuracy of the information contained in this document. However, ROHM does not warrants that such information is error-free, and ROHM shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.

11) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. For more details, including RoHS compatibility, please contact a ROHM sales office. ROHM shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

12) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.

13) This document, in part or in whole, may not be reprinted or reproduced without prior consent of ROHM.

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/