

## SiC MOSFET

# 5 kW Inverter Circuit Using 4<sup>th</sup> Generation SiC MOSFETs

The high-efficiency inverter circuits using the 3<sup>rd</sup> generation MOSFETs were explained in the application note “5 kW High-Efficiency Fan-less Inverter Circuit” (64AN084J Rev.001) (\*1). This application note introduces inverter circuits in which the 3<sup>rd</sup> generation MOSFETs switching devices are replaced with the 4<sup>th</sup> generation SiC MOSFETs and assesses how this replacement improves the performance.

This evaluation has been performed jointly with Power Assist Technology Ltd. (<https://www.power-assist-tech.co.jp/>)

## Evaluation of the replacement in full bridge type inverter circuits

Figure 1 shows the appearance of the evaluated platform employing the full bridge type inverter circuit. Figure 2 shows its basic circuit configuration.



Figure 1 Evaluated platform

To output 5 kW of power, the switching devices are connected in parallel. Although the number of arms is two, a total of eight switching devices are used. Here, the efficiency is measured and compared between the inverters using the 3<sup>rd</sup> and 4<sup>th</sup> generation SiC MOSFETs for these eight switching devices.

Since the basic design is originally based on IGBT (\*1), the designed oscillation frequency is 20 kHz, leading to the use of larger reactors. However, to facilitate the assessment of difference in the performance of devices using the SiC MOSFET, the frequency is set to 40 kHz for this evaluation.

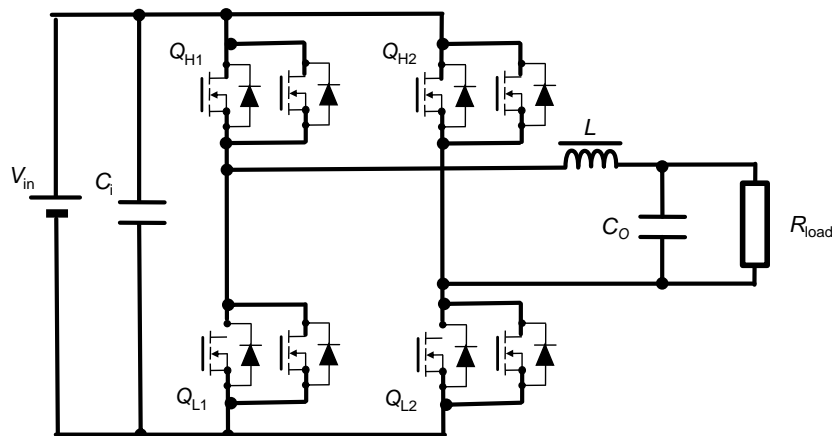


Figure 2 Circuit configuration

## Efficiency evaluation

For comparison of performance in the application note “5 kW High-Efficiency Fan-less Inverter Circuit” (\*1), the input and output power conversion efficiencies were used to explain the difference from IGBT. In this application note, the 3<sup>rd</sup> and 4<sup>th</sup> generation SiC MOSFETs are operated under exactly the same conditions to measure the conversion efficiencies in the full bridge type inverter circuits.

Table 1 shows the evaluation conditions and the circuit constants.

Table 1 Evaluation conditions and parts used

Items	3 <sup>rd</sup> Generation	4 <sup>th</sup> Generation
Switching Devices	650 V, 30mΩ (SCT3030AL)	750 V, 26mΩ (SCT4026DE)
Input voltage ( $V_{in}$ )	DC 320 V	
Input capacitance ( $C_i$ )	560 $\mu$ F $\times$ 4	
Switching frequency ( $f_{sw}$ )	40kHz	
Leakage / Smoothing inductance ( $L$ )	300 $\mu$ H $\times$ 4 (BCH61-35150)	
Copper wire resistance of the reactor	20mΩ $\times$ 4	
Output capacitance ( $C_o$ )	1 $\mu$ F $\times$ 8	
Output voltage ( $V_{out}$ )	AC 200 V	

Figure 3 shows the efficiency of the inverters taking output power  $P_{out}$  as the horizontal axis. Efficiency  $\eta$  is calculated as  $P_{out}/P_{in}$ , i.e., a ratio of  $P_{out}$  against input power  $P_{in}$ . However, the total power loss ( $P_{total} = P_{in} - P_{out}$ ) does not include the gate drive power in the MOSFET.

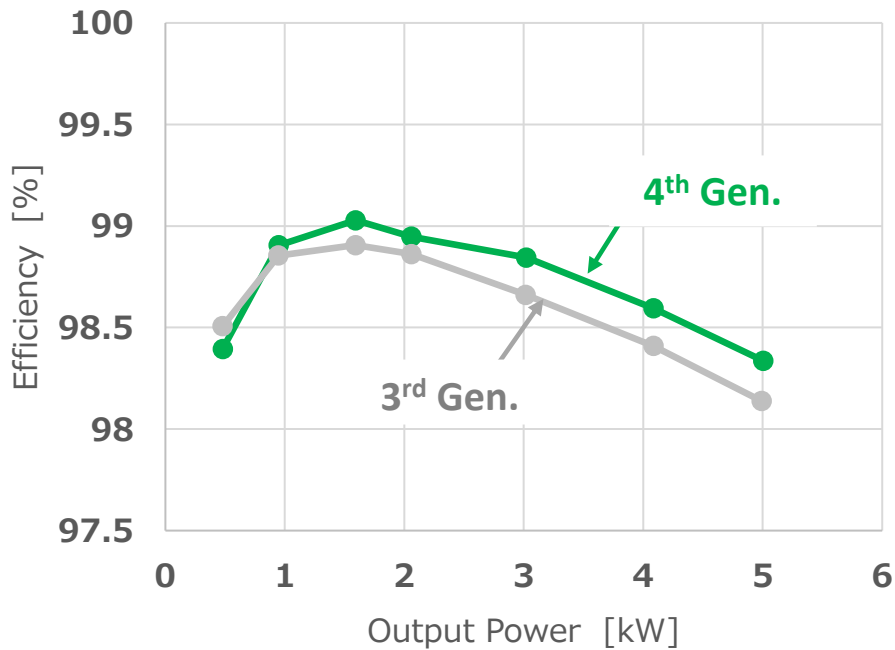


Figure 3 Efficiency taking  $P_{out}$  as indicator

If the 4<sup>th</sup> generation SiC MOSFETs are used, the efficiency is improved over nearly an entire load range. At 5 kW, the loss is reduced by 10.13 W compared with the 3<sup>rd</sup> generation SiC MOSFETs. The reduction in loss results in an improvement of 0.20% in efficiency. Furthermore, the maximum efficiency is improved by 0.12% from 98.91% to 99.03%, achieving an efficiency over 99%.

Next, we examine the loss analysis.

### Loss analysis

The pie charts in Figure 4 show a breakdown of the total power loss ( $P_{total}$ ) of the inverters when they are operated at  $P_{out} = 5$  kW. Pie charts (a) and (b) show the cases of using the 3<sup>rd</sup> and 4<sup>th</sup> generation SiC MOSFETs, respectively. The loss is broken down into the following: the conduction and switching losses in the MOSFET, the conduction loss in the body diode during the dead time periods of the upper and lower arms, the copper and core losses in the reactors, the ESR losses in the input and output capacitors, and others.

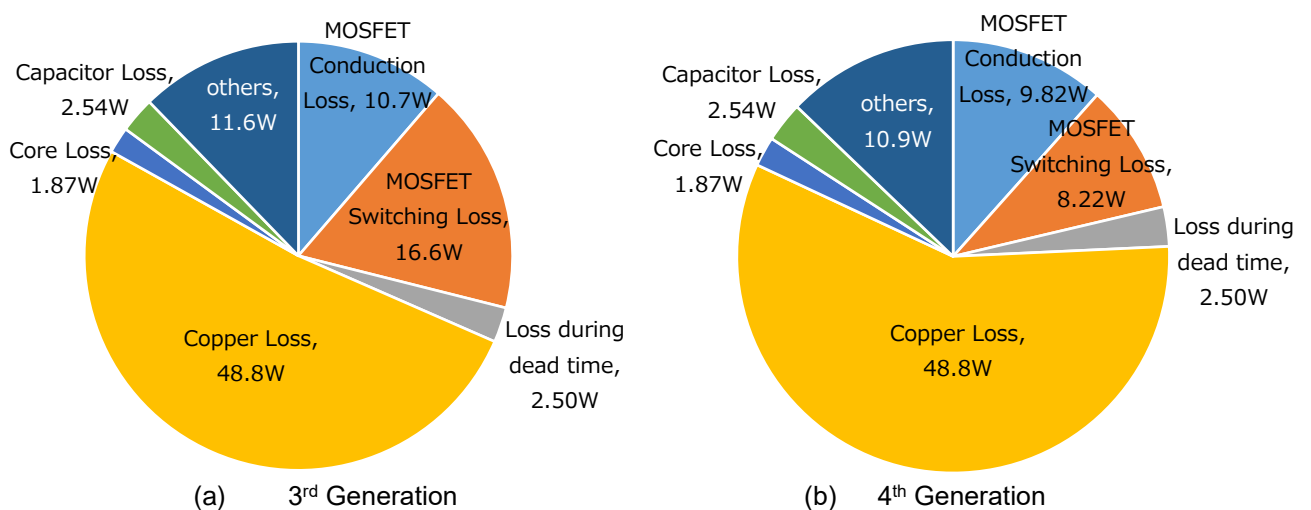


Figure 4 Analysis of  $P_{total}$  at 5 kW

The characteristics of the MOSFET depend on the temperature. However, the inverters were under a sufficient cooling condition using a cooling fan and the temperature increase was approximately 50°C. Therefore, the calculations for this loss analysis are based on the on-resistance ( $R_{ON}$ ) when the temperature is increased by approximately 50°C. The details are explained below.

### 1) Conduction loss in the MOSFET:

For the 4<sup>th</sup> generation SiC MOSFETs,  $R_{DS(ON)}$  is approximately 32mΩ when the temperature is increased by 50°C. The effective current flowing in each MOSFET is 12.5 Arms. The upper arm MOSFET ( $Q_{H1}$  and  $Q_{H2}$ ) and the lower arm MOSFET ( $Q_{L1}$  and  $Q_{L2}$ ) are operated in the synchronous rectification mode, and either of the upper or lower arm MOSFET remain ON except for the dead time (DT) of 220 ns. Since one cycle of the MOSFET is 25 μs, the conduction loss in the MOSFET of the PWM part is  $(12.5 \text{ Arms})^2 \cdot 32\text{m}\Omega \cdot (1 - (220 \text{ ns} \cdot 2) / 25 \mu\text{s}) \cdot 2 \text{ pcs} = 9.82 \text{ W}$ .

Similarly, the conduction loss is calculated to be 10.7 W for the 3<sup>rd</sup> generation SiC MOSFETs, because  $R_{DS(ON)}$  is approximately 35mΩ.

### 2) Switching loss in the MOSFET:

Figures 5 and 6 show the characteristics of  $R_G$ - $E_{SW}$ ,  $R_G$ - $dV/dt$ , and  $R_G$ - $dI/dt$  for the 4<sup>th</sup> generation SiC MOSFETs (SCT4026DE) used in the PWM part. Figures 5 and 6 take drain current  $I_D$  and external gate resistance  $R_G$  as the horizontal axis of the graph, respectively. These characteristics were measured with the double pulse test, which is widely known.

As  $R_G$  is decreased, the switching speed is increased,  $E_{SW}$  is decreased, and  $dV/dt$  and  $dI/dt$  are increased. In the TO-247N package evaluated here, an increase in  $dI/dt$  increases the electricity generated due to the parasitic inductance of the source terminal that reduces the charge or discharge current to the gate capacitance. Therefore, it can be seen that the switching loss shows nearly no change if  $R_G$  is 4.7Ω or less. Accordingly, for this evaluation, the total switching loss is calculated using  $E_{on}$  and  $E_{off}$  when  $R_G$  is 4.7Ω.

The energy of switching loss in the MOSFET ( $E_{SW}$ ) is mainly composed of the energy of turn ON loss ( $E_{on}$ ), energy of turn OFF loss ( $E_{off}$ ), and energy of reverse recovery loss ( $E_{rr}$ ).

The average current flowing through one MOSFET at the point of phase angle  $\theta$  is expressed as Equation (1). Therefore, the average  $P_{sw}$  of the MOSFET in the PWM part is the integrated value of  $E_{total\_sw} \cdot f_{sw}$  over the entire period, and the integration can be calculated with averaging Equation (2).

$$I = \sqrt{2} \cdot 12.5 \cdot \sin \theta \quad (A) \quad (1)$$

$$P_{sw} = \frac{1}{T} \int_0^T E_{total\_sw} f_{sw} dt \cdot 4\text{pcs} = 8.22 \text{ W} \quad (2)$$

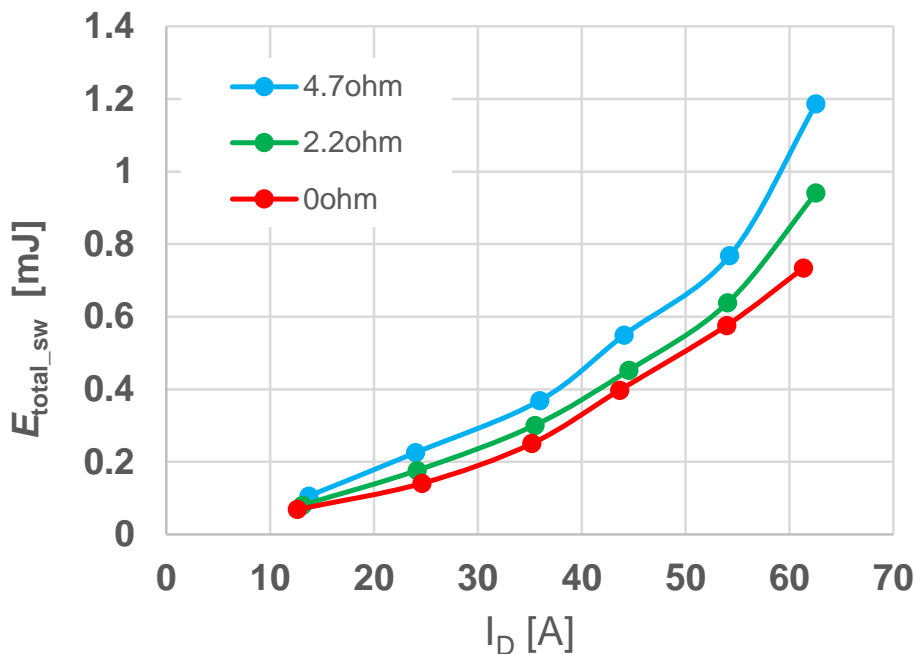


Figure 5 SCT4026DE switching characteristics taking  $I_D$  as the horizontal axis

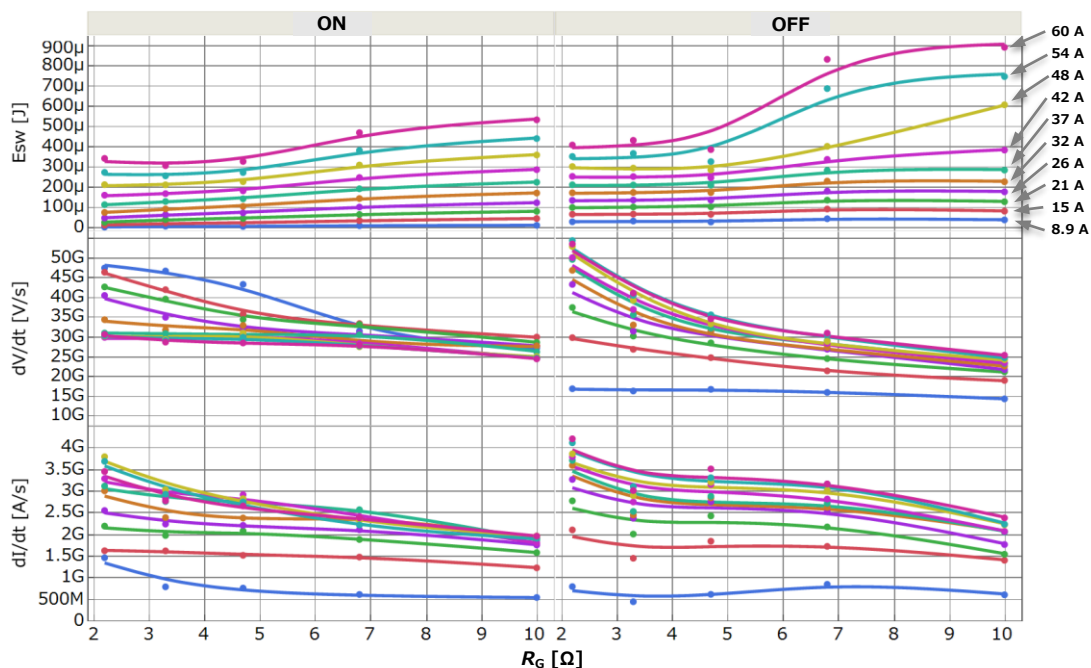


Figure 6 SCT4026DE switching characteristics taking  $R_G$  as the horizontal axis

### 3) Power loss during DT period:

For these inverters, DT is set to 220 ns. During this period, the current flows into the body diode of the MOSFET. The average current flowing through the body diode can also be expressed with Equation (1). As with  $P_{sw}$ , the power loss during the DT period ( $P_{DT}$ ) is calculated according to the following equation.

$$P_{DT} = \frac{1}{T} \int_0^T |V_{DS}| \cdot |I_D| \cdot f_{sw} \cdot 2DT dt \cdot 2pcs. \quad (3)$$

$V_{DS}$  and  $I_D$  represent the source-drain voltage and current of the MOSFET, respectively. Calculation based on the 3<sup>rd</sup> quadrant V-I characteristics of the MOSFET results in  $P_{DT} = 1.25 \text{ W} \cdot 2 \text{ pcs} = 2.50 \text{ W}$ .

### 4) Copper loss:

The inverters are configured with four reactors in series. For operations at 20 kHz, the magnetizing inductance of each reactor is designed to be 300  $\mu\text{H}$  or more, and the number of windings is 40 turns or more. Therefore, the resistance value of the copper winding is 19.53m $\Omega$  and the copper loss when the effective current is 25 Arms is  $(25 \text{ Arms})^2 \cdot 19.53\text{m}\Omega = 12.21 \text{ W}$  for each reactor. Since the four reactors are connected in series, the total copper loss is  $12.21 \text{ W} \cdot 4 = 48.83 \text{ W}$ . This value is basically independent of the carrier frequency.

### 5) Core loss:

The core loss in the reactors can be calculated from the maximum value of reactor ripple current  $\Delta i_L$ , which is determined with Equation (4). Reactors have certain direct current superimposition characteristics that depend on the current value and duty ratio  $d$ . The maximum value is obtained when  $d$  is 0.5, resulting in  $\Delta i_L = 2.58 \text{ A}$ .

$$\Delta i_L = \frac{d(1-d)V_{in}T}{L} \quad (4)$$

From the core loss characteristics of the core material used (FeNi-based high flux core), the core loss is estimated to be 1.87 W.

### 6) Equivalent series resistance (ESR) loss of capacitors:

The ripple current flowing in the input and output capacitors generates a loss due to the equivalent series resistance (ESR) of the capacitors. The ripple current in the output capacitor is equal to  $\Delta i_L$  of the reactors. The ripple current of the input capacitor ( $i_{Cin}$ ) can be calculated with Equation (5).

$$i_{Cin} = \sqrt{\frac{V_{OUT}}{V_{IN(min)}} i_{OUT}^2 \left(1 - \frac{V_{OUT}}{V_{IN(min)}}\right) + \frac{1}{12} \Delta i_L^2} \quad (5)$$

Calculation using these equations results in 2.54 W for the loss in the input and output capacitors. However, most of the loss is generated in the input capacitor.

### 5) Others:

The power losses other than those described above, including the conduction loss in the wiring parts of the circuit board, are approximately 11.6 W and 10.9 W for the third and fourth generations, respectively. The reduction by approximately 0.7 W for the fourth generation can be attributed to the difference in the drive power of the MOSFET, which is considered as one of the factors in increasing the switching speed.

Figure 7 shows a comparison of the breakdown of the losses at 5 kW. It can be seen that the difference in the losses in the transistors has a significant effect on the difference in the total losses. Even when the switching frequency is increased by a factor of two or more, simply replacing the Si IGBT with the 3<sup>rd</sup> generation SiC MOSFETs reduces the total loss by 37 W (28%). Replacing the third generation with the 4<sup>th</sup> generation further reduces the total loss by 10 W (11%). The comparison of the third and fourth generations also indicates that the reduction in the switching loss causes the difference in the total losses.

Table 2 summarizes the performance of the inverter circuits using the respective switching devices. Since this evaluation is performed for the same platform, the size advantages cannot be compared. However, even the switching frequency is increased, a loss reduction as much as 36% is achieved with the 4<sup>th</sup> generation SiC MOSFETs. Therefore, it is evident that a significant performance improvement can be expected, such as simplifying the cooling configuration and downsizing the reactors.

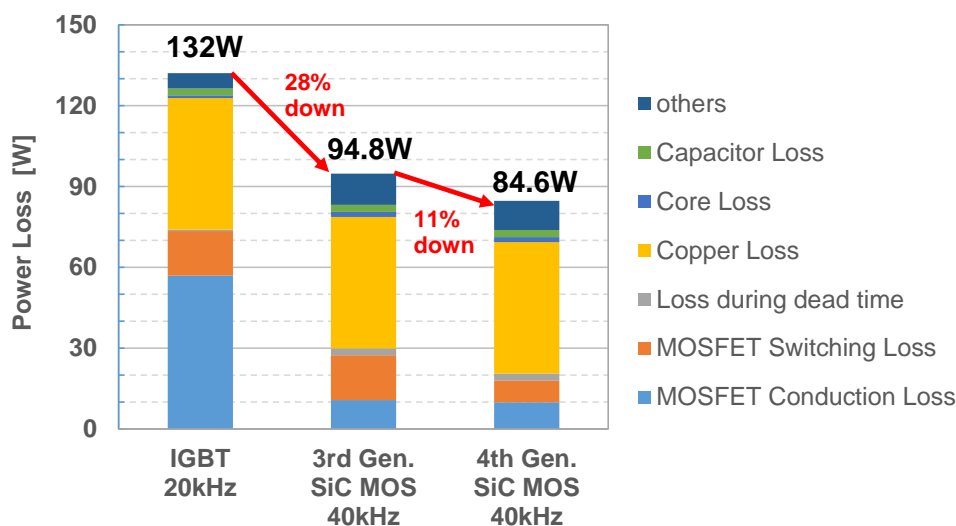


Figure 7 Comparison of breakdown of  $P_{total}$  of inverters at 5 kW

Table 2 Comparison of performance of inverter circuits

	IGBT	3 <sup>rd</sup> Generation SiC MOSFETs	4 <sup>th</sup> Generation SiC MOSFETs
Switching transistors	STGW60H65DFB 650 V, 60 A	SCT3030AL 650 V, 30mΩ	SCT4026DE 750 V, 26mΩ
Switching frequency	20 kHz	40 kHz	40 kHz
Conversion efficiency (@5 kW)	97.43%	98.14%	98.33%
Total loss (@5 kW)	132 W	94.8 W	84.6 W

## Summary

By using SiC MOSFET as the switching devices in the full bridge type inverter circuit, the conversion efficiency can be substantially increased even though the switching operations are performed at a higher frequency compared with Si IGBT. Furthermore, replacing the 3<sup>rd</sup> generation with the 4<sup>th</sup> generation SiC MOSFETs considerably improves the switching characteristics, achieving a further improvement in efficiency.

It is expected that the 4<sup>th</sup> generation SiC MOSFETs can significantly contribute to downsizing and energy conservation of any power supply system.

## References:

\*1. 5 kW High-Efficiency Fan-less Inverter

Application Note (No. 64AN084JRev.001), ROHM Co., Ltd. September 2021



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