Power switching device

Best practices for the connection of Driver Source/Emitter terminals in discrete devices

In recent years, there has been a growing adoption of discrete 4-pin and 7-pin packages featuring an auxiliary (Kelvin) terminal for the gate driving circuit return, referred to as the Driver Source in MOSFETs and the Driver Emitter in IGBTs. The primary function of this terminal is to reduce switching losses in power switching devices by decoupling the gate drive loop from the power loop such as MOSFETs and IGBTs. Its effectiveness, however, hinges on proper connection to the gate driver circuit. Incorrect wiring can even result in device failure. This application note aims to provide guidelines on correctly connecting the Driver Source (Emitter) terminal. It builds upon the previously published application note, "Improvement of Switching Loss by Driver Source," which offers a detailed explanation of power device behavior when driven using this auxiliary terminal.[1]

Target packages

TO-247-4L

TO-263-7L

Connecting the Driver Source terminal

For simplicity, this application note will refer to the auxiliary terminal as the "Driver Source," as in MOSFET devices. However, the principles discussed here are also applicable to other devices with a Kelvin terminal, such as IGBTs. Figure 1 shows the circuit symbol of MOSFET with a Driver Source. Figure 2 illustrates the internal structure of a TO-247-4L package with a MOSFET device.

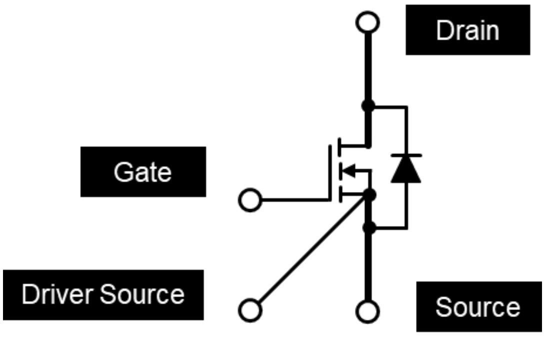


Figure 1. Circuit symbol of a MOSFET with Driver Source

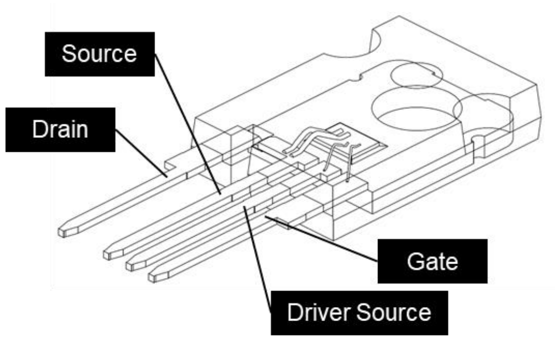


Figure 2. Internal structure of TO-247-4L package with a MOSFET device

Figure 3 shows a MOSFET connected to a gate driving circuit using the Driver Source as a return terminal. In this configuration, the drain current (I_D) flows from the Drain to Power Source terminal, without disturbing the voltage applied to the gate of the device.

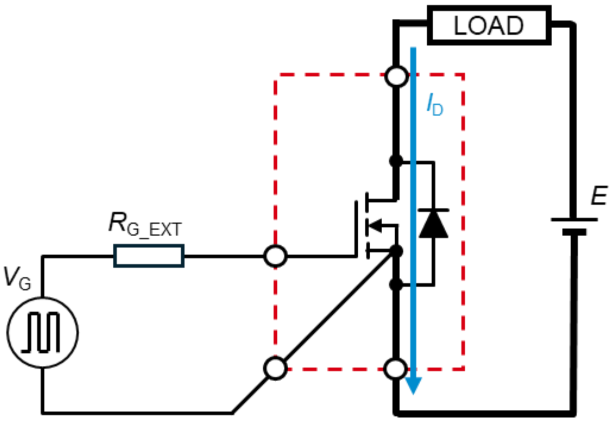


Figure 3. Connection of a MOSFET to the gate driving circuit using the Driver Source terminal

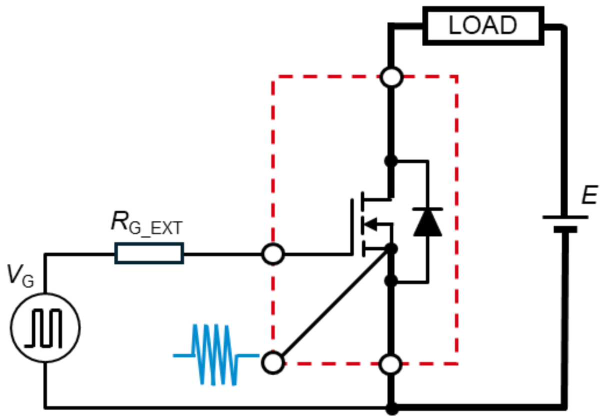


Figure 5. Open Driver Source terminal

Risky configurations for the Driver Source terminal

Even though the Driver Source is connected to the same potential as the Power Source at the chip level (see Figure 2), certain configurations can pose risks to the device:

1. Driver Source and Power Source pins are directly connected together

In the case of a direct connection, as shown in Figure 4, the drain current I_D will partially flow through the Driver Source terminal.

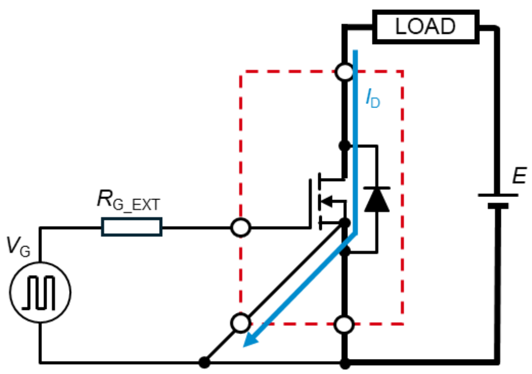


Figure 4. Direct connection of Driver Source and Power Source

The bond wire on the Driver Source side and the bond wire(s) on the Power Source side may differ in thickness and number. Even if the device is used within the rated current, the wire on the Driver Source side may overheat and fail. Additionally, there is a risk of unintended current flow between the Driver Source and Power Source connection points in the chip, which could lead to unwanted heat generation.

2. Driver Source pin is left floating

A floating terminal, as displayed in Figure 5, has high impedance and can emit switching noise. This may lead to unintended effects in the surrounding area and may also cause malfunction of the gate-source signal due to noise interference.

Recommended connection methods for different types of Gate Driver ICs

To address the hazardous connection methods described earlier, the following four suitable connection methods for each type of Gate Driver IC are outlined below.

1. Isolated 1ch Gate Driver IC

Figure 6 shows the circuit diagram when two single-channel isolated Gate Driver ICs (ROHM: BM61x4x) are used in a half-bridge configuration. This setup provides an ideal connection to the Driver Source pin for both high-side and low-side devices.

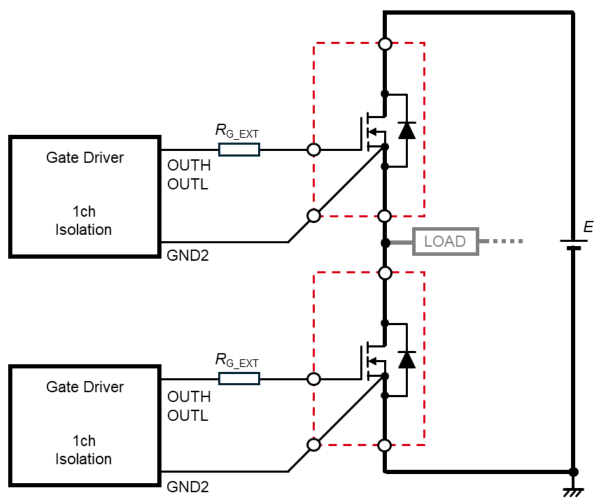


Figure 6. MOSFETs in half-bridge configuration using two single-channel isolated Gate Driver ICs

2. 2ch Gate Driver IC with separated gate drive GND and power GND terminals and no low-side isolation

Figure 7 shows the circuit diagram of a 2ch Gate Driver IC (ROHM: BM60213FV-C) with separated gate drive GND and power GND terminals, used to drive MOSFETs in a half-bridge configuration. In this setup, the high side is isolated using the bootstrap method, while the low side is not isolated. Along with the "Isolated 1ch Gate Driver IC" configuration, this gate driving circuit can also maximize the performance of a power switching device with the Driver Source terminal.

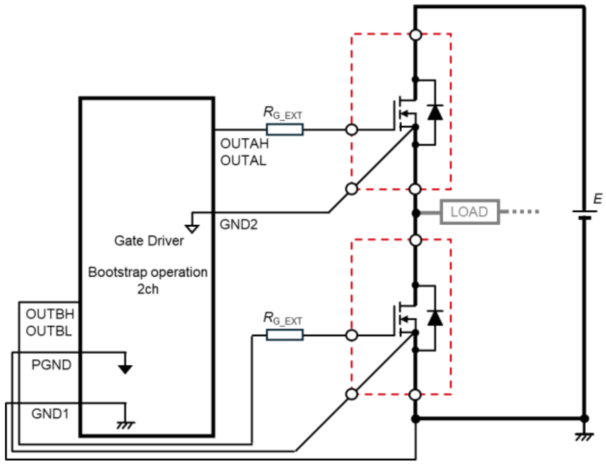


Figure 7. Circuit diagram for using ROHM: BM60213FV-C gate driver IC.

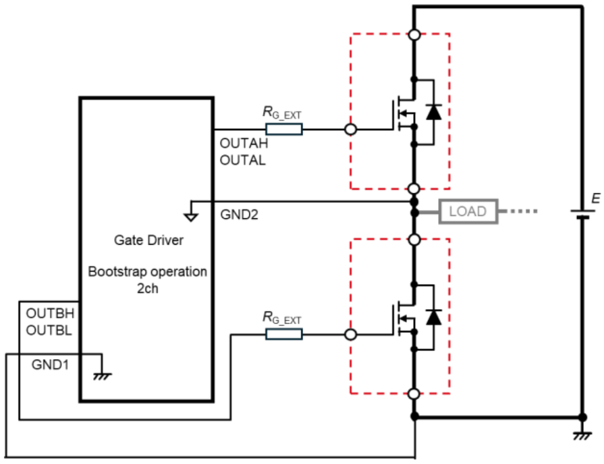
Although ROHM: BM60213FV-C Gate Driver IC features separate GND terminals, it does not offer Miller clamp function, which might be desirable is fast switching applications. A comparator-less Miller clamp circuit that can be added to the gate driving circuit has been introduced in the application note "Design Method for Comparator-less Miller Clamp Circuits".[2]

3. 2ch Gate Driver IC with single GND terminal and no low-side isolation

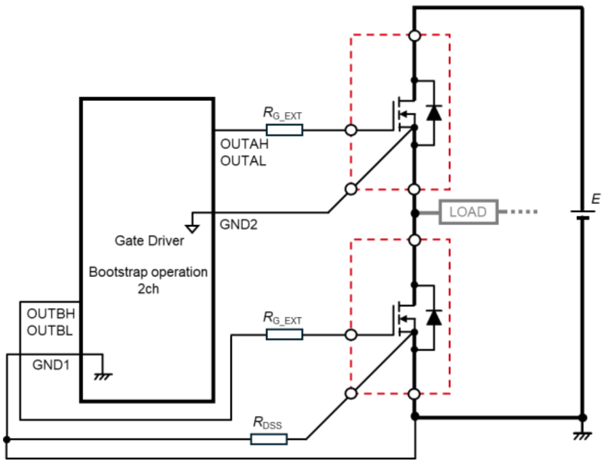
Figure 8 shows the circuit diagram of a 2ch Gate Driver IC (ROHM: BM60212FV-C) connected to MOSFETs in a half-bridge configuration, where the high side is isolated using the bootstrap method and the low side is not isolated. The gate driver IC has a single GND terminal for both gate driving and power circuits. This type of gate driver is not the preferred choice for driving devices with a Driver Source terminal. Options 1 and 2 mentioned earlier should be used whenever possible. Otherwise, if the Gate Driver IC cannot be changed, we recommend:

(a) Using power switching devices without a Driver Source. Packages without a Driver Source terminal, such as TO-247N (3 pins), avoid dangerous configurations that can lead to device failure. However, if it is not possible to switch to a package without a Driver Source, refer to alternative (b).

(b) Inserting an additional resistor (R_{DSS}) between the Power Source and the Driver Source. Please be aware that the switching loss will be similar to that of packages without a Driver Source.



(a) Power switching devices without a Driver Source terminal



(b) Inserting an additional resistor (R_{DSS}) between the Power Source and the Driver Source terminals

Figure 8. Circuit diagram for using ROHM: BM60212FV-C

The current (I_{DRV}) flowing through the Driver Source terminal was verified by simulating the circuit of Figure 9. The parasitic inductance due to the Power Source board pattern is represented by L_{SOURCE}. The parasitic inductance representing the package's internal connection of the Power Source terminal from the PCB to the chip has also been considered in the simulation but for simplicity it is not represented in Figure 9. The simulation results including the waveforms of I_D and I_{DRV} are shown in Figure 10 for L_{SOURCE} = 30 nH and R_G = 2.2 Ω. The condition "Separate Power Source and Driver Source connection" of Figure 10(x) was simulated using the circuit described in Figure 7.

Simulation conditions

SiC MOSFET : SCT4062KR(1200V 62mΩ TO-247-4L)

HV dc voltage : E = 800V

Drain current : I_D = 40A (Pulse)

Gate voltage : V_{GS} = 18 V/0 V

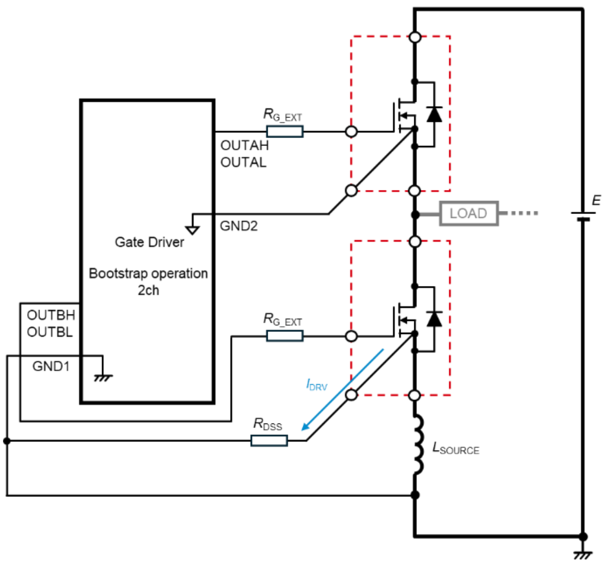
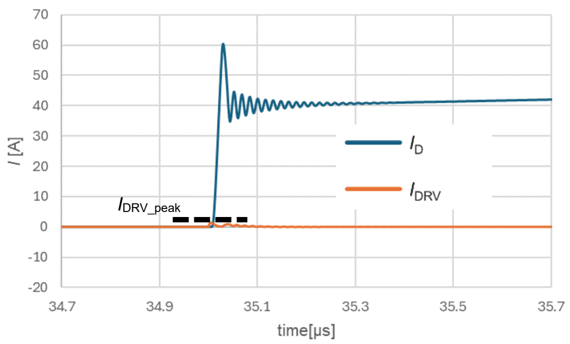
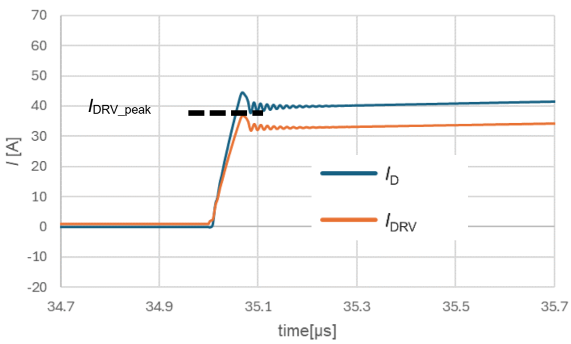


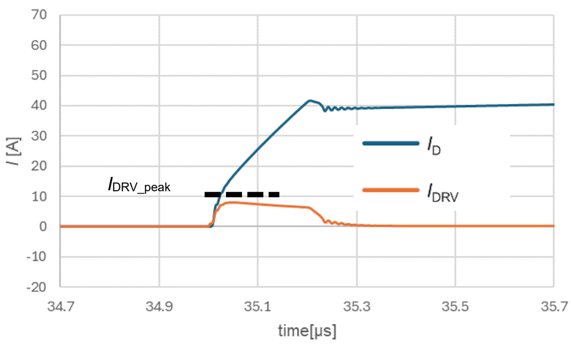
Figure 9. Simulation circuit



(x) L_{SOURCE}=30nH, R_G=2.2Ω (Separate Power Source and Driver Source)

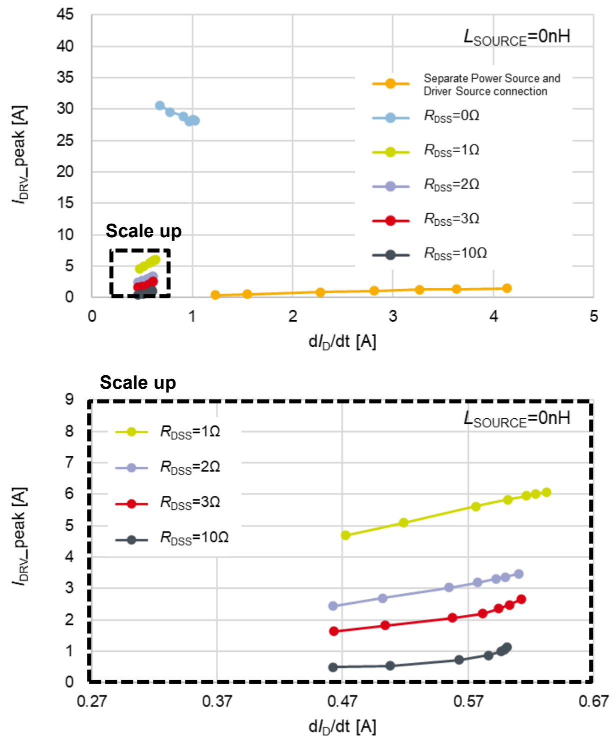


(y) L_{SOURCE} =30nH, R_G=2.2Ω, R_{DSS}=0Ω

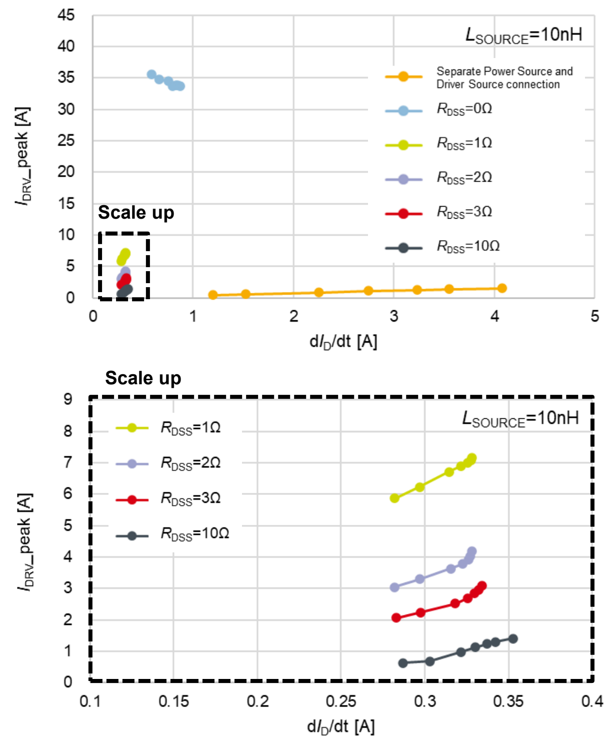


(z) L_{SOURCE} =30nH, R_G=2.2Ω, R_{DSS}=1Ω

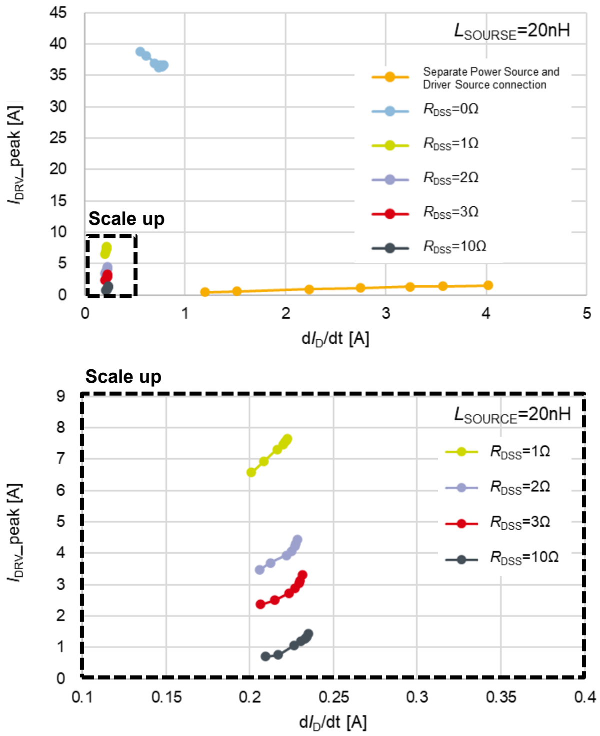
Figure 10. Simulation waveforms



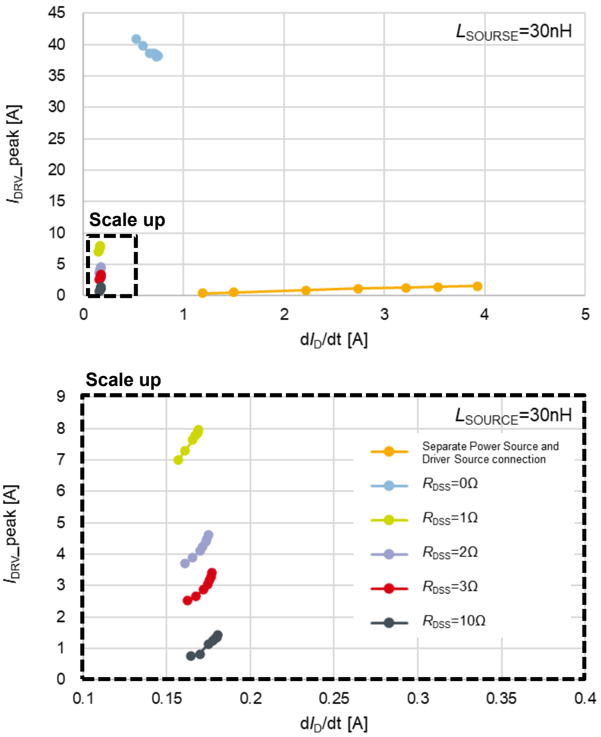
(b-1) L_{SOURCE} =0nH



(b-2) L_{SOURCE} =10nH



(b-3) L_{SOURCE} =20nH



(b-4) L_{SOURCE} =30nH

Figure 11. Simulation results[*1]

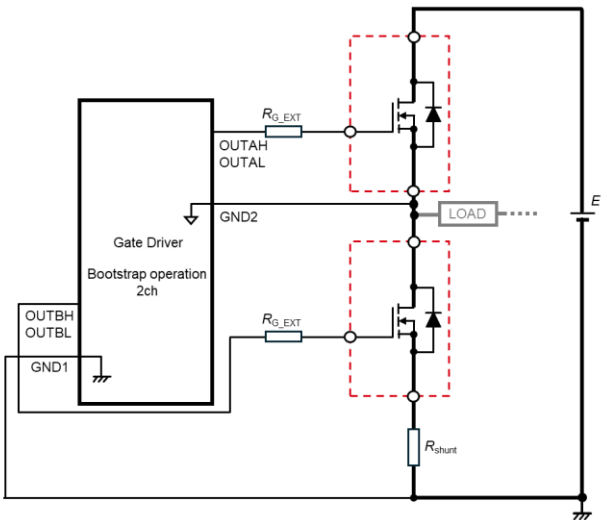
※1 This simulation does not assure the characteristics and operation of your equipment. When using the product, please select the final circuit and constant after thorough consideration and evaluation by the customer.

Figure 11 shows a plot of the peak I_{DRV} values (I_{DRV_peak}) when R_{DSS} and dI_D/dt are varied across four different L_{SOURCE} values, ranging from 0 to 30 nH. As expected, the dI_D/dt decreases from 1–4 A/ns when the source pins are connected separately, to 0.1…0.8 A/ns when the source pins are connected either directly or through a resistor (R_{DSS}). This reduction in dI_D/dt leads to increased switching losses.

The simulations indicate that most drain current flows through the Driver Source terminal when connected directly to the Power Source without an additional resistor R_{DSS}, see Figure 10(y). Considering the fusing current of the wire on the Driver Source side, R_{DSS} should be at least 1 Ω to avoid overloading the bond wire. Please consider for the dimensioning of R_{DSS} that it must be able to dissipate the energy stored in the parasitic inductance L_{SOURCE}. The peak power in that resistor will be affected by the R_{DSS} value selected. It will be higher for low R_{DSS} values, as Figure 11 indicates (P_{peak} = $I_{DRV\_peak}^2$ R_{DSS}). The total energy that the resistor needs to dissipate during each switching instance, however, will decrease for low R_{DSS} values. This is due to the increase of the current I_{DRV}, which reduces the current flowing through L_{SOURCE}: E = ½ L_{SOURCE} (I_D - I_{DRV}).

When connecting shunt resistors, the following points should be considered when using a non-isolated gate driver IC with a single GND terminal. When a power switching device without a Driver Source is used, as in Figure 8(a), and the shunt resistance (R_{shunt}) is part the gate drive circuit, as illustrated in Figure 12, the gate drive voltage applied to the low-side device will be reduced by the following amount:

$$V_{GS\_DOWN} = R_{shunt} \times I_D \qquad (1)$$



Figures 12. Device without a Driver Source terminal connected to a non-isolated gate driver with the shunt resistor included in the gate loop.

As the gate drive voltage decreases, R_{ON} increases, leading to higher losses in the device. Additionally, if the gate drive voltage significantly decreases, it may cause a substantial rise in the MOSFET's ON-state resistance, potentially resulting in thermal destruction. When including R_{shunt} in the gate loop, it is necessary to pay careful attention to these risks and verify that there is no thermal issues in the actual circuit.

If the shunt resistor R_{shunt} is placed outside of the gate loop, as in Figure 13, its function will be suppressed, as both terminals will be connected to GND. The load current will flow mostly through the gate drive return pattern.

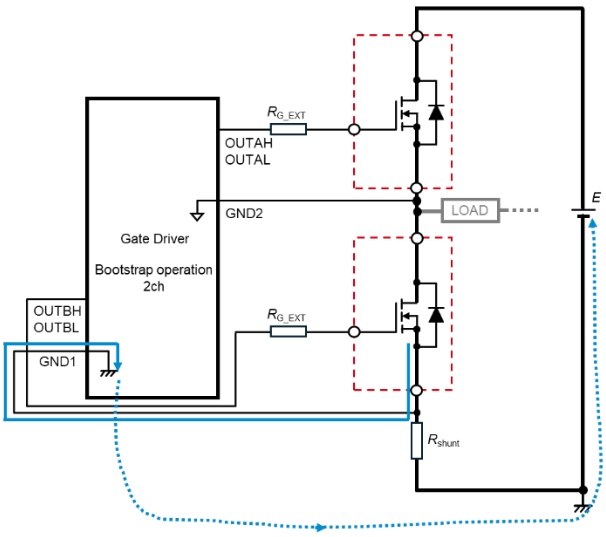


Figure 13. Improper use of R_{shunt} when using a non-isolated gate driver.

Therefore, when using a non-isolated gate driver IC with single GND terminal, the connection method shown in Figure 13 is not suitable. Instead, refer to the connection method indicated in Figure 11. It is important to verify the impact on the thermal behavior of the power devices in the actual circuit should be verified. For devices with a Driver Source, apply the method illustrated in Figure 11, incorporating an additional resistor R_{DSS} between the two source terminals.

Summary

When selecting a power switching device with Driver Source for your design, choose an isolated Gate Driver IC whenever possible. If a non-isolated Gate Driver IC is mandatory, it is strongly recommended to use one with separated GND terminals for the gate driving loop and for the power loop. Special attention must be given to the maximum voltage allowed between the two GND pins, ensuring it is respected under all operating conditions.

If including a Gate Driver IC with separate GND terminals is not feasible, consider using a power switching device without Driver Source. Pay close attention to the shunt resistance and its effect on the gate voltage.

If using a non-isolated single-ground Gate Driver IC for a power device with Driver Source is unavoidable, an additional resistor between Power Source and Driver Source can be employed as a last resort. This is, however, not the preferred solution outlined in this application note.

References:

[1] Improvement of switching loss by Driver Source
Application Note (No. 62AN040E Rev.002)
ROHM Co., Ltd., April 2020
Improvement of switching loss by Driver Source (rohm.com)

[2] Design Method for Comparator-less Miller Clamp Circuits
Application Note (No. 65AN011E Rev.002)
ROHM Co., Ltd., April 2022
Design Method for Comparator-less Miller Clamp Circuits (rohm.com)

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