SiC MOSFET

Design Method for Comparator-less Miller Clamp Circuits

Power semiconductors, such as MOSFETs and IGBTs, are used as switching elements in various power supply applications and power lines. SiC MOSFETs, which are increasingly employed recently, operate at such a high speed that changes in the voltage and current during switching are significantly affected by the package inductance of the device itself as well as the wiring inductance of peripheral circuits. Particularly, since a positive surge in the gate-source voltage can occur unexpectedly during the changes in the voltage and current of the device itself, various countermeasures against such surges have been considered. Accordingly, this application note is aimed at providing a design method for “comparator-less Miller clamp (CLMC) circuits” to implement an external Miller clamp (MC) circuit as a countermeasure against the positive surges in the MOSFETs.

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Surges occurring in the gate-source voltage

Application Note “Gate-Source Voltage Behavior in a Bridge Configuration”*1 provides a detailed explanation for the gate-source voltage generated when a switching device in a bridge configuration is turned ON or OFF. In a synchronized boost circuit as shown in Figure 1, positive surges occur not only on the switching side (LS) but also on the commutation side (HS) depending on the voltage on the switching side.

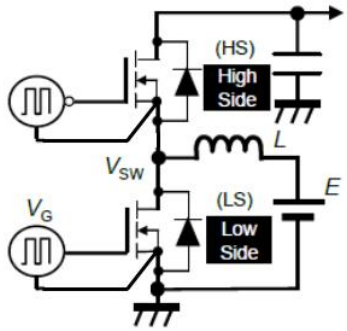

Figure 1. Synchronized boost circuit (4L device)

Figure 2 shows the behavior when the LS is turned ON. The horizontal axis indicates the time. Time regions t_k (k = 1 to 5) are defined as follows.

t_1: Period while the HS is ON (synchronous rectification period)

t_2: Dead time period from when the HS is turned OFF until the LS is turned ON

t_3: Period while the LS is ON and the MOSFET current is changing

t_4: Period while the LS is ON and the MOSFET voltage is changing

t_5: Period while the LS is ON

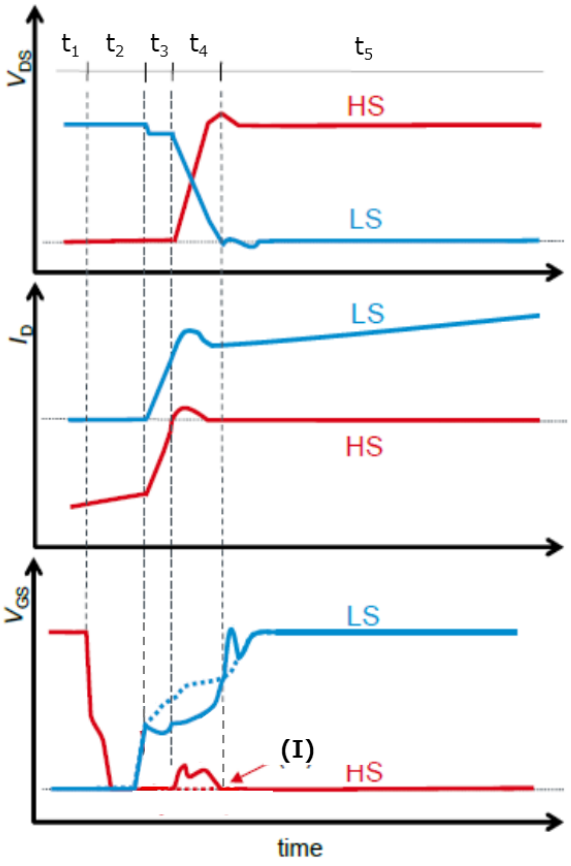

Figure 2. Behavior of the gate-source voltage (during turn ON)

The event (I) shown in the figure is caused by the following factor.

Event (I): Change in the drain-source voltage (dV_{DS}/dt)

Comparator-less Miller clamp circuits

The positive surge in the event (I) as explained in Figure 2 can be reduced with a Miller clamp circuit.

However, this positive surge may be found after a gate driver IC was selected. In this case, it is difficult to replace the gate driver IC with one with a built-in Miller clamp circuit afterward. For such cases, we propose the CLMC circuits that can be driven with an external circuit as shown in Figure 3.

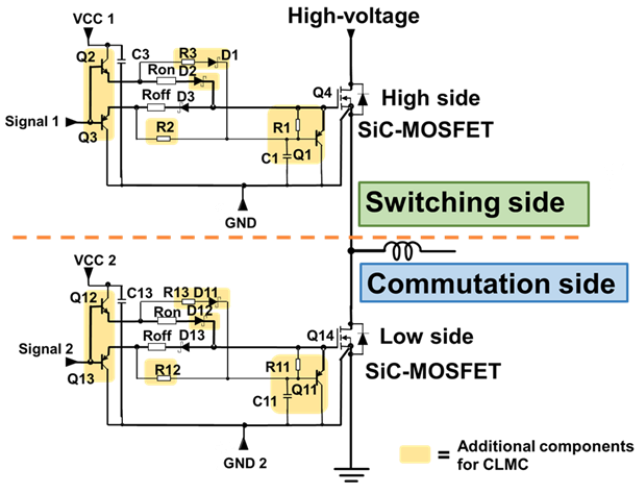

Figure 3. CLMC circuit configuration

Figure 4 shows the timing chart of the CLMC circuit.

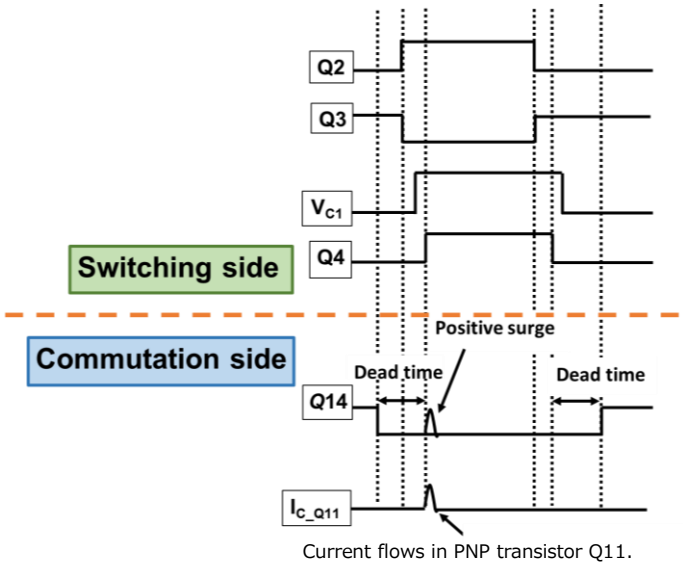

Figure 4. Timing chart of CLMC circuit

As shown in Figure 3, the CLMC circuit is characterized by the ability to be driven with the gate drive signal of the SiC MOSFET without requiring any comparators.

Next, we explain the operation of the CLMC circuit.

Operation of comparator-less Miller clamp circuits

- Switching side

  As shown in Figure 4, when SiC MOSFET Q4 is turned ON, R3 and D1 are used to charge C1 earlier than the gate of the SiC MOSFET, preventing Q1 from being turned ON.

  Similarly, when the SiC MOSFET is turned OFF, R2 and Q3 are used to discharge C1 later than the gate of the SiC MOSFET, preventing Q1 from being turned ON.

- Commutation side

  As also shown in Figure 4, a positive surge occurs at the gate of Q14 on the commutation side when the SiC MOSFET on the switching side is turned ON.
  At this time, since C11 is not charged, the charging current flows through R11 and charges C11. Then, Q11 can be turned ON by voltage V_{BE} applied between its base and emitter, clamping the positive surge.

Design of comparator-less Miller clamp circuits

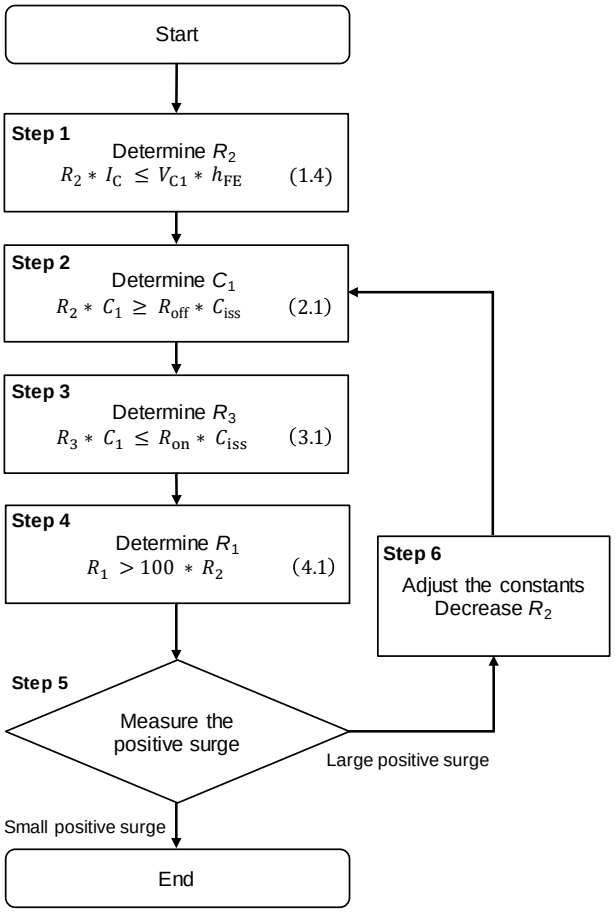

Figure 5. Design flow for components

Step 1: Determine R_2

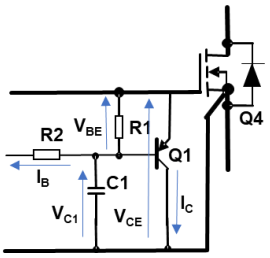

Figure 6. Bipolar transistor peripheral circuit

First, assume that the emitter-collector voltage of bipolar transistors Q1 and Q11 is V_{CE} and the base-collector voltage is V_{C1}. If the base-emitter voltage V_{BE} of Q1 and Q11 is approximately 0.7 V, the following relation holds:

$$V_{C1} = V_{CE} - 0.7 \quad (1.1)$$

Set your own positive surge amplitude V_{CE} to be clamped and calculate V_{C1}.

Use V_{C1} calculated with Equation (1.1) to calculate I_B. If the current flowing to the base is I_B, the following relation holds:

$$I_B = V_{C1} / R_2 \quad (1.2)$$

Furthermore, using h_{FE} of the bipolar transistors used for Q1 and Q11, the following relation holds:

$$I_C = I_B * h_{FE} \quad (1.3)$$

From Equations (1.2) and (1.3), Equation (1.4) is obtained for the cases where you want to reduce a positive surge larger than V_{CE}.

$$R_2 * I_C \leq V_{C1} * h_{FE} \quad (1.4)$$

Step 2: Determine C_1

Next, determine C_1. C_{iss} is the value of C_{iss} of the SiC MOSFETs used for Q4 and Q14. If time constant $C_1 * R_2$ is the time constant of the SiC MOSFET $C_{iss} * R_{off}$ or less, Q1 is erroneously turned ON during turn OFF. Therefore, Equation (2.1) must be true.

$$R_2 * C_1 \geq R_{off} * C_{iss} \quad (2.1)$$

There is no upper limit of C_1 with Equation (2.1) only. However, if C_1 is too large, the drive power of the gate driver may be affected. Therefore, set C_1 as small as possible to keep Equation (2.1) true. In addition, the standard for the C_1 value that may affect the drive power of the gate driver is provided as follows:

$$C_1 \leq C_{iss} \quad (2.2)$$

If C_1 exceeds C_{iss}, set the values of R_2, V_{CE}, and R_{off} again.

Step 3: Determine R_3

Determine R_3 similarly. To prevent Q1 from being erroneously turned ON when Q4 is turned ON, set time constant $C_1 * R_3$ to $C_{iss} * R_{on}$ or less.

$$R_3 * C_1 \leq R_{on} * C_{iss} \quad (3.1)$$

Step 4: Determine R_1

Next, determine R_1. Use Equation (4.1) to determine R_1 so that its influence on R_2 is 1% or less.

$$R_1 > 100 * R_2 \quad (4.1)$$

Step 5: Measure the positive surge

If the positive surge measured here is smaller than V_{CE}, the adjustment is finished. If the positive surge is larger than V_{CE}, continue to step 6.

Step 6: Adjust the constants

Set R_2 smaller than the value determined in step 1. Then, continue to step 2 and beyond. Always select the value of C_1 as small as possible to keep Equation (2.1) true. In addition, if Equations (3.1) and (4.1) still hold under the condition with reconfigured R_2 and C_1, it is unnecessary to set R_3 or R_1 again.

The procedure is finished if the remeasured positive surge is smaller than V_{CE}. If the positive surge is still larger, repeat step 6.

Waveforms after adjustment of the circuit constants

Design a circuit according to the design procedure in practice. Use the SiC MOSFET SCT3040KR for Q4 and Q14, and the bipolar transistor BSS5130AHZG for Q1 and Q11.

Step 1: Determine R_2

Assume that positive surge amplitude V_{CE} to be clamped is 4 V and V_{C1} is 3.3 V. Assume that h_{FE} is 15 and I_C is 3 A, and use Equation (1.4) to set the constant as follows.

$$R_2 * 3\,A \leq 3.3\,V * 15$$
$$R_2 \leq 16.5\,\Omega$$
$$R_2 = 4.7\,\Omega$$

Step 2: Determine C_1

Assume that C_{iss} is 2 nF and R_{off} is 2.2Ω, and use Equation (2.1) to determine the constant as follows.

$$4.7\,\Omega * C_1 \geq 2.2\,\Omega * 2.2\,nF$$
$$C_1 \geq 940\,pF$$
$$C_1 = 1\,nF$$

Step 3: Determine R_3

Assume that R_{on} is 10Ω, and use Equation (3.1) to determine the constant as follows.

$$R_3 * 1\,nF \leq 10\,\Omega * 2\,nF$$
$$R_3 \leq 20\,\Omega$$
$$R_3 = 3.3\,\Omega$$

Step 4: Determine R_1

Since 4.7Ω is selected for R_2, the constant is determined as follows from Equation (4).

$$R_1 > 100 * 4.7\ \Omega$$
$$R_1 = 4.7\ \mathrm{k\Omega}$$

Step 5: Measure the positive surge

Figure 7 shows the gate-source voltage when the switching side is turned ON in the following configurations: a CLMC circuit with the constants determined as described above, a gate driver IC with a built-in Miller clamp (hereafter referred to as a "built-in MC"), and a circuit using no Miller clamp (hereafter referred to as "no MC"). In addition, Figure 8 shows the gate-source voltage on the commutation side during this time.

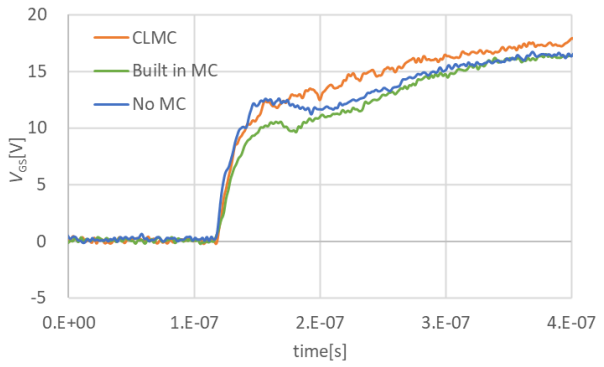

Figure 7. Gate-source voltage on the switching side when the switching side is turned ON

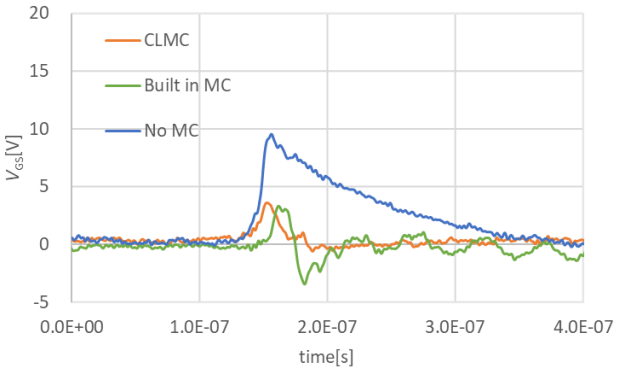

Figure 8. Gate-source voltage on the commutation side when the switching side is turned ON

From Figure 8, the maximum values of the positive surge are 9.5 V, 3.6 V, and 3.3 V for the no MC, CLMC, and built-in MC configurations, respectively. In the CLMC configuration, the adjustment of the circuit constants is finished since the positive surge is smaller than V_{CE} at 4 V.

Since the difference between the CLMC and built-in MC configurations is 0.3 V, the effect of the CLMC can be well confirmed. Furthermore, a phase delay occurs in the built-in MC configuration compared with the CLMC and no MC configurations. This is due to a longer rise time of the gate voltage when the SiC MOSFET is turned ON in the built-in MC configuration. Since the MOSFET for the built-in Miller clamp of the gate driver IC is OFF, C_{oss} of the MOSFET for the Miller clamp appears as the input capacitance of the SiC MOSFET, resulting in the longer rise time. This also produces a delay in the positive surge.

Waveforms without adjustment of the circuit constants and their problems

In this section, we explain problems that may occur if the circuit constants are not adjusted according to the design flow in Figure 5.

First, Figure 9 shows a graph indicating the relation of C_1 and the positive surge when R_1 and R_2 are fixed at 4.7kΩ and 1Ω, respectively.

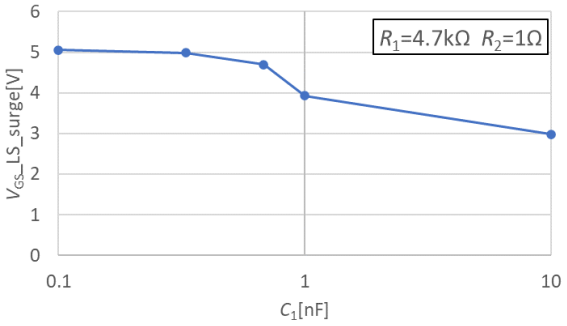

Figure 9. Relation of C_1 and the positive surge

In addition, Figure 10 shows the gate-source voltage waveforms when the switching side is turned ON with C_1 at 100 pF under the condition in Figure 9. The HS and LS represent the high side (switching side) and the low side (commutation side), respectively.

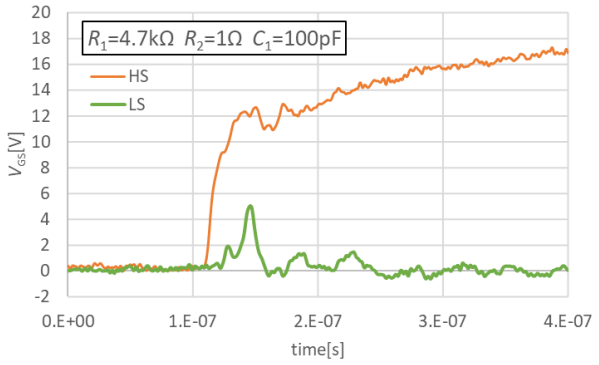

Figure 10. Gate-source voltages when the switching side is turned ON

As shown in Figure 10, if Equation (2.1) is ignored in step 2 and C_1 is small, the positive surge is increased. This is because the effect of the Miller clamp is decreased. If a smaller C_1 is set, the bases of Q1 and Q11 are charged more quickly. As a result, the base voltage is increased and base-emitter voltage V_{BE} is decreased for Q1 and Q11, reducing the effect of the Miller clamp.

Figure 11 shows the gate-source voltage waveforms when the switching side is turned ON with C_1 at 10 nF under the condition in Figure 9. In addition, Figure 12 shows the gate-source voltage waveforms when the switching side is turned OFF.

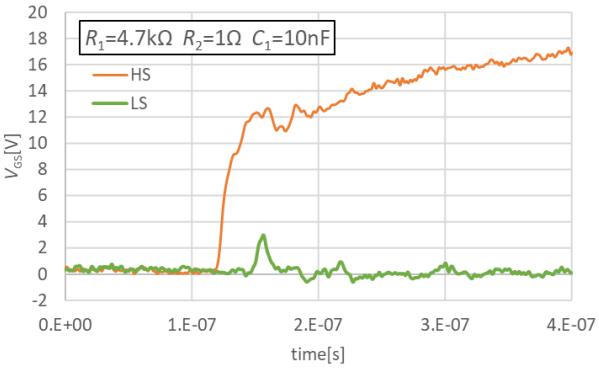

Figure 11. Gate-source voltages when the switching side is turned ON

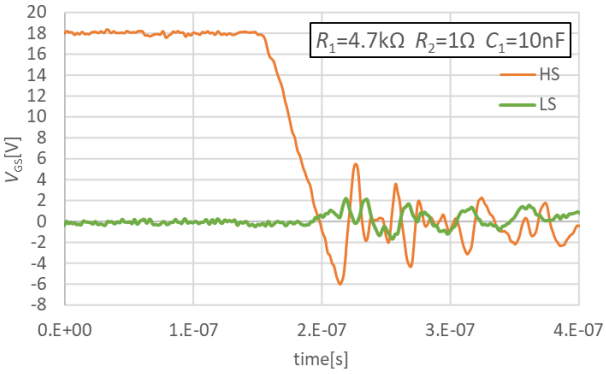

Figure 12. Gate-source voltages when the switching side is turned OFF

The larger the C_1, the smaller the positive surge. However, if Equation (2.2) in step 2 is ignored and C_1 is too large, the gate-source voltage oscillates during turn OFF as with the voltage waveforms shown in Figure 12. This is because Q1 is turned ON by an increase in V_{BE} of bipolar transistor Q1. If C_1 is too large, the base voltage is not charged, resulting in the increase in V_{BE}. Based on these considerations, always observe Equation (2.2).

Next, Figure 13 shows the gate-source voltage waveforms with a higher R_2 when the switching side is turned ON.

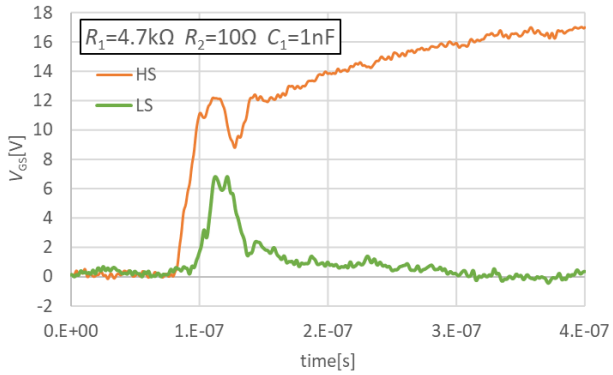

Figure 13. Gate-source voltages when the switching side is turned ON

Even if the circuit is designed so that Equation (1.4) can hold, the positive surge is increased with a higher R_2. This is because time constant C_1 * R_2 is larger and the discharge takes a longer time, leaving charges in the base of Q1. Therefore, it is necessary to set the time constant with R_2 and C_1 so that Equation (2.1) can hold and decrease R_2 as far as possible at the same time.

Results of board evaluation

The efficiencies are measured in the CLMC, built-in MC, and no MC configurations. The result is shown in Figure 14.

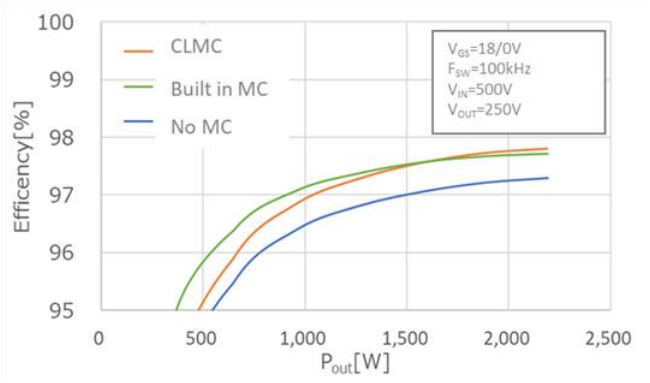

Figure 14. Result of comparison of efficiencies

In Figure 14, under a light load of 1.5 kW or less, the efficiency is the highest for the built-in MC configuration, followed by the CLMC and then no MC configurations. The low efficiency for the no MC configuration is due to a larger switching loss caused by the erroneous turn ON. The highest efficiency for the built-in MC configuration can be explained as follows. As described above, the rise time of the gate voltage is longer due to the MOSFET for the built-in Miller clamp of the gate driver IC. Therefore, dI_D/dt (change in the drain current) is decreased and the maximum value of I_D (drain current) is decreased. As a result, the efficiency is increased compared with the CLMC configuration because the conduction loss is decreased.

However, under a heavy load above 1.5 kW, the efficiency is the highest for the CLMC configuration with a faster switching speed. Note that the drive power of the gate driver is increased due to C_1. This is not directly related to the drive of the SiC MOSFETs including Q4 and Q14.

Summary

Using the CLMC allows you to reduce the positive surge compared to the no MC configuration and obtain a higher efficiency under a heavy load compared with the built-in MC configuration. Therefore, the CLMC configuration is expected to be fully effective particularly under a heavy load.

The most important point for designing a CLMC circuit is to first keep Equation (2.1) always true, and design the circuit so that the base of Q1 always falls after Q4 is turned OFF.

Furthermore, keep Equation (3.1) always true as well, and design the circuit so that the base of Q1 always rises before Q4 is turned ON.

References:

*1 “Gate-Source Voltage Behavior in a Bridge Configuration” Application Note (No. 60AN134JRev.002)
ROHM Co., Ltd., April 2020

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