SiC MOSFET

Basics and Design Guidelines for Gate Drive Circuits

SiC MOSFETs serve as the primary switching devices in a wide range of switching power supplies, controlled by applying a constant gate-source voltage. To ensure optimal performance with low conduction and switching losses as well as reduced electromagnetic interference (EMI), it's crucial to design an effective gate drive circuit. To harness the full potential of SiC MOSFET devices, it's essential to comprehend the fundamental state transitions that occur when a gate-to-source voltage is applied. This application note provides a comprehensive summary of these state transitions and serves as a guide for the design of gate drive circuits for SiC MOSFET devices.

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1. About SiC MOSFET

1.1 Importance of SiC MOSFET

In recent years, the rapid advancement of electric mobility (e-mobility) has underscored the need for efficient power conversion systems. Power conversion entails altering the form of electrical power by selectively switching current on and off to regulate the power delivered from the source to the load or by converting direct current to alternating current. Power devices serve as the essential switches for these on/off operations. Figure 1 illustrates the power handling capacity and the switching frequency range of these power devices.. Furthermore, the demand for energy-efficient and compact equipment has been on the rise. Achieving miniaturization of passive components like inductors and capacitors is possible by increasing the switching frequency. However, there's a trade-off to consider, as higher switching frequencies can lead to increased switching losses. SiC MOSFETs provide an attractive solution with their excellent switching properties, making them crucial for a wide range of applications.

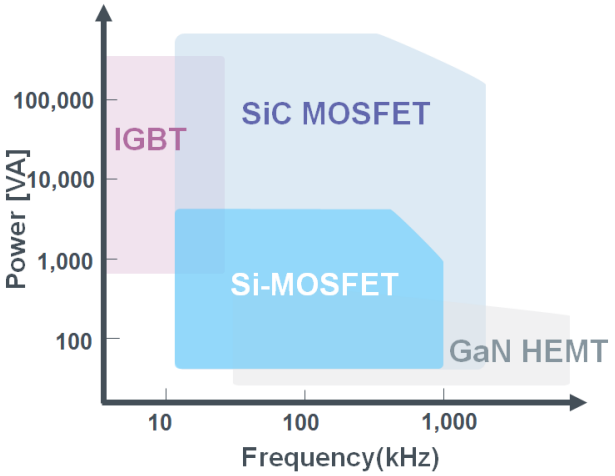

Figure 1. Power handling and switching frequency range for semiconductor devices.

1.2 Basic construction of SiC MOSFET

The planar and trench SiC MOSFET gate structures are shown in Figure 2. When a voltage is applied to the gate electrode, an electric field is established across the gate oxide (SiO2 layer). This electric field forms and controls the conductivity of the horizontal channel region directly beneath the gate electrode. Current flows through this channel from drain to source. With this mechanism, MOSFET realizes voltage-controlled switching, high-speed operation with n-type channels, and high voltage resistance with a vertical configuration.

SiC MOSFET can be broadly divided into planar structures (Figure 2-(a)) and trench structures (Figure 2-(b)) depending on the gate-structure and drift-layer structure.

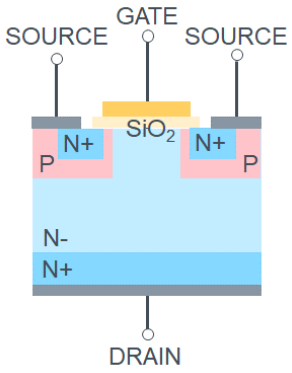

Figure 2-(a). Planar structure

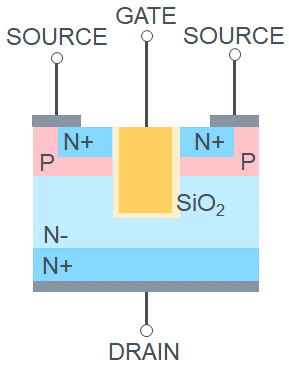

Figure 2-(b). Trench structure

・Planar structure

In a planar gate structure, the gate electrode is formed on the surface of the semiconductor material as shown in Figure 2 (a). As a result, horizontal channel is formed beneath the gate electrode.

・Trench structure

In a trench gate structure, the gate is constructed as a deep trench etched into the semiconductor material, as shown in Figure 2 (b). The gate electrode is then deposited inside the trench. In this structure, the channels are formed vertically and therefore, miniaturization of the cells is possible.

1.3 Parasitic capacitance characteristics

SiC

A SiC MOSFET consists of three electrodes: source, gate, and drain. The capacitance between the source and gate electrodes is denoted as C_{GS}, the capacitance between the drain and gate electrodes is C_{GD}, and the capacitance between the source and drain electrodes is C_{DS}.

As shown in Figure 3, C_{GD} is determined by the electrostatic capacitance formed by the gate oxide film as a dielectric, while C_{GS} is determined by the capacitance C_O formed between the gate-source and the sum of the P-channel (C_P) and N-channel (C_{N+}). Therefore, the gate-source capacitance can be expressed as ($C_{GS}=C_O+C_P+C_{N+}$).

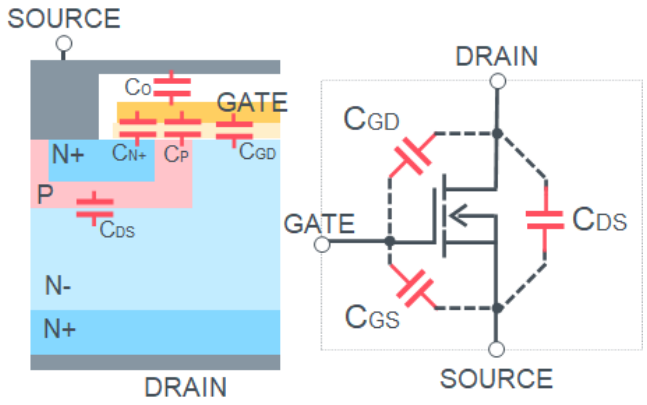

Figure 3. Parasitic capacitance in SiC MOSFET

A trench structure with a single-cell structure and a gate oxide etched vertically tends to have larger parasitic capacitance. However, ROHM's SiC MOSFETs offer low on-resistance of the trench structure by adapting advanced processing technology. As the chip size decreases, the parasitic capacitance of the entire chip can also be reduced. Figure 4 compares the gate capacitance of ROHM's 2G SiC MOSFET (planar structure) and the 4G SiC MOSFET (trench structure). In 4G SiC MOSFET, the parasitic capacitance is smaller than that of the planar structure due to the miniaturization of the cell, even though the gate structure is trench.

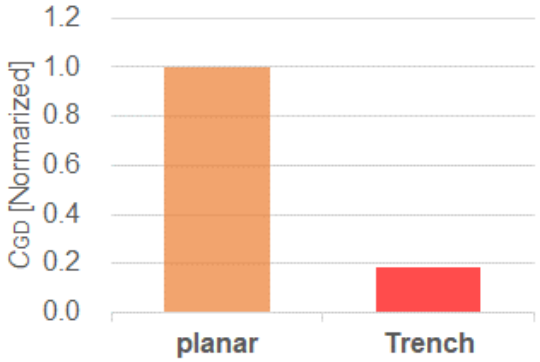

Figure 4-(a). C_{GD} Comparison (ROHM Planar vs Trench)

Measurement conditions: V_{GS}=0V, V_{DS}=800V, T_j=25℃

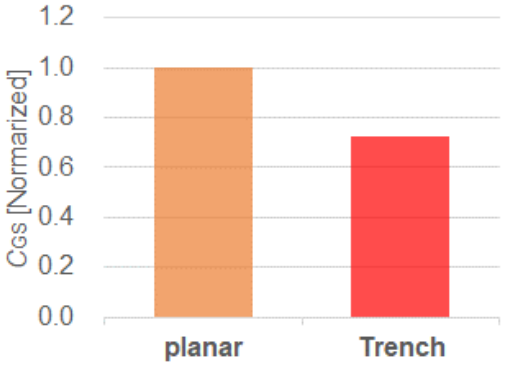

Figure 4-(b). C_{GS} Comparison (ROHM Planar vs Trench)

Measurement conditions: V_{GS}=0V, V_{DS}=800V, T_j=25℃

These parasitic capacitances are typically represented in MOSFET datasheet by three parameters: (I) Input capacitance (C_{iss}), (II) Output capacitance (C_{oss}), (III) Miller capacitance (C_{rss}). These are important parameters that affect the switching characteristics of the device.

(I). Input capacitance: C_{iss} = C_{GD}+C_{GS}

To turn MOSFET on/off, C_{iss} must be charged/discharged, which affects the delay times. The charge required to charge C_{iss} is Q_g.

(II). Output capacitance: C_{oss} = C_{DS} + C_{GD}

C_{oss} affects the turn-off properties. Larger C_{oss} require more time to charge C_{oss} when turned off, which increases the turn-off time.

(III). Miller capacitance: C_{rss} = C_{GD}

C_{rss} affects the switching rate. If C_{rss} is large, the drain-source voltage turns on and turns off longer. C_{oss}, C_{rss} are also dependent on the drain-to-source voltage V_{DS}. As shown in Figure 5, increasing V_{DS} tends to reduce the C_{oss}, C_{rss} capacitance values.

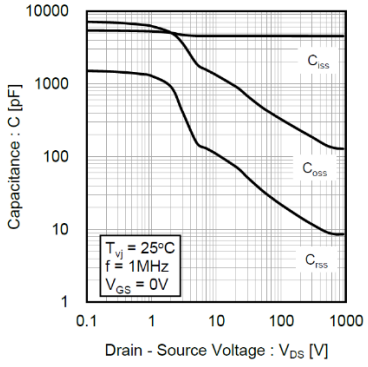

Figure 5. ROHM's 4G SiC MOSFET Capacitance vs. drain-source voltage

1.4 Gate charge characteristics

The gate-charge characteristic of SiC MOSFET should be considered while designing a gate drive circuit to properly determine the driver's current source and sink capability. The gate charge is the required amount of charge, or the current in each period, in order to charge and discharge the input capacitance C_{iss}. The gate voltage transition from low to high can be divided into three main periods as shown in Fig.6.

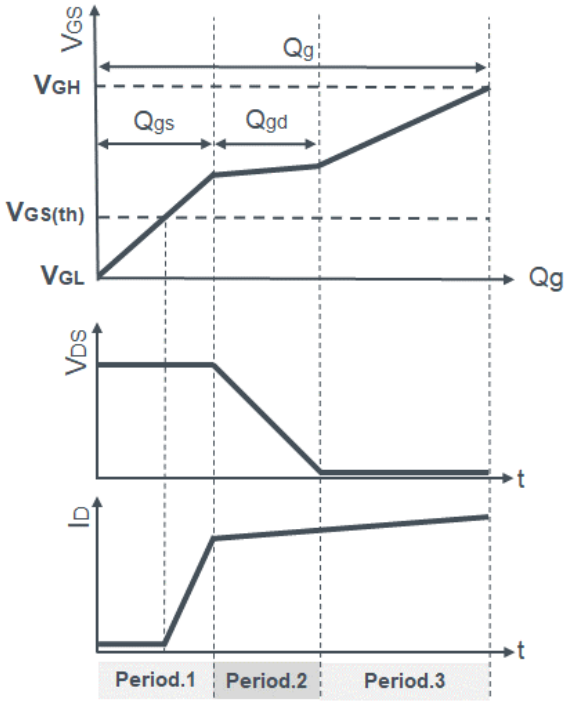

Figure 6. Gate Charge and Drain-Source Voltage/Current

Period.1

This is the period for the gate voltage to rise and reach the threshold voltage. The gate-source capacitance C_{GS} is charged to increase the gate voltage. The current begins to flow between the drain and source after $V_{GS(th)}$ is exceeded. The drain-source voltage (V_{DS}) also falls after the drain current is increased.

Period.2

This period is known as Miller plateau region, where C_{GD} is charged, V_{DS} drops, and the gate voltage is constant. The gate voltage at this period is defined as Miller plateau voltage.

Period.3

The switching operation is complete when C_{GD} voltage is equal to C_{GS} voltage, the drain-source voltage does not change, C_{GS} and C_{GD} charge start again, and the gate voltage starts to increase.

To increase the rate at which the drain-source voltage changes, either select a device with a smaller C_{GD} or increase the current discharged into the C_{GD} to shorten the miller duration.

2. Considerations in gate drive design

As a case study, synchronous-rectification BOOST circuit is used to explain prospective issues that may occur while switching SiC MOSFETs. The circuit of the synchronous-rectification BOOST is shown in Figure 7.

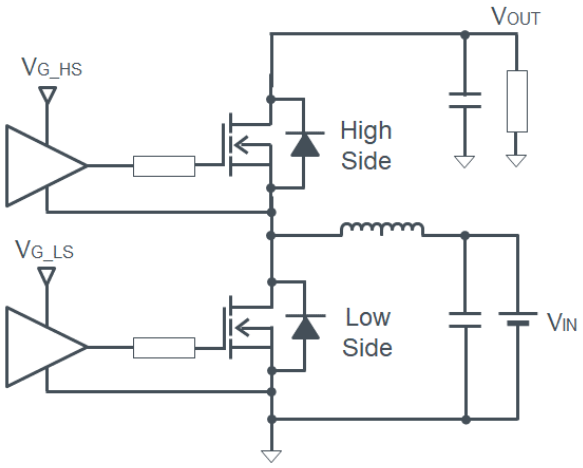

Figure 7. synchronous BOOST-circuit

2.1 Power loss

The power loss (P_{LOSS}) that occurs in devices that drive an inductor load is a switching loss (E_{on}/E_{off}) caused by overlapping voltage and current during the turn-on and turn-off switching phases, shown in Figure 8. On the other hand, conduction loss (E_{COND}) is determined by the device's on-resistance and the current flowing during the on-phase. The power-loss P_{LOSS} can be calculated

$$P_{\mathrm{LOSS}} = (E_{\mathrm{on}} + E_{\mathrm{off}} + E_{\mathrm{COND}}) \times f_{\mathrm{SW}} \cdots (1)$$

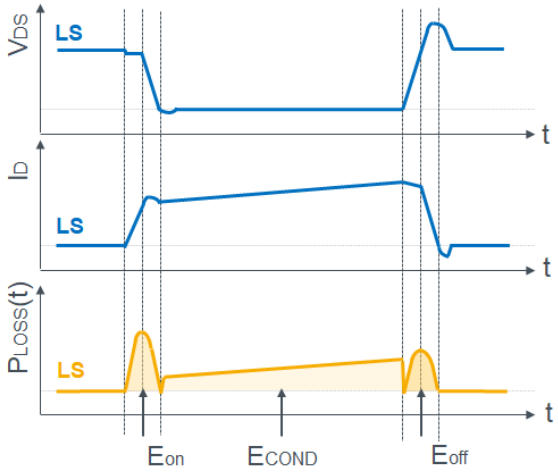

Figure 8. device-loss wave form

One way to reduce power loss is to reduce the switching frequency. However, reducing the switching frequency in certain applications may not be a feasible solution. Therefore, the gate drive circuit can be used to reduce the power loss. Figure 9 shows the relationship between the gate resistance value vs turn-on & turn-off losses (E_{on} and E_{off}). Figure 10 shows the relationship between the gate resistance (R_{G_EXT}) vs the switching speed (dV/dt). From Figure 9, it can be observed that low R_{G_EXT} value reduces both turn-on and turn-off switching loss. This is due to the fact that V_{DS} slew rate is higher by reducing R_{G_EXT} and increasing the switching speed (dV/dt) as shown in Figure 10.

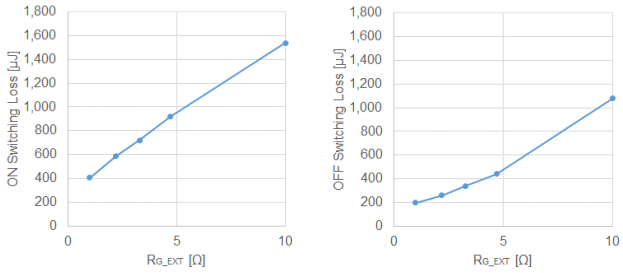

Figure 9. R_{G_EXT} vs. E_{SW}

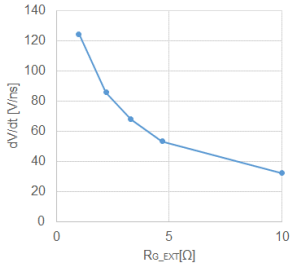

Figure 10. R_{G_EXT} vs. dV/dt

2.2 Drain-source turn-off surge voltage

When MOSFET of Low Side is turned off, the drain-source voltage V_{DS} rises to the output voltage (V_{OUT}), but a surge voltage is generated due to the inductance component of the current flow path.
To suppress V_{DS} surge-voltage, a snubber circuit may be utilized between the drain and source. Another solution is to increase the external gate resistor R_{G_EXT} value to reduce the switching speed. Figure 11 shows the drain-source-voltage waveforms at different values of R_{G_EXT}.

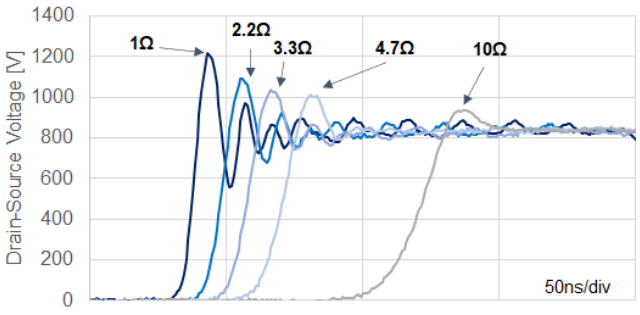

Figure 11. V_{DS} surge waveforms at different R_{G_EXT}

2.3 Positive and negative surge gate-source voltage

While changes in V_{DS} and I_D are often a focus point, it's important not to overlook their impact on the gate-source voltage ($V_{GS\text{-}HS}$). A brief overview of this analysis is provided in this application note, with more in-depth information available in reference [1].
The equivalent circuit representing the turn-on behavior of the low side MOSFET (hereafter LS) is shown in Figure 12 and the waveforms are depicted in Figure 13. When LS turns on, I_D changes first. Since LS's I_D is increasing and I_D of High Side (hereafter HS) is decreasing, during event (I) power is generated with polarity indicated in Figure 12 (I). The current generated by this electromagnetic current charges $C_{GS\text{-}HS}$ with the source-side as positive, so in HS $V_{GS\text{-}HS}$ is pulled to the negative side and appears as a negative surge. When I_D changes, the potential of V_{DS} on LS decreases. As shown in event (II) in Figure 13, each HS, LS "voltage rises in the positive direction" occurs in $V_{GS\text{-}HS}$. Therefore, the turned-off HS may experience a parasitic turn-on (PTO) due to the rise in $V_{GS\text{-}HS}$, which overlaps with the turn-on operation of LS causing the through current to flow. The charge current to

C_{GS} continues to flow until the turn-on operation is complete, and the energy is stored in L_{G_HS}, but disappears when V_{SW} change is complete, and L_{G_HS} generates a power as shown in event (III) in Figure 12. Due to this electromotive force, it can again be seen as a "negative surge".

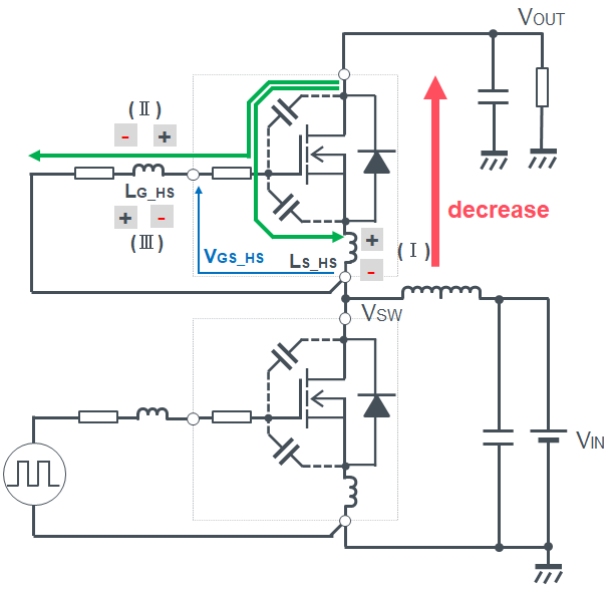

Figure 12. Equivalent circuit showing gate-source behavior during (LS turn-on).

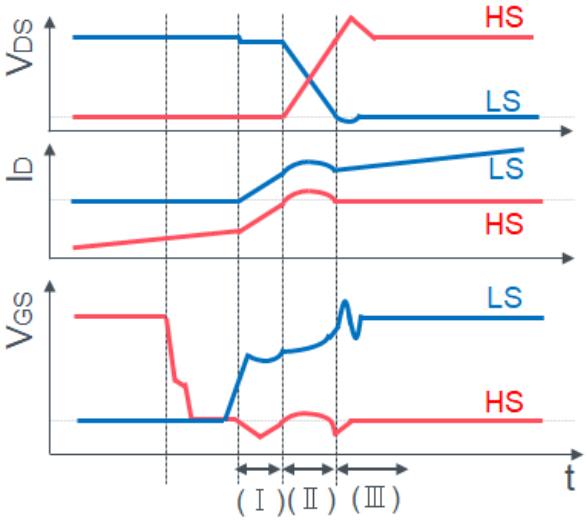

Figure 13. Waveforms (V_{DS} I_D V_{GS}) during (LS turn-on)

The equivalent circuit representing the turn-off behavior of the LS is shown in Figure 14 and the waveforms are depicted in Figure 15. Like turn-on, the numbers (IV), (V) and (VI) are assigned to distinguish the events. Compared to when turning on, the basic operation is the same as when the order of change between V_{DS} and I_D changes.

Turn-off	Turn	on
Event (IV) →	Event	(II)
Event (V) →	Event	(III)
Event (VI) →	Event	(I)

V_{GS} "Negative Surge" on HS becomes an event (IV). V_{GS} raised by the event (VI) is already near the end of the turn-off, and even if HS is in the turn-on operation, LS is turned off, which is of little consequence.

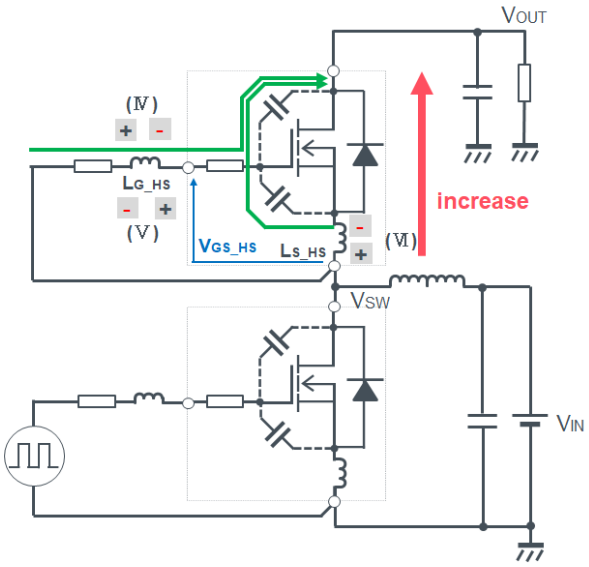

Figure 14. Equivalent circuit showing gate-source behavior during (LS turn-off).

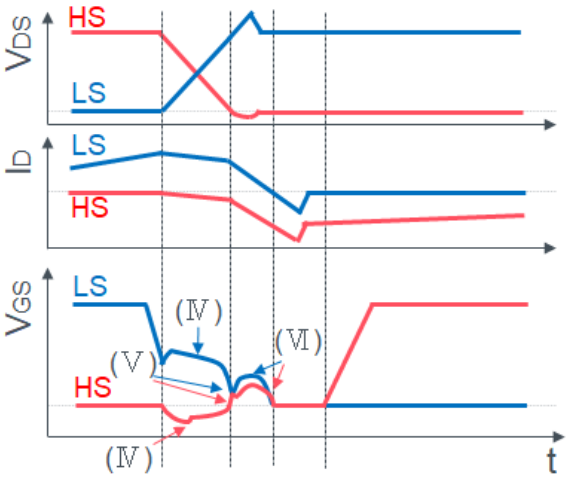

Figure 15. Waveforms(V_{DS} I_D V_{GS}) during (LS turn-off)

2.4 Parasitic turn-on (PTO) phenomenon

During turn-on (event II), unintentional turn-on may occur when the gate voltage rises above the gate threshold voltage $V_{GS(th)}$ due to the positive voltage rise. This is known as a parasitic turn-on (PTO). The positive voltage rise is dependent on the switching speed on LS and the gate resistor (R_{G_HS}) value. The lower the switching speed on LS and the lower the gate resistor (R_{G_HS}) on HS, the less that HS is prone to parasitic turn-on. Figure 16 shows the voltage (HS) gate-source voltage waveform when the drive (LS) is turned on at different values of R_{G_HS}. It can be observed that the larger the gate resistance (R_{G_HS}), the greater the voltage rise of the gate voltage as depicted in Figure 16-(a). On the other hand, Figure 16-(b) shows that the faster the switching by reducing the gate resistance (R_{G_LS}) on the drive side (LS), the higher the voltage rise of the HS gate voltage.

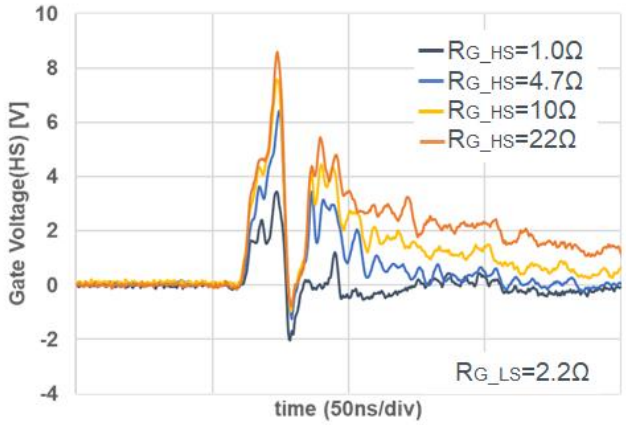

Figure 16-(a). Reflux side gate resistance and the reflux side gate voltage rise

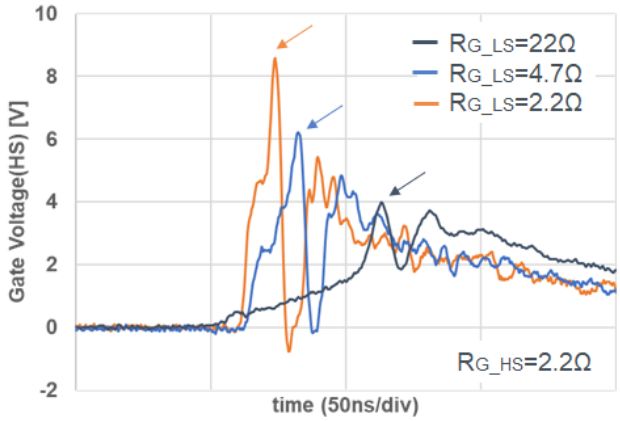

Figure 16-(b). Drive-side gate resistance and return-side gate voltage rise

If a parasitic turn-on occurs, the following four currents are observed for LS drain-source current, as shown in Figure 17.

① Normal turn-on current
② Recovery current of HS diode
③ Through current by parasitic turn-on
④ C_{oss} charge current

Therefore, it is very difficult to determine whether a parasitic turn-on is occurring. Since the waveform being evaluated also includes the effect of the device's internal resistor, it is not a good standard to simply judge whether the gated waveform has exceeded $V_{GS(th)}$.

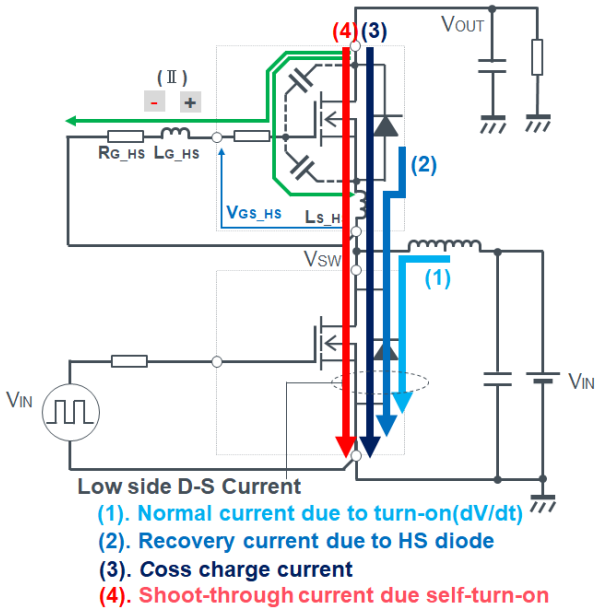

Figure 17. LS current at parasitic turn-on

Figure 18 shows a waveforms comparison when the return-side gating resistor (R_{G_HS}) is set at 1Ω and 22Ω. When R_{G_HS} is 22Ω, the gate-voltage increases and exceeds the threshold $V_{GS(th)}$ for approximately 10ns. At this time, it can be seen that parasitic turn-on result in a current increase resulting in a drop in V_{DS}, and a decrease in the peak. The drive-side drain-source current also increases.

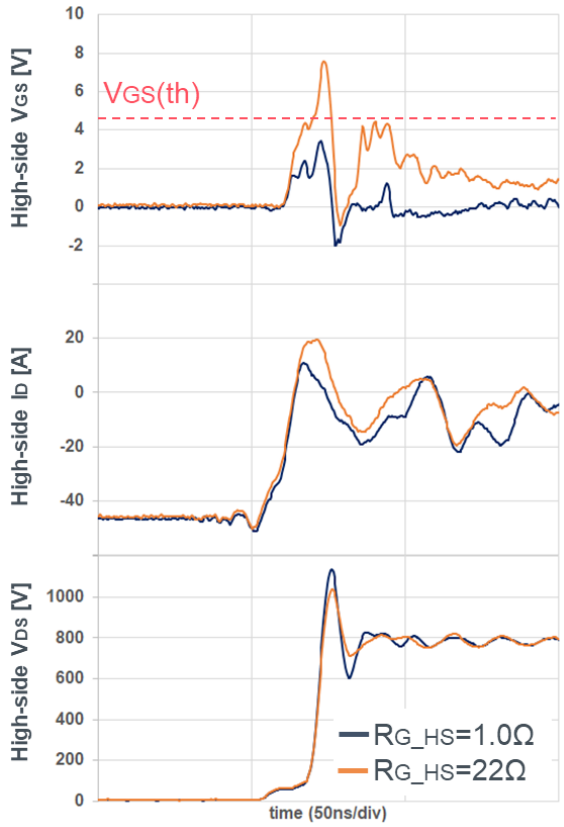

Figure 18. Waveforms with suspected PTO.

As shown in Figure 19, the recovery loss E_{RR} at turn-on (including the current waveform that appears to be parasitic turn-on) slightly increases with R_{G_HS} = 22Ω compared with switching loss. However, the turn-on loss (E_{on}) and turn-off loss (E_{off}) is almost not affected, and the impact of parasitic turn-on is considered to be minimal. If there is a suspicion of parasitic turn-on at room temperature, it can be confirmed by judging the switching loss at high temperature when $V_{GS(th)}$ is low, or by comparing the loss when a negative bias is applied and turn-off at 0V and no significant difference is found.

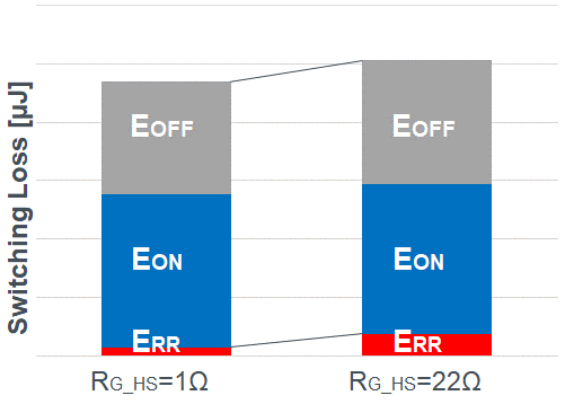

Figure 19. Switching-Loss Comparison by Changing Reflux-Side Gate Resistor

2.5 Generation of negative surge voltage

Figure 20 shows the reflux-side gate waveforms when the drive-side turn-off occurs with gate resistors and gate negative voltage settings. It can be confirmed that there is no effect of the gate negative surge caused by the gate negative voltage. The larger the gate resistance, the smaller the effect of negative surge.

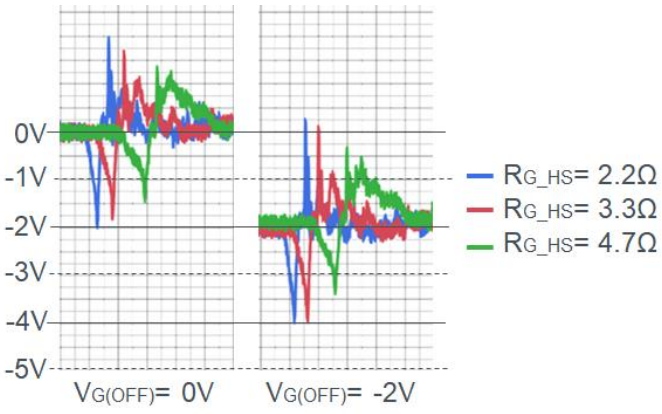

Figure 20. gate resistor and gate negative surge

3. Roles of the gate driver

When designing a gate drive circuit, it is necessary to understand the role of the gate driver. The main roles are shown below.

3.1 Driving capability

Recommended drive voltages for power devices vary by device and manufacturer. For ROHM's SiC MOSFET, we recommend 15~18V (V_{GH}) for the positive gate-source voltage and 0V (V_{GL}) for the negative gate-source voltage. The main source of the gate signal is the microcontroller (MCU), which is 5V/3.3V (DVDD's CMOS output). To optimally drive a power device, The gate driver raises the output to 15V or more to optimally drive the power device. This section shows a low-side gate driver circuit diagram to drive a power device as shown in Figure 21.

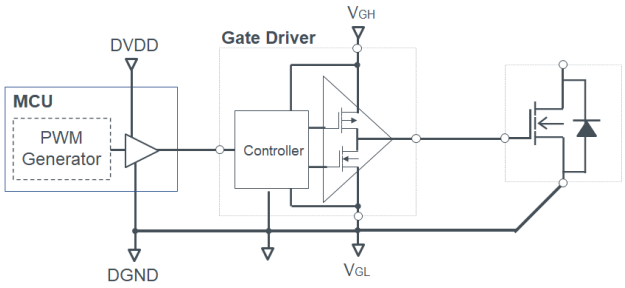

Figure 21. Schematic diagram of "Low-side" gate driver

3.2 High-speed switching

The microcontroller (MCU), which is the source of the gating signal, generally has a low current capability below 0.1A and cannot directly drive power devices. Assuming that the input capacitance of MOSFET is 5nF and that the output impedance of I/O port of the microcontroller is 500Ω, the time-constant t is given below.

$$t = CR = 5n \times 500 = 2.5\ [\mu s]$$

The gate turns on and off at a very slow rate, resulting in a large switching loss. Driving at high speed is also one of the roles of the gate driver in order to drive power devices optimally.

3.3 Level shift from the control circuit

Figure 22 shows a typical gate-driver that serves as a level-shift. MCU's GND potential, which is the source of the gate signal, and the source potential (V_{S_HS}, V_{S_LS}) of the power device almost differ. To apply the optimum gate-source voltage, the level of the MCU's signal must be shifted, which is one of the key roles of the gate driver.

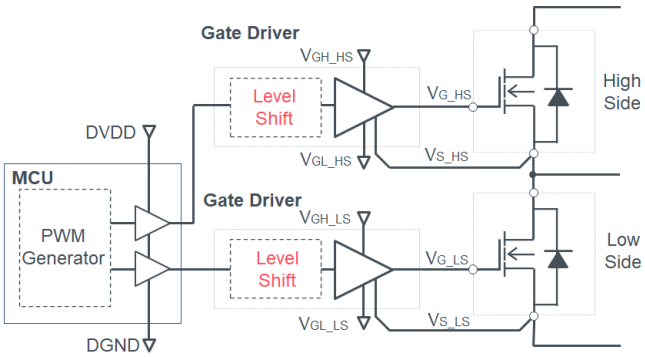

Figure 22. "Level-Shift" Gate-Drive Schematic

3.4 Isolate the control and power circuits

In applications using power devices, the bus voltage of the main circuit handles voltages of several hundred volts or more, and currents of several tens of amperes or more flow between the drain and the source of the power device. If there is no isolation between the control system and the power system, an electric leak may occur, and the insulation of the product itself may not be adequate. Furthermore, if failure occurs in the system, the electronic components may be damaged and the user may receive an electric shock. Figure 23 shows an isolated gate-drive schematic. Use of a gate-driver IC with isolation capabilities in this manner reduces the chance of an electric shock.

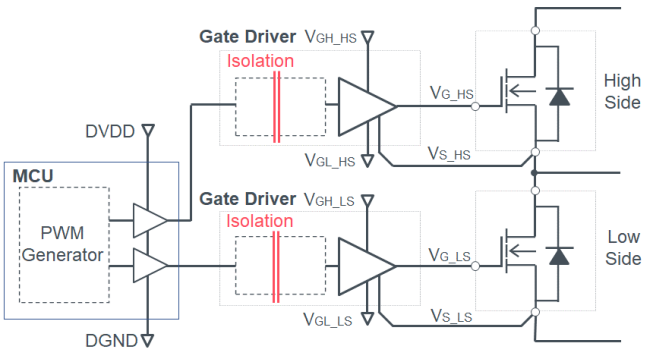

Figure 23. "Isolated" Gate-Drive Diagram Example

4. Design guidelines for gate drive circuits

The gate driver circuit consists of a gate driver and its peripheral circuits, but the gate driver is generally IC. In order to optimize the device, figure 24 shows the requirements that need to be fulfilled to select suitable gate driver IC. Furthermore, it is important to select the gate resistor, to design the gate drive voltage/current drive capability, and to design the protective circuit. The basic design items of the gate driver circuit are shown below.

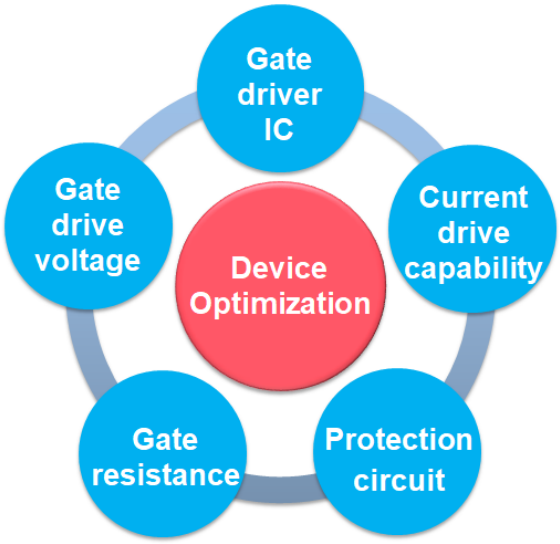

Figure 24. Designing elements of gate-drive circuitry

4.1 Selection of gate driver IC

The gate driver IC must be selected according to the application, such as 1ch (low side)/2ch (low side + high side) drive type, insulation type/non-insulation type, etc. Table 1 introduces the types of gate driver IC in the driving scenarios. This section shows an example of designing Figure25 when 2ch output-gate driver IC is used.

Table 1. Gate Driver Types and Functionals

Function	Type of gate driver IC		
	Low side	Level shift	Insulation type
Low-side drive	Yes	Yes	Yes
High side drive	None	Yes	Yes
Insulation	None	None	Yes

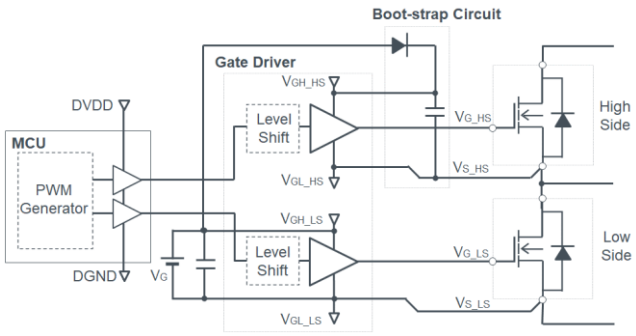

Figure 25. Schematic diagram using "2ch gate driver IC

There are also three types of isolation methods for gate-driver IC: photocoupler, magnetic, and capacitive.

✓ Photocoupler isolation: Consists of a light-emitting device (Light emitting) and a light-receiving element (Receiving). The current signal input to the photocoupler is converted into an optical signal by the internal element, allowing signals to be transmitted from the light-emitting side to the light-receiving side. (Figure 26)

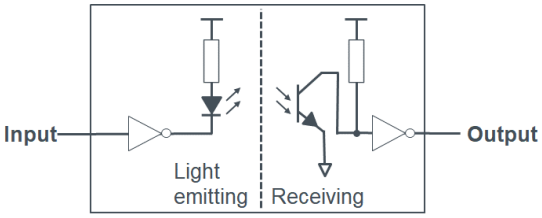

Figure 26. Photocoupler isolation

✓ Magnetic isolation: A coil is used on the input and output sides, and signals are passed between insulated coils. (Figure 27)

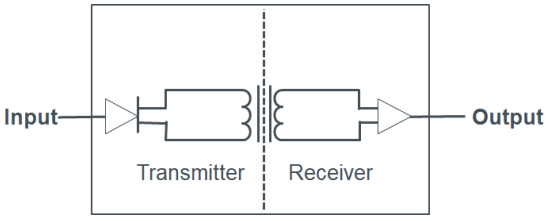

Figure 27. Magnetic isolation

✓ Capacitive isolation: An SiO_2 capacitor is used to isolate the input-side (Transmitter) from the output-side (Receiver), and AC is passed between the insulated capacitors as shown in Figure 28.

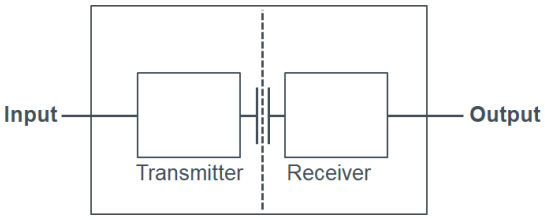

Figure 28. Capacitive isolation

Although the photocoupler system is inexpensive as shown in Figure 29, its lifetime is shorter than that of the magnetic and capacitive systems due to the aging of LED and encapsulation resins. This is a disadvantage of a slow communication rate. Magnetic and capacitive systems are called digital isolators, which are highly integrated and have a long life because they can be created on-chip. In product design, high reliability and long life are important. Recently, magnetic and capacitive methods have been widely adopted.

In addition, common-mode transient immunity (CMTI) must be considered as one of the factors for selecting an isolated gate driver. This is an index that ensures stable operation even when a large d*V*/dt occurs between the input and output of the gate driver IC during switching. When driving a SiC MOSFET, the drain-source d*V*/dt during switching is the speed of 40~90*V*/ns. Since CMTI is 50*V*/ns in the photocoupler method and the magnetic and capacitive methods are 100*V*/ns in the photocoupler method, we recommend that you select either the magnetic or the capacitive isolation in applications where SiC MOSFET, etc. are implemented and high-speed switching is expected. In this application note, the gate driver IC(BM61S41RFV made of insulated types and 1ch outputting ROHM) is selected for the magnetic method.

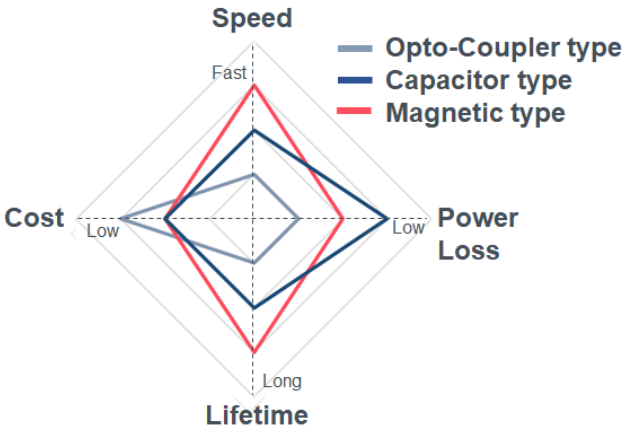

Figure 29. Characteristics of Gate Driver IC Isolation Method

4.2 Determination of gate drive voltage

When setting the gate-drive voltage for SiC MOSFET, refer to the recommended drive voltage in the datasheet. The recommended gate drive voltage depends on the structure and material of the device. Since SiC MOSFET gate-drive voltages are generally 15V~20V, care must be taken when replacing Si-MOSFET with SiC MOSFET. Figure 30 shows the on-resistance vs V_{GS} relationship for the ROHM's 4th generation SiC MOSFET and Si-MOSFET. It can be observed that the on-resistance of Si-MOSFET remains almost unchanged as long as the gate-source voltage is between 10~15V. However, when SiC MOSFET is driven below 15V, the on-resistance rapidly increases. Therefore, it is recommended to set the gate-source voltage above 15V to obtain a sufficiently low-on-resistance when using ROHM's 4th generation SiC MOSFET.

Care must also be taken that the gate drive voltage does not exceed the absolute maximum rating of the gate-to-source voltage. Even if the applied gate voltage is kept below the absolute maximum rating, a ringing voltage is generated by the gate inductance and capacitance, which can lead to the breakdown of the gate oxide layer.

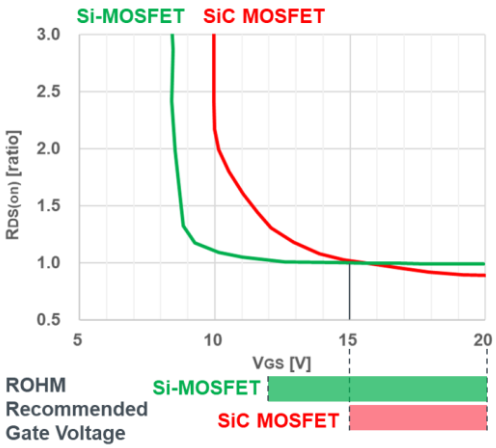

Figure 30. Relationship between V_{GS} and on-resistance

4.3 Investigation of Drive Current Capability of Gate Driver

Determine the switching device to be used, the gate resistance, and the gate drive voltage. You should then consider whether those constants actually have the drive capability to turn on/off at the desired time. When high-current modules/devices are connected in parallel, the input-capacitance C_{iss} is increased and the switching times are increased. As shown in Figure 31, a push-pull circuit is

designed by combining a NPN bipolar transistor and a PNP bipolar transistor. In push-pull circuits, when the gate driver IC is turned on, NPN bipolar transistor is turned on and current is supplied from V_{GH}, and when the gate driver is turned off, the current is sinked through PNP bipolar transistor. In this way, if the gate-driver IC has insufficient drive current capability, it can be compensated from a power supply with enough current-supplying capability.

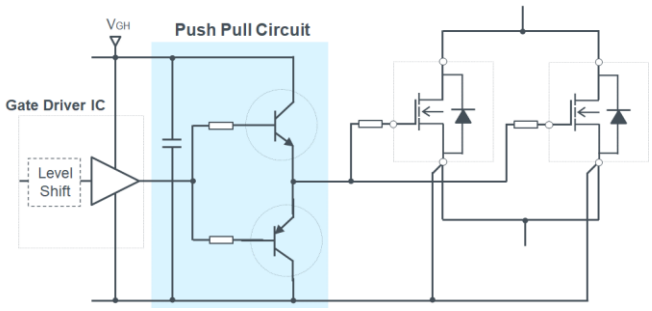

Figure 31. push-pull circuit

4.4 Power consumption of the gate drive circuit

This section explains the power consumed by the gate drive circuit. Figure 32 shows a gate driver using a gate driver IC.

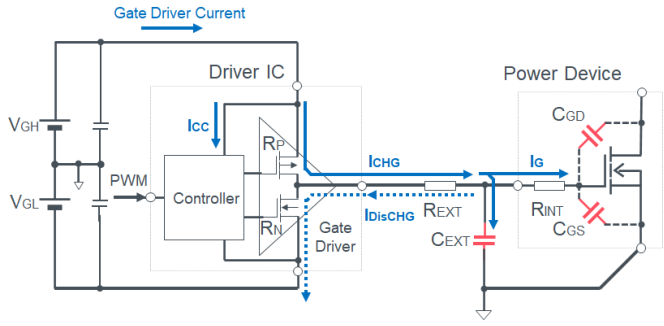

Figure 32. Gate driver circuit example

To turn on the gate, you need to charge the gate-to-source capacitor (C_{EXT}) as well as the input capacitance C_{iss} (C_{GS}+C_{GD}). In addition, to turn off the device, the gate charge must be discharged. Figure 33 describes the equivalent circuit of the gate drive circuit shown in Figure 32, divided into turn-on and turn-off. as the charging current (I_{CHG}), the discharging current (I_{DisCHG}), and the current drawn in the gate-driver IC (I_{CC}).

R_P : On-resistance of complementary P-type MOSFET in gate driver.

R_N : On-resistance of complementary N-type MOSFET in gate driver.

R_{EXT} : External gate resistor in Figure 32.

R_{INT} : Internal gate resistor in Figure 32.

Capacitive components are charged at turn-on. The power consumed by the resistor by the current flowing at that time is defined as P_{RES}.

The power consumption P_{GDR} of the gate drive circuit is the sum of the loss P_{RES} that occurs in R_P, R_{EXT}, R_{INT} during the process of charging a capacitive component (1), the power consumption P_{DisCHG} that occurs in R_{INT}, R_{EXT}, R_N when a capacitive component discharges when turning off ②, and the power P_{IC} that is consumed by the gate driver IC ③. Therefore, it can be expressed by Equation ②.

$$P_{GDR} = P_{RES} + P_{DisCHG} + P_{IC} \cdots (2)$$

Figure 34 shows the breakdown of power consumed. You can see that the loss that occurs in P_{CHG} is equal to the energy stored in the capacitive components.

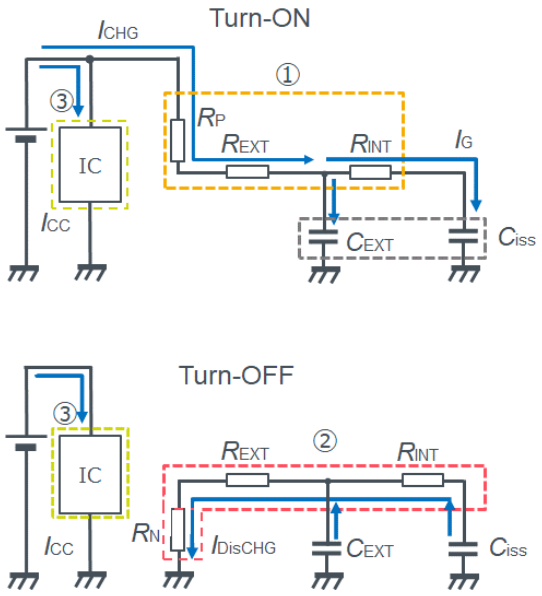

Figure 33. Equivalent gate-drive circuit at turn-on/turn-off

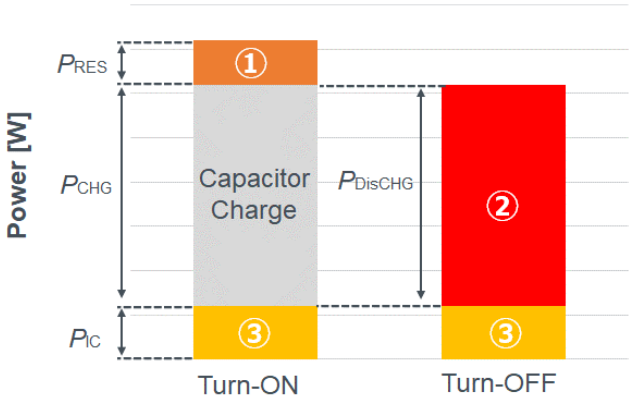

Figure 34. Breakdown of power consumption by gate-drive circuit

P_{RES} of power dissipated in the resistor when it is charged to its capacitance is given by Eq. 3.

$$P_{RES} = I_{CHG}{}^{2} \times (R_P + R_{EXT}) + I_G{}^{2} \times R_{INT} \cdots (3)$$

The energy charged to the capacitive component during turn-on is Eq. (4).

$$P_{CHG} = \frac{1}{2} \times \left(Q_g \times V_G + C_{EXT} \times V_G{}^{2}\right) \times f_{SW} \cdots (4)$$

Q_g : Total gate charge
V_{GH} : Turn on gate voltage
V_{GL} : Turn off gate voltage
The turn-on/turn-off voltage V_G is of the form (5).

$$V_G = V_{GH} + |V_{GL}| \cdots (5)$$

P_{DisCHG} is the power P_{CHG} charged during turn-on and consumed during turn-off, which leads to equation (6).

$$P_{DisCHG} = P_{CHG} \cdots (6)$$

The mean current I_{CHG} charged from the gate driver is given by Equation 7.

$$I_{CHG} = \frac{P_{CHG}}{V_G} = \frac{1}{2} \times \left(Q_g + C_{EXT} \times V_G\right) \times f_{SW} \cdots (7)$$

The average current I_G charged to the gated device is given by Equation (8).

$$I_G = \frac{1}{2} \times Q_g \times f_{SW} \cdots (8)$$

If the current supplied to the gate-driver IC is I_{CC}, P_{IC} becomes Equation (9).

$$P_{IC} = V_G \times I_{CC} \cdots (9)$$

4.5 Peak current of the gate drive circuit

The peak current I_{CHG_PEAK} of the gate drive is given by Eq. 10 when the gate driver ideally turns on instantaneously.

$$I_{CHG\_PEAK} = \frac{V_G}{R_P + R_{EXT} + R_{INT}} \cdots (10)$$

In practice, the gate driver also has a turn-on time. Figure 35 shows the ideal gate current waveform (t_{RISE}=0ns) and real waveform (t_{RISE}=20ns) when the gate driver turns on instantaneously at V_G=15V and gate resistors are 10Ω. According to (9), when a delay occurs, the peak-current drops. Although it is difficult to accurately calculate the peak current, it can be said that equation (9) represents the maximum value of the peak current.

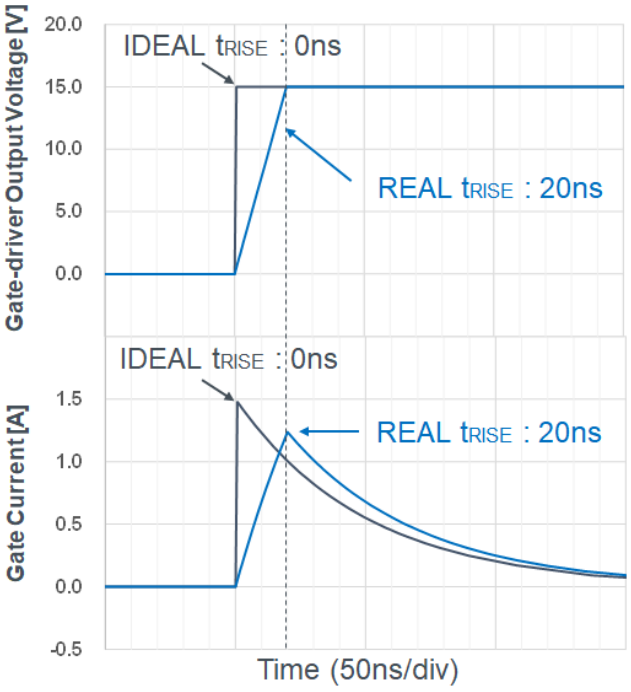

Figure 35. Relation between turn-on time and the gate current

4.6 Power dissipation of the gate drive IC

The power-consumption P_{DRV} of the gate driver IC is given by Equation (11) where the on-resistor of the power supply side of the drive stage of the gate driver IC is R_N to the on-resistor of R_P, GND side.

$$P_{DRV} = I_{CHG}{}^{2} \times R_P \times Duty + I_{CHG}{}^{2} \times R_N \times (1 - Duty) + I_{CC} \times V_G \cdots (11)$$

4.7 Selection of gate resistance

When determining the value of the gate resistance, select the optimal value from various factors. Figure 36 shows the effect of the gate-resistor on the circuit.

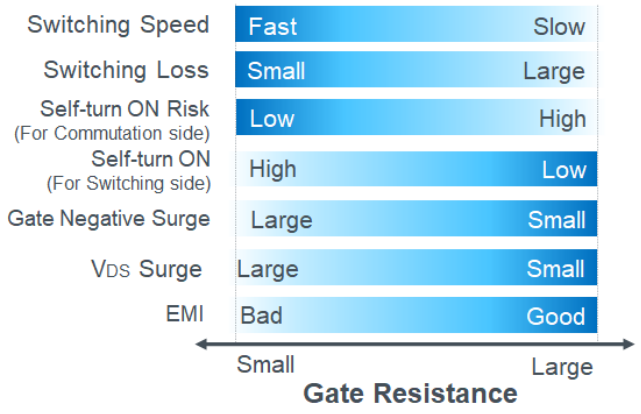

Figure 36. Effect of gate resistor on the circuit.

Reducing the gate resistance can reduce power dissipation by increasing the switching speed. However, it must be adjusted to an appropriate gate resistance because of risks such as increased surge-voltage and EMI. By using a diode as shown in Figure 37, it is possible to design a gate-resistor that differs in magnitude between turn-on and turn-off. If there is a margin of V_{DS} surge, the gate resistor at turn-off can be made smaller so that turn-off becomes faster. However, since the circuit becomes complicated, it is necessary to design with safety design and fail-safety in mind, including reliability and accidents in the event of failure.

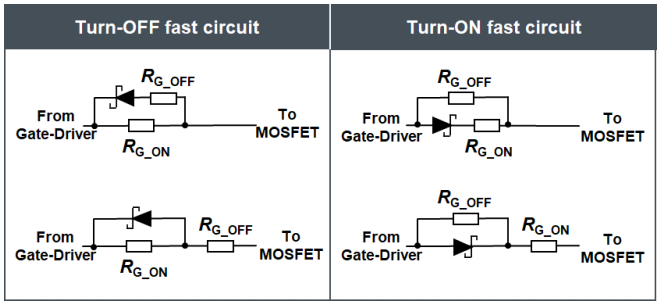

Figure 37. Implementation of a gate-resistor using diodes

When the switching speed changes due to changes in the gate resistance, the switching loss is affected. Use of a gate resistor that is too large for V_{DS} surge-suppression will reduce the turn-on and turn-off switching speeds and increase switching losses. The loss will raise the die temperature and the drain-source on-resistance will also increase because it has positive temperature coefficient, as shown in Figure 38. This leads to increased losses and increased on-resistance cycles that can lead to breakage. Therefore, it is necessary to select the optimum gate resistance value while paying attention to the loss.

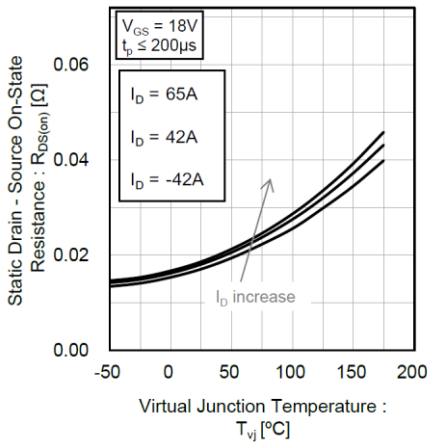

Figure 38. On-resistance vs Temperature for ROHM SiC MOSFET

4.8 Design of protection circuits

Described in detail in the application note "Gate-Source Voltage Surge Suppression Methods"*2. In applications utilizing SiC MOSFETs, it is crucial to consider the impact of voltage and current fluctuations during switching, including the inductance of the device's own package and peripheral circuit wiring. Neglecting these factors can lead to various issues, such as unanticipated positive or negative surges in the gate-source voltage. Figure 39 shows an example of a gate-source surge-proof circuit to avoid problems.

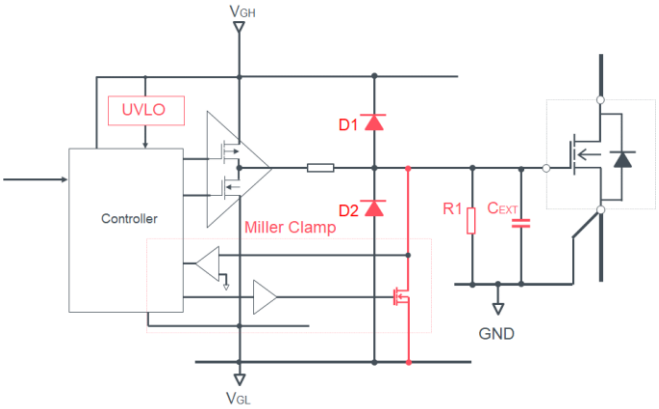

Figure 39. Protector Designs example

① Gate-to-Source Capacitance (C_{EXT})

When both the switching frequency and switching speed of SiC MOSFET are high, and assuming that the current flowing through the gate-to-drain capacitance C_{GD} is all flowing through the gate-to-source capacitance C_{GS}, the MOSFET gate-to-source voltage V_{GS} can be expressed as a voltage divider of the gate-to-drain capacitance C_{GD} and the gate-to-source capacitance C_{GS}, as shown in Equation 12.

$$V_{GS} \approx \frac{C_{GD}}{C_{GS}+C_{GD}} V_{DS} \cdots (12)$$

If a capacitive C_{EXT} is added between the gate and source as shown in Figure 39, the gate-to-source voltage V_{GS} is given by Equation 13.

$$V_{GS} \approx \frac{C_{GD}}{C_{EXT}+C_{GS}+C_{GD}} V_{DS} \cdots (13)$$

Therefore, it is possible to reduce the gate-source-voltage V_{GS} and reduce the risk of parasitic turn-on. However, large C_{EXT} also increase the loss. Therefore, the appropriate capacitance value should be carefully selected.

② **Positive surge clamp diode (D1)**

Implementing a diode-to-gate D1 across V_{GH} allows the voltage to be clamped by V_{GH}, suppressing positive surges. It is also recommended to use a Schottky Barrier Diode (SBD) because D1 must absorb tens of ns of impulses and be clamped as low as possible.

③ **Negative Surge Clamp Diode (D2)**

It is clamped to V_{GL} when a negative surge occurs due to a diode (D2) between the gating V_{GL}. D2 recommends the use of Schottky Barrier Diodes (SBD) as well as D1.

④ **Miller clamp (MC) circuit (Q1)**

By turning on MOSFET for Miller clamping while the device is turned off, V_{GS} is connected to 0V and the gate-potential is clamped to ground. As shown in Figure 40, to implement a Miller clamp circuit, a control signal is required to drive MOSFET for Miller clamp. Control signaling requires monitoring V_{GS} during turn-off to find the driving timing. This is often provided in gate-driver IC. In this application note, the selected gate driver IC (BM61S41RFV-C) includes a built-in Miller clamp circuit.

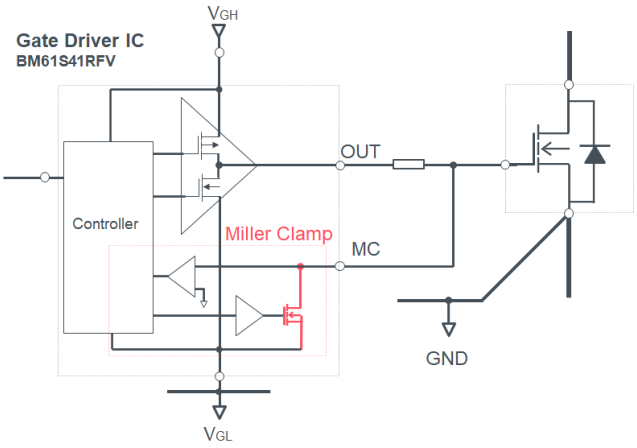

Figure 40. Sample Circuit of IC with Built-in Miller Clamp Circuit

⑤ **Undervoltage detection (UVLO)**

If MOSFET is turned on while the power supply voltage (V_{GH}) of the gate drive is not sufficiently rising, the on-resistance will be high, which may lead to heat generation or damage. When the power supply voltage is monitored and a low voltage is detected, there is a gate driver IC equipped with a control circuitry that does not turn on the gate. The gate driver IC(BM61S41RFV) described in this application note has a UVLO function.

⑥ **Gate-source resistor (R1)**

Connect a resistor between the gate and source to fix the gate potential when the gate power supply is off.

5. Design example of a gate drive circuit

5.1 ROHM SiC MOSFET SCT4018KR

The gate drive circuit design conditions are as follows. The gate driver IC uses a ROHM's BM61S41RFV-C suitable for driving SiC MOS at high speeds with 1ch isolation types with Miller clamping capability.
The turn-on gate voltage (V_{GH}) is 18V and the turn-off gate voltage (V_{GL}) is 0V. The gate-resistor (R_{EXT}) is 4.7Ω.

Circuit Design	Power Device (SiC MOSFET: SCT4018KR)	Gate Driver IC (BM61S41RFV-C)
• V_{GH}=18V • V_{GL}=0V • C_{EXT}=100pF • f_{SW}=50kHz	• C_{iss}=4.5nF • R_{INT}=1Ω	• ICC=0.7mA • R_P=0.67Ω typ. • R_P=0.30Ω min. • R_N=0.45Ω typ. • R_N=0.15Ω min.

The gate-voltage V_G can be calculated from equation (5).

$$V_G = V_{GH} + |V_{GL}| = 18 + |0| = 18[V]$$

Total Gate Charge (Q_g) is170nC at V_{GS}=+18V as mentioned in the datasheet and depicted in Figure 41.

$$Q_g = +Q_g + |-Q_g| = 170n + 0 = 170n\ [C]$$

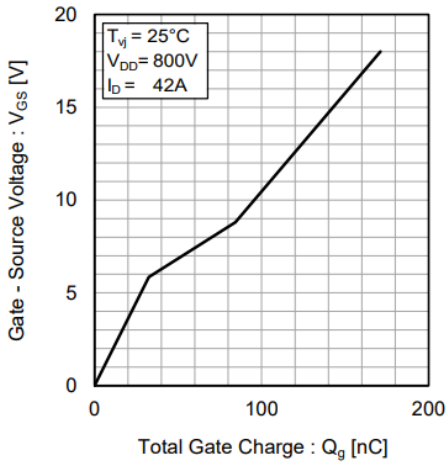

Figure 41. ROHM SiC MOSFET SCT4018KR Q_g vs. V_{GS}

P_{CHG} of power charged to the capacitive components during switching is calculated from equation (4).

$$P_{CHG} = \frac{1}{2} \times (Q_g \times V_G + C_{EXT} \times {V_G}^2) \times f_{SW}$$
$$= 0.5 \times (170n \times 18 + 100p \times 18^2) \times 50k$$
$$= 77\ [mW]$$

P_{DisCHG} of power consumed by the energy discharged from the capacitive components during turn-off is calculated from equation (4).

$$P_{DisCHG} = P_{CHG} = 77\ [mW]$$

The average current I_{CHG} can be calculated according to Equation (7) as follows:

$$I_{CHG} = \frac{P_{CHG}}{V_G} = \frac{1}{2} \times (Q_g + C_{EXT} \times V_G) \times f_{SW}$$
$$= 0.5 \times (170n + 100p \times 18) \times 50k$$
$$= 4.3\ [mA]$$

From Equation (8), the average current I_G

$$I_G = \frac{1}{2} \times Q_g \times f_{SW} = \frac{1}{2} \times 170n \times 50k = 4.3\ [mA]$$

While actually operating the device, consider the optimal gate resistance based on the gate resistance factors shown in Figure 36. The surge waveform of V_{DS} should be below the breakdown voltage. Figure 42 shows the characteristics of gate-resistor R_{EXT} and V_{DS} surges. V_{DS} surge on Figure 42 turn-on graph is the surge on the commutation side, and the turn-off graph is V_{DS} surge on the drive side. Figure 43 shows the gate-resistor R_{EXT} and switching-loss properties.

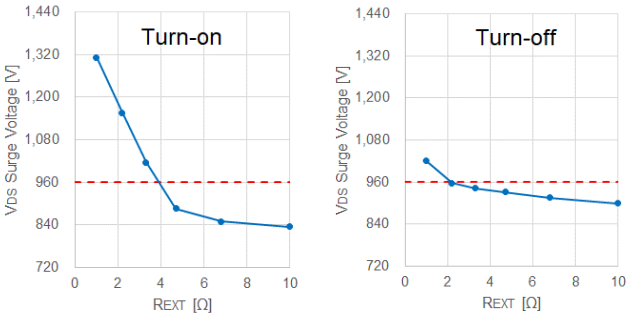

Figure 42. R_{EXT} vs V_{DS} Surge Voltage

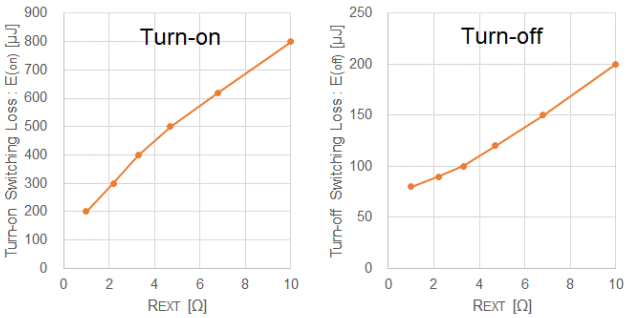

Figure 43. R_{EXT} vs. Switching Loss

If the derating is 80% of the absolute max. rated 1,200V, V_{DS} surge must be kept below 960V by adjusting the gate-resistance. When the gate resistance is low, the switching loss becomes small, but in order to reduce V_{DS} surge to less than 960V, a gate resistance of about 4Ω or more at turn-on and about 2Ω or more at turn-off must be selected.

A resistor of 4.7Ω is selected as shown in Figure 44 to realize a low gate-resistance at turn-off.

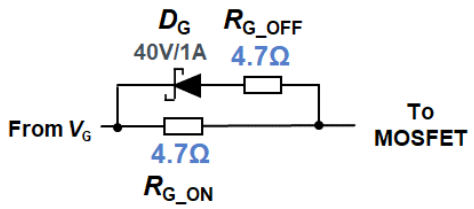

Figure 44. selected gating resistor

The power dissipation P_{RES} generated by the resistor when

the capacitance is charged on the turn-on is given by Equation (3):

$$P_{\mathrm{RES}} = {I_{\mathrm{CHG}}}^2 \times (R_{\mathrm{P}} + R_{\mathrm{EXT}}) + {I_{\mathrm{G}}}^2 \times R_{\mathrm{INT}}$$
$$= (4.3m)^2 \times (0.67 + 4.7) + (4.3m)^2 \times 1$$
$$= 0.117\ [mW]$$

From Equation 8, the power dissipation of the gate driver IC can be calculated.

$$P_{\mathrm{IC}} = V_{\mathrm{G}} \times I_{\mathrm{CC}}$$
$$= 18 \times 0.7m$$
$$= 12.6\ [mW]$$

The power dissipation P_{GDR} of the gate-driver is calculated from Equation (2):

$$P_{\mathrm{GDR}} = P_{\mathrm{RES}} + P_{\mathrm{DisCHG}} + P_{\mathrm{IC}}$$
$$= 0.117m + 77m + 12.6m$$
$$= 90\ [mW]$$

The peak-current $I_{\mathrm{CHG\_PEAK}}$ of the gate-drive is calculated from Equation 10. From the datasheet of the gate driver IC, minimum value of the output resistance R_{P} of the charge-side transistor is 0.3Ω, and minimum value of the output resistance R_{N} of the discharge-side transistor is 0.15Ω. Therefore, the largest peak current is calculated at discharge.

$$I_{\mathrm{CHG\_PEAK}} = \frac{V_{\mathrm{G}}}{R_{\mathrm{N}} + R_{\mathrm{G\_EXT}} + \mathrm{R_{G\_INT}}}$$
$$= \frac{18}{0.15 + \frac{4.7}{2} + 1} = 5.14\ [A]$$

The discharging time t_{DisCHG} is calculated from the time constant expression.

$$t_{\mathrm{DisCHG}} = \frac{Q_g + C_{\mathrm{EXT}} \times V_{\mathrm{G}}}{\mathrm{I_{CHG\_PEAK}}} = \frac{170n + 100p \times 18}{5.14} = 33.4[ns]$$

When a square wave with a time constant like a Figure 45 is converted into a pulse, it is calculated by the peak current 5.14A and pulse duration (t/2)16.2ns).

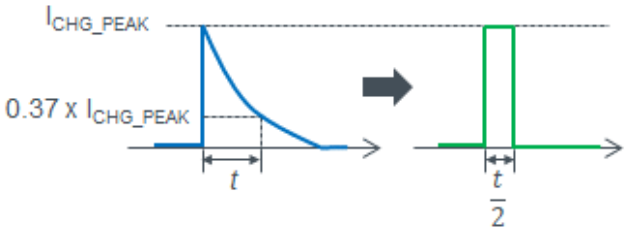

Figure 45. Pulse-conversion of a square wave with Time-Constant

$$Duty = t \times f_{SW} \times 2 = 33.4n \times 50k \times 2 = 0.0033$$

From Figure 46, the resistor's consecutive pulse power limit is approximately 13W.

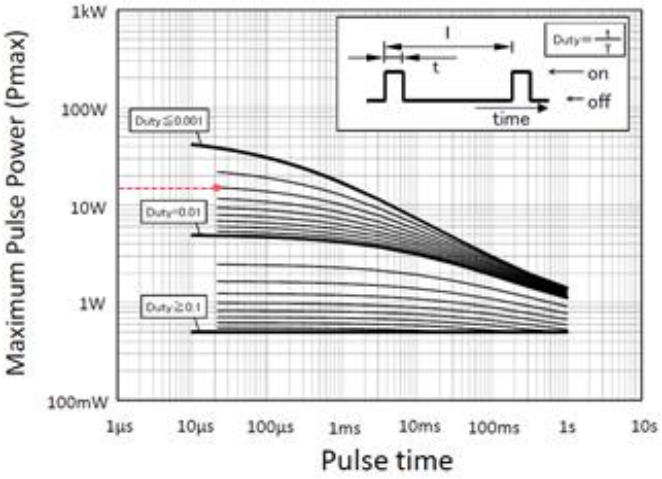

Figure 46. Consecutive pulse limiting power.

The pulse rated voltage of the resistor is calculated from the following formula.

$$V_{\mathrm{R\_MAX}} = \sqrt{P_{\mathrm{max}} \times R} = \sqrt{13 \times 4.7} = 7.81\ [V]$$

The peak-voltage $V_{\mathrm{R\_PEAK}}$ generated in the gate-resistor is:

$$V_{\mathrm{R\_PEAK}} = \frac{I_{\mathrm{CHG\_PEAK}}}{2} \times R = \frac{5.14}{2} \times 4.7 = 12.09\ [V]$$

Since $V_{\mathrm{R\_MAX}}$=7.81V exceeds the pulse-rated voltage, the gate resistor should be set to 4.7Ω in 2-series and 2-parallel. $V_{\mathrm{R\_MAX}}$ and $V_{\mathrm{R\_PEAK}}$ are calculated as follows:

$$V_{\mathrm{R\_PEAK}} = \frac{I_{\mathrm{CHG\_PEAK}}}{4} \times R = \frac{5.14}{4} \times 4.7 = 6.04\ [V]$$

You were able to drop below the rated-voltage $V_{\mathrm{R\_MAX}}$=7.81V.

The power dissipation of the gate drive circuit is a 90mW, and the power supply of the gate drive circuit must be designed to have a power rating equal to or greater than 90mW and have no effect on the steep loading variation of the max. 5.14 A/33 ns range.

The power P_{DRV} of the gate-driver IC is calculated as follows from Equation (11) as Duty50%.

$$P_{\mathrm{DRV}} = {I_{\mathrm{CHG}}}^2 \times R_{\mathrm{P}} \times Duty + {I_{\mathrm{CHG}}}^2 \times R_{\mathrm{N}} \times (1 - Duty)$$
$$+ I_{\mathrm{CC}} \times V_{\mathrm{G}}$$
$$= (4.3m)^2 \times 0.67 \times 0.5 + (4.3m)^2 \times 0.45 \times (1 - 0.5)$$
$$+ 0.7m \times 18$$
$$= 12\ [mW]$$

Since the packaged power P_{d} is P_{d}=694mW from the thermal resistance of 180°C/W, it was confirmed that the heat generation of the gate-driver IC is acceptable.

For the gated resistor (R_{EXT}) power P_{R_EXT},

$$P_{R\_EXT} = {I_{CHG}}^2 \times R_{EXT} = (8.6m)^2 \times 4.7$$
$$= 0.325\ [mW]$$

ROHM withstanding surge resistance: When ESR10 is selected, the rated power is 250mW and the mean power is no issue. However, instantaneous heat generation is accumulated by the pulse power, so perform thermal measurement evaluation to judge.

Figure 44 turnoff diode (D_G) is selected as 40V/1A.

Figure 47 shows an example of the gate-drive circuit diagram when ROHM SiC MOSFET SCT4018KR is mounted, which was examined in the design example.

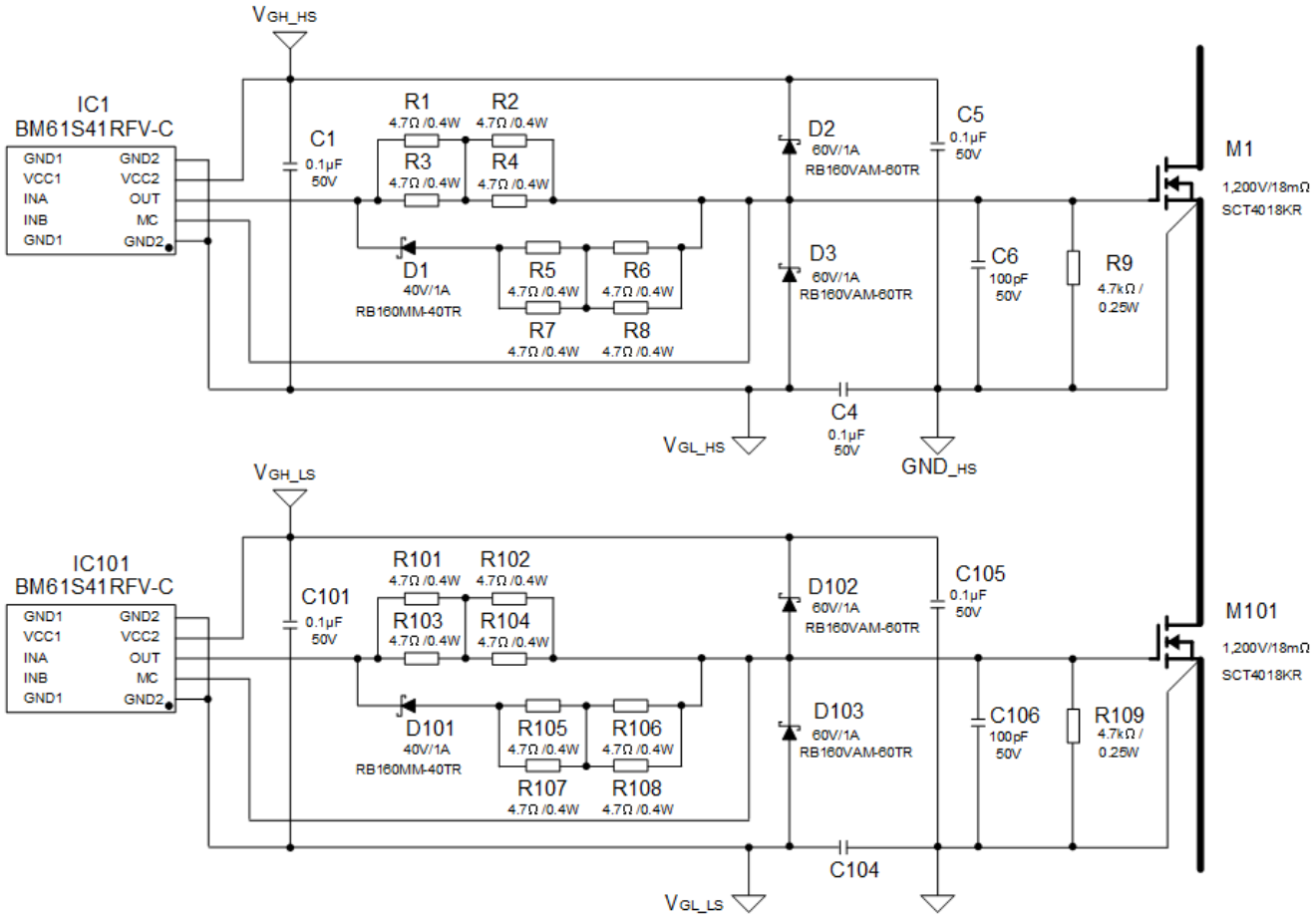

Figure 47. SCT4018KR Gate-drive circuit diagram example

6. Summary

As switching speeds continue to increase with the adoption of SiC MOSFETs, the risks of issues such as drain-source surges and parasitic turn-on also rise. A comprehensive review of gate-drive designs is essential to mitigate problems and harness the full potential of SiC MOSFETs. The gate drive circuit design guidelines and protective circuit examples presented in this application note are expected to be valuable resources for optimizing gate drive circuit design.

Reference materials

*1 "Gate-Source Voltage Behavior in Bridge Configuration"

Application Notes (No. 60AN134J Rev.002)

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*2 "Gate-Source Voltage Surge Suppression Methods"

Application Notes (No. 62AN009J Rev.002)

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