SiC MOSFET

Oscillation countermeasures for MOSFETs in parallel

In recent years, the trend toward larger currents in applications such as industrial equipment and xEV has led to paralleling power devices embedded in inexpensive discrete packages. By connecting MOSFETs in parallel, the current flowing through individual devices is reduced which better distributes the heat generated from the devices. However, individual devices have characteristic variations. Therefore, when MOSFETs are connected in parallel and operated simultaneously, it is difficult to perfectly synchronize the operation of each device. Therefore, for using paralleled devices, attention must be paid to driving methods. This application note describes parallel-connected SiC MOSFET oscillations in detail, based on measurement results, and provides guidelines for PCB layouts, including driving circuits. *1

Contents

*1: In this application note, we will explain the operation when two MOSFETs are connected in parallel. In case the number of parallels increases, unexpected situations due to variations in each device cannot be avoided. Therefore, when connecting them in parallel, please evaluate them thoroughly and judge whether they can be used or not. In addition, since the characteristic variation of the device is inevitable, it is recommended to utilize designs with a single device as much as possible.

1. Board for parallel connection

Figure 1-1 shows a schematic of the circuit created for evaluating parallel-connected MOSFET devices. MOSFETs are connected in parallel with the high side and low side arms, and ON/OFF with a single driving signal. Figure 1-2 shows the picture of the created circuit board.

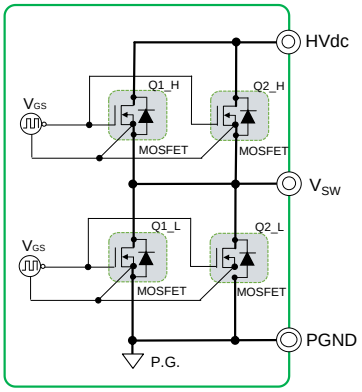


Figure 1-1. Simplified diagram of PCB008P

Figure 1-2. PCB008P (top view)

2. Gate driving circuit in parallel connection

When connected in parallel, the gate driving circuit is usually designed with one gate driver for two or more MOSFETs. Figure 2-1 shows the reference circuit. In Figure 2-1, the precautions are shown briefly. Therefore, the component circuits, etc. must be set according to the characteristics of used MOSFETs.

The following three steps are suggested for driving paralleled switches.

1. Check the output current of the gate driver. If the gate drive output current is insufficient to drive Q1 and Q2, add a buffer circuit by using Q3 and Q4. PCB008P uses a bipolar transistor (ROHM part numbers 2SCR542P and 2SAR542P) to amplify the driving gate current to a maximum of 10A.
2. To provide an opportunity to make the switching of Q1 and Q2 uniform, always insert separate gate resistors R_G_Q1 and R_G_Q2 in addition to the common gate resistor R_G_com. Later, in this application note, "5. Oscillation Evaluation Results" and "6. Verifying of Oscillation Countermeasures" will justify this recommendation. In PCB008P, R_G_com was set to 4.7 Ω, R_G_Q1, and R_G_Q2 were set to 2 Ω.
3. For gate drivers with a mirror clamp (MC), please monitor the proximity of the gate rather than R_G_Q1 and R_G_Q2, and connect to MC pin using a diode D1, D2 so that a dot-OR circuit (a circuit that connects via a diode and enables a higher-voltage signal) is formed. When Q1 and Q2 are connected in this way, the surge voltage of the gate can be suppressed during the commutation operation. R2 and R3 regulate the current flowing through MC pins. R2 and R3 is set to 0 Ω in PCB008P. I

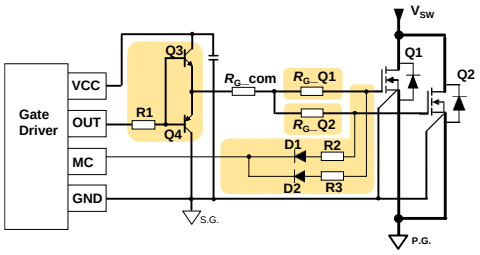


Figure 2-1. Gate driving circuit for low-side devices

You can also use one gate driver for each MOSFET. In this case, oscillation does not occur in the current path described in this application note. However, since MOSFET characteristics variation is included in ON/OFF in addition to the gate driver characteristics variation, the switching can be asynchronous and one of MOSFETs could be overloaded. Therefore, designs with smaller variations are required. Also, if the outputs of the gate drivers are connected directly to each other in order to match the timing, one of the gate drivers could become ON due to the variation of the gate drivers as shown in Figure 2-2, and either of them could become OFF, causing the gate voltage on ON side and GND on OFF side to be short-circuited, which could damage the gate drivers. Therefore, do not connect the outputs of the gate drivers to each other.

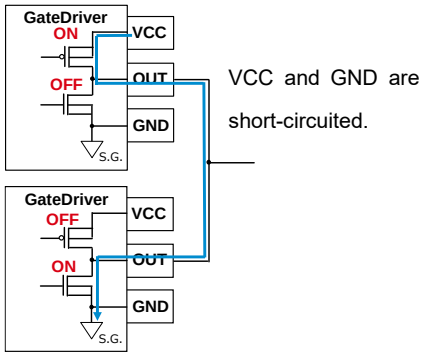


Figure 2-2. Short circuit between gate drivers due to direct connection of output of gate drivers

3. Oscillation factors in parallel connection

Oscillation that occurs in parallel connection is triggered by a deviation in the timing of each device's operation. The current is flowing in one MOSFET when ON or OFF is timing-shifted due to unbalance of the layout or variation of MOSFET itself, and the induced electromotive force generated in the parasitic inductance of the layout differs between each MOSFET, creating an electric potential difference. This electric potential difference interacts with parasitic capacitances, causing the oscillation phenomena. Figure 4-1 displays pertinent parasitic elements.

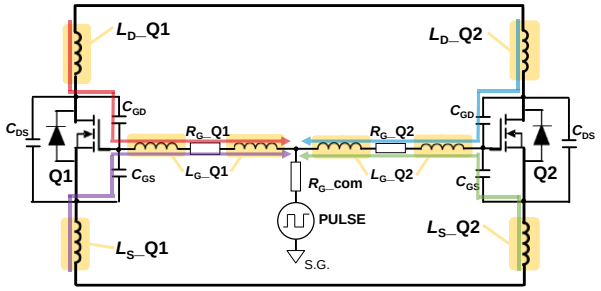


Figure 4-1. Oscillation path

If the amplitude of this oscillation becomes large, there is a possibility to cause damage. In addition, even if the oscillation noise of the gate pin does not exceed V_{GS} rating, it is possible that standard EMC limits will be violated. Therefore these oscillations must be suppressed as much as possible.
The following five factors cause differences in the timing of ON or OFF of MOSFETs.

A: The parasitic inductance on the board (hereafter referred to as "parasitic inductance") of Q1 and Q2 is unbalanced.

B: Large dI_D/dt of MOSFET.

C: Individual gate resistors R_G_Q1 and R_G_Q2 have different values.

D: Thresholds of MOSFET (hereafter referred to as "$V_{GS(th)}$") of Q1 and Q2 is unbalanced.

E: The parasitic capacitances of MOSFET of Q1 and Q2 is unbalanced.

Factors A-C depend on the circuit design, while factors D-E depend on MOSFET device characteristics. These factors are verified by using the evaluation board PCB008P in the next section.

4. Oscillation evaluation items

Based on the five factors shown in the previous section, the following tests were identified to demonstrate principles

A': Unbalance parasitic inductance in Q1 and Q2.

A'-1: Unbalance the parasitic inductances of the drain (L_D) in Q1 and Q2.

A'-2: Unbalance the parasitic inductances of the source (L_S) in Q1 and Q2.

A'-3: Unbalance the parasitic inductances of the gate (L_G) in Q1 and Q2.

A'-4: Unbalance the parasitic inductances of the kelvin source (L_{KS}) in Q1 and Q2.

B': Increase the rate of change of MOSFET drain current (hereafter referred to as ''dI_D/dt'').

B'-1: Increase the drain current ($I_{D,\ pulse}$).

B'-2: Reduce common gate resistor R_G_com.

C': Unbalance individual gate resistors R_G_Q1 and R_G_Q2.

D': Unbalance the threshold voltage ($V_{GS(th)}$) of Q1 and Q2.

E': Unbalance parasitic capacitances Q1 and Q2.

E'-1: Unbalance C_{GD} Q1 and Q2.

E'-2: Unbalance C_{GS} Q1 and Q2.

E'-3: Unbalance C_{DS} Q1 and Q2.

Please note that test E' was investigated by simulation.

Figure 4-2 shows the conditions and circuit for evaluating oscillations. Also shown in Figure 4-3 is a picture of the evaluation. In this evaluation, an opto-isolated differential probe made by Tektronix® was used for V_{GS} waveform

measurement probe to correctly measure the oscillation waveform of the gate. Especially in the measurement of the gate voltage, the influence of the measurement environment becomes large for the high-side switch. For more details, refer to the application note "Precautions during gate-source voltage Measurement for SiC MOSFET" [1].

Evaluation Board: PCB008P
Number of parallel: 2 parallel
SiC MOSFET: SCT4018KR (1200V 18mohm TO-247- 4L)
Evaluation circuit: Double-pulse circuit of low-side (hereafter referred to as “LS”) switching
HV dc voltage E=800V
Inductor L=250μH
Gate voltage V_{GS}=18V/0V
Temperature T=25℃

Measurement instrument
Oscilloscope: MSO58 5-BW-500 made by Tektronix®
V_{DS} probe: THDP0200 made by Tektronix®
V_{GS} probe: TIVP05, 650-6122-00 made by Tektronix®
I_D probe: SS-665 made by IWATSU

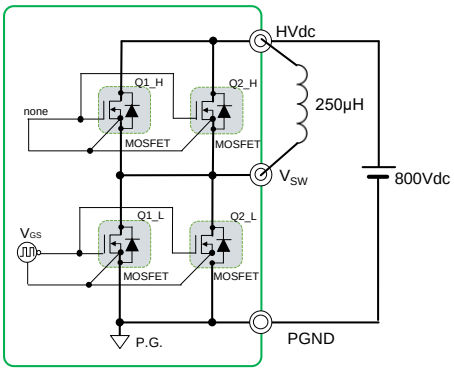


Figure 4-2. Double-pulse test setup to evaluate low-side switching

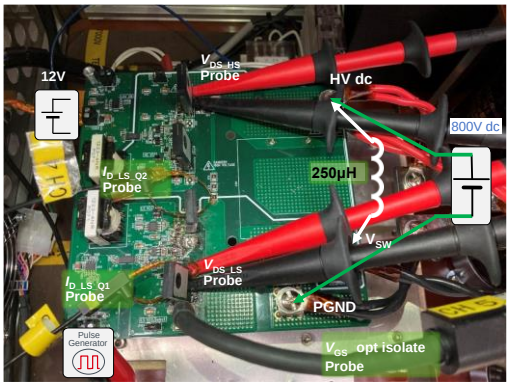


Figure 4-3. Evaluation image

Oscillation waveform of the gate was revealed in this oscillation evaluation. The gate OFF waveforms are compared in the following sections because the gate OFF has a higher rate of change in the drain current than the gate ON and a stronger trigger for oscillation.

5. Oscillation evaluation results

A‘: Unbalance parasitic inductance in Q1 and Q2.

At first, the parasitic inductance components on the board were analyzed using Ansys® Electromagnetic Field Analysis Software (Q3D Extractor®. Figure 5-1 shows the circuit diagram with parasitic inductances, Figure 5-2 shows the PCB pattern layout of PCB008P, and Table 5-1 shows the parasitic inductance extraction results.

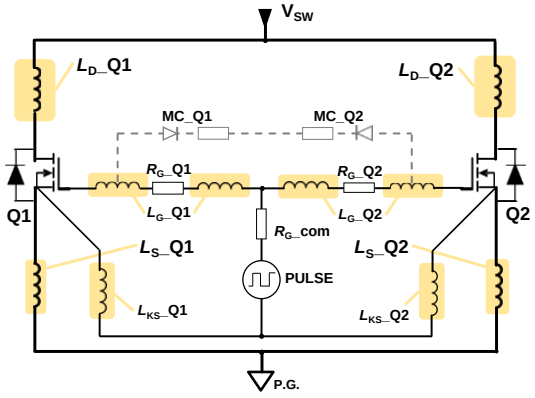
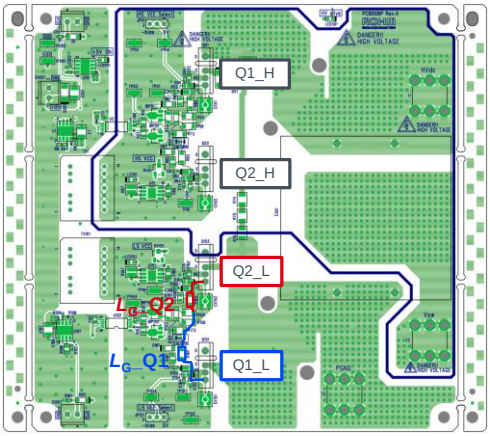
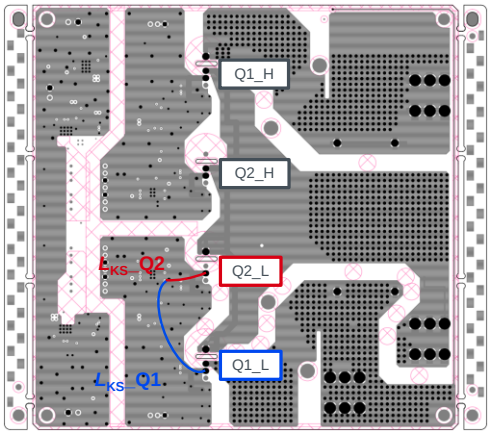


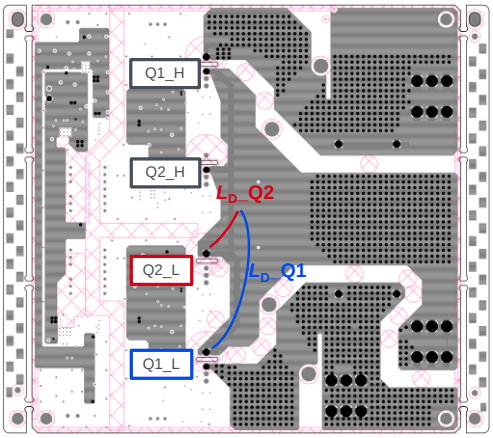
Figure 5-1. Parasitic inductance extraction points



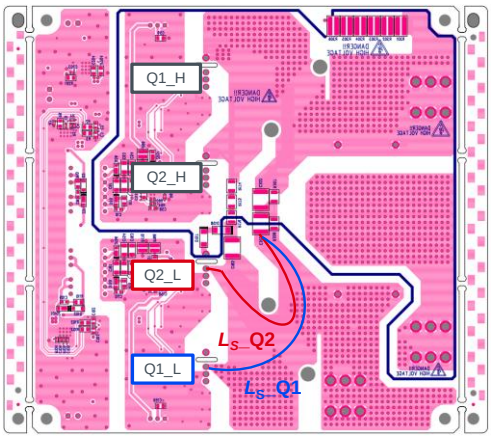
(a) Component surface pattern (L_G)



(b) Layer 2 pattern (L_{KS})



(c) Layer 3 pattern (L_D)



(d) Solder Surface Pattern (L_S)

Figure 5-2. PCB008P Layout Diagram

Table 5-1. Parasitic inductance extraction results

	L_Q1[nH]	L_Q2[nH]	L_Q1-L_Q2[nH]
L_D	15.67	4.61	11.06
L_S	10.70	16.20	-5.50
L_G	17.66	6.74	10.92
L_{KS}	7.74	2.62	5.12

The extraction results shows that the parasitic inductance is already unbalanced on the board. In this evaluation, the parasitic inductance of the MC circuit shown by the dotted line in Figure 5-1 was not considered. The reason is that the parasitic capacitance of the MC diode (approximately 50 pF) used in this evaluation has high impedance in the frequency band of the oscillation that occurs in this case. The MC circuit does not form a path for oscillation and this particular parasitic inductance element can be ignored.

To demonstrate the impact of increase imbalance, a cable was intentionally added to the lead terminal of MOSFET. Figure 5-3 shows an image of the cable addition in case MOSFET is viewed from the side.

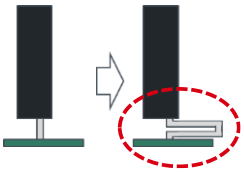


Figure 5-3. Increasing inductance via additional cable

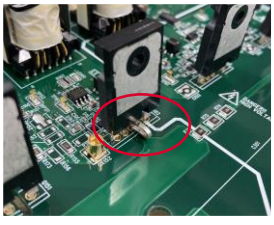
The following three types of cable (b) to (d) were additionally connected. Figure 5-4 shows the state image of the cable addition.

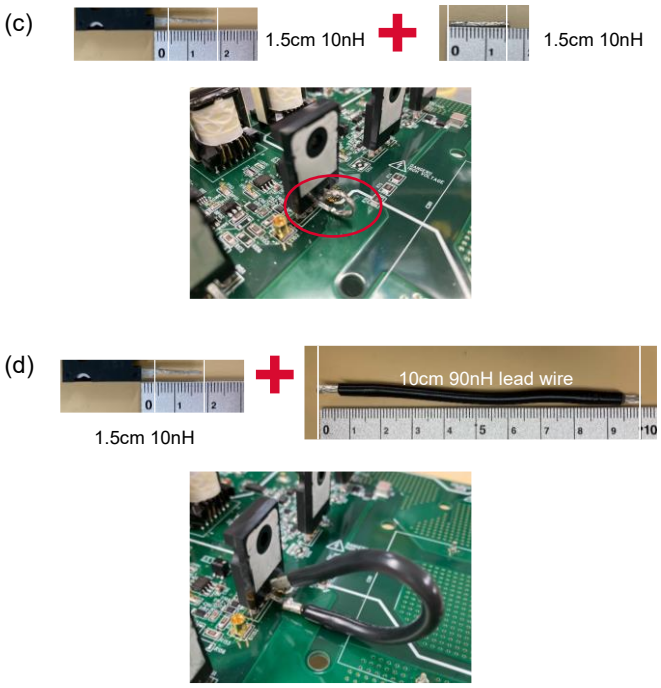
(a) No additions
(b) Add 10nH
(c) Add 20nH
(d) Add 100nH

(a)

(b)

1.5cm 10nH





(d)

Figure 5-4. Parasitic inductance Addition

By assuming the variation on a typical board to be 10nH to 20nH and adding an additional 10nH and 20nH to the PCB008P, it is now possible to evaluate the variation from 10nH to 25nH. In addition, in this evaluation, to investigate whether MOSFET would be damaged by oscillations by performing a margin evaluation, we also evaluated an unrealistic parasitic inductance, an additional 100nH

The double pulse evaluation conditions for evaluation item A' are as follows. To make oscillation easier to observe, the individual gate resistors were set to 0Ω.

$I_{D,\ pulse}$: 128A per each (256A total)
R_G_Q1, R_G_Q2: 0Ω
R_G_com: 2Ω
$V_{GS(th)}$_Q1 and $V_{GS(th)}$_Q2: 4.2V (Actual values of used devices)

A'-1: Unbalance L_D in Q1 and Q2.

L_D added by cable to exaggerate the parasitic inductance of Q1. Figure 5-5 shows the V_{GS}_LS_Q1 waveform during gate OFF.

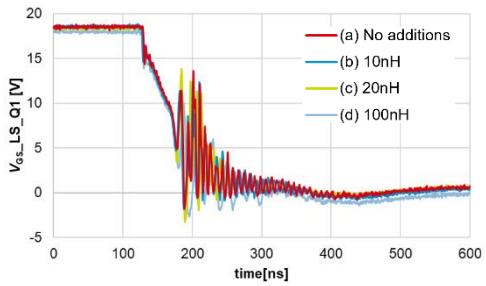


Figure 5-5. V_{GS}_Q1_low-side waveform (Unbalance L_D)

Oscillation occurs under the condition (a) because the individual gate resistance is 0 Ω and/or because the parasitic inductance of the board is unbalanced. When conditions (b), (c) and (d) are compared based on conditions (a), there is no significant difference in oscillation amplitude.

A'-2: Unbalance L_S in Q1 and Q2.

L_S added by cable to Q2 to exaggerate the parasitic inductance of Q2. Figure 5-6 shows the V_{GS}_LS_Q1 waveform during gate OFF. Cable was added to Q2, but all conditions in this evaluation were compared with the gate voltage waveform of Q1. Because the gate of Q1 and Q2 are connected to each other through R_G_Q1 and R_G_Q2, it has been confirmed that similar amplitude waveforms can be observed.

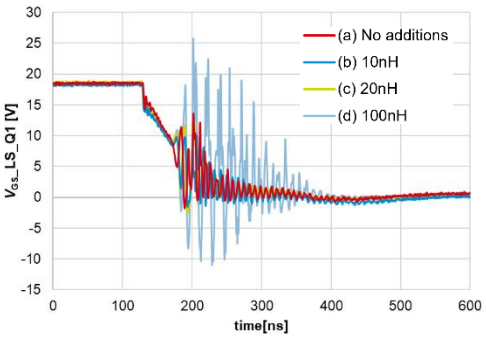


Figure 5-6. V_{GS}_Q1_low-side waveform (Unbalance L_S)

When conditions (b), (c), and (d) are compared based on condition (a), there is no significant difference in condition (c), but in condition (d), oscillating up to about -10V to 25V and significantly exceeding V_{GS} rating. The duration of oscillation is about three times longer. This is oscillation caused by parallel resonance and using in this condition could cause damage.

A'-3: Unbalance L_G in Q1 and Q2.

L_G added by cable to Q1 to exaggerate the parasitic

inductance of Q1. Figure 5-7 shows the V_{GS}_LS_Q1 waveform during gate OFF.

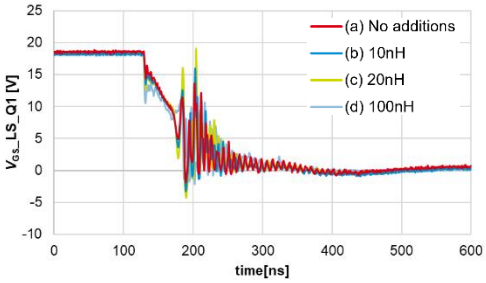


Figure 5-7. V_{GS}_Q1_low-side waveform (Unbalance L_G)

When conditions (b), (c), and (d) are compared based on conditions (a), the oscillation amplitude large in places under some conditions, but there is no significant change in the oscillation duration.

A'-4: Unbalance L_{KS} in Q1 and Q2.

L_{KS} added by cable to Q1 to exaggerate the parasitic inductance of Q1. Figure 5-8 shows the V_{GS}_LS_Q1 waveform during gate OFF.

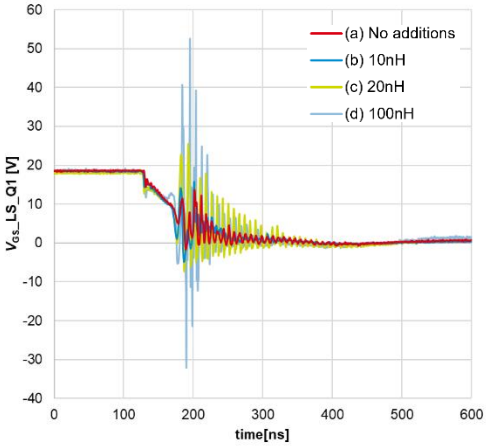


Figure 5-8. V_{GS}_Q1_low-side waveform (Unbalance L_{KS})

Comparing conditions (b), (c), and (d) with respect to condition (a), it was found that the larger L_{KS} is unbalanced, the larger the oscillation amplitude of the gate voltage becomes. In condition (d), the oscillation amplitude exceeds 50V and V_{GS} rating, but there is a risk of exceeding the V_{GS} rating even in condition (c). Unbalanced L_{KS} elements increases the oscillation amplitude and duration.

B': Increase the dI_D/dt.

B'-1: Increase the $I_{D, pulse}$.

Next, $I_{D, pulse}$ was changed for evaluation. The evaluation conditions for the evaluation items B'-1 are as follows.

IR_G_Q1, R_G_Q2: 0Ω
R_G_com: 2Ω
$V_{GS(th)}$_Q1 and $V_{GS(th)}$_Q2: 4.2V

Figure 5-9 shows the V_{GS}_LS_Q1 waveforms during gate OFF in case $I_{D, pulse}$ is conditioned as (a) to (c) below.

(a) $I_{D, pulse}$: 64A per each (128A total)
(b) $I_{D, pulse}$: 128A per each (256A total)
(c) $I_{D, pulse}$: 160A per each (320A total)

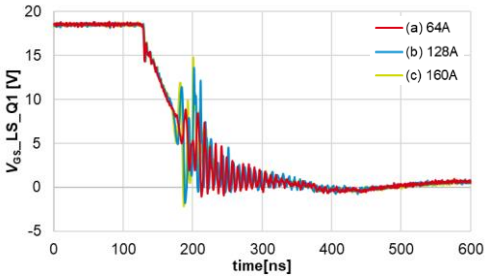


Figure 5-9. V_{GS}_Q1_low-side waveform (Increase $I_{D, pulse}$)

Figure 5-10 shows the I_D_LS_Q1 waveform. The dI_D/dt of Q1 during gate OFF is as follows.

(a) $I_{D, pulse}$: 64A per each (128A total) dI_D/dt: 5.8A/ns
(b) $I_{D, pulse}$: 128A per each (256A total) dI_D/dt: 8.5A/ns
(c) $I_{D, pulse}$: 160A per each (320A total) dI_D/dt: 10.2A/ns

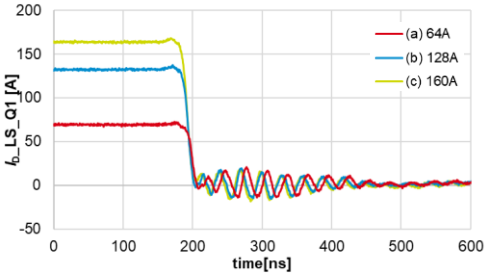


Figure 5-10. I_D_Q1_low-side waveform (Increase $I_{D, pulse}$)

In case I_D is increased, dI_D/dt at the time of gate OFF increases, and the switching speed increases. Therefore, it is easier to trigger oscillation, and the oscillation amplitude increases.

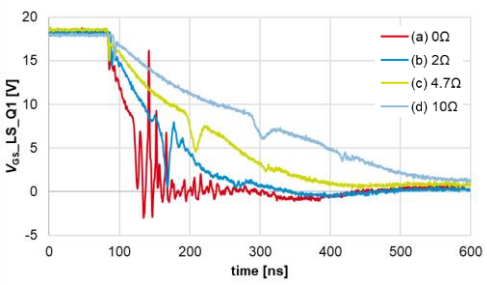
B'-2: Reduce common gate resistor R_G_com.

Reducing the common gate resistor increases the switching speed and dI_D/dt. The evaluation conditions for the evaluation items B'-2 are as follows. In case R_G_com is 0Ω, if the individual gate resistance is 0Ω the sum of the gate resistances becomes 0Ω, and V_{DS} surge exceeds the V_{DS} rating. Therefore R_G_Q1 and R_G_Q2 were set to 2Ω.

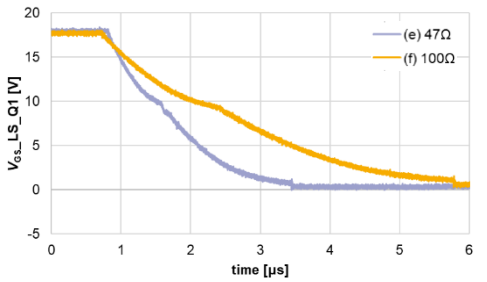
$I_{D, pulse}$: 128A per each (256A total)
R_G_Q1 and R_G_Q2: 2Ω
$V_{GS(th)}$_Q1 and $V_{GS(th)}$_Q2: 4.2V

Figure 5-11 shows the V_{GS}_LS_Q1 waveform during gate OFF in case R_G_com is changed from (a) to (f) below.

(a) R_G_com: 0Ω
(b) R_G_com: 2Ω
(c) R_G_com: 4.7Ω
(d) R_G_com: 10Ω
(e) R_G_com: 47Ω
(f) R_G_com: 100Ω



(a) 0Ω (b) 2Ω (c) 4.7Ω (d) 10Ω

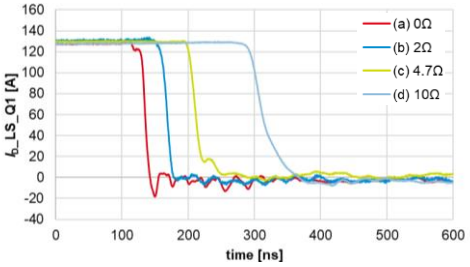


(e)47Ω (f)100Ω

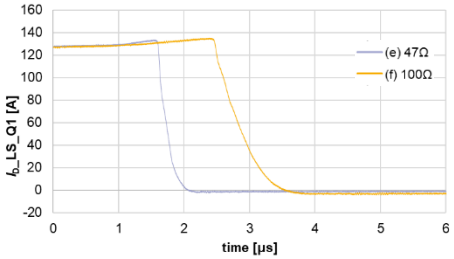
Figure 5-11. V_{GS}_Q1_low-side waveforms with variable R_G_com

Figure 5-12 shows the I_D_LS_Q1 waveform during gate OFF in case R_G_com is changed from (a) to (f). The dI_D/dt of Q1 during gate OFF is as follows.

(a) R_G_com: 0Ω dI_D/dt: 12.3A/ns
(b) R_G_com: 2Ω dI_D/dt: 8.7A/ns
(c) R_G_com: 4.7Ω dI_D/dt: 6.4A/ns
(d) R_G_com: 10Ω dI_D/dt: 3.5A/ns
(e) R_G_com: 47Ω dI_D/dt: 4.0A/ns
(f) R_G_com: 100Ω dI_D/dt: 2.0A/ns



(a)0Ω (b)2Ω (c)4.7Ω (d)10Ω



(e)47Ω (f)100Ω

Figure 5-12. I_D_Q1_low-side waveform (Reduce R_G_com)

The smaller the R_G_com value, the higher dI_D/dt at the time of gate OFF, and the faster the switching speed and the more pronounced the oscillations. Oscillation was suppressed in case R_G_com (dI_D/dt) per one MOSFET was 4.7 Ω or more (less than 6.4A/ns) on the circuit board. This indicates that the oscillation is significantly affected by dI_D/dt.

C': Unbalance Individual gate resistors R_G_Q1 and R_G_Q2.

R_G_Q1 and R_G_Q2 were unbalanced for evaluation. The evaluation conditions for the evaluation items C' are as follows.

$I_{D,pulse}$: 128A per each (256A total)
Parasitic inductance: L of evaluation board (Table 5-1)
$V_{GS(th)}$_Q1, $V_{GS(th)}$_Q2: 4.2V

Figure 5-13 shows the V_{GS}_LS_Q1 waveform during gate OFF in case R_G_Q1 and R_G_Q2 is changed from (a) to (c) as below. R_G_com should be better to compare at 0 Ω in condition (a). However, in case the total gate resistor is 0 Ω, V_{DS} surge exceeded the V_{DS} rating, so the R_G_com value is set to 2 Ω.

(a) R_G_com: 2Ω R_G_Q1: 0Ω R_G_Q2: 0Ω
(b) R_G_com: 0Ω R_G_Q1: 0Ω R_G_Q2: 10Ω
(c) R_G_com: 0Ω R_G_Q1: 0Ω R_G_Q2: 100Ω

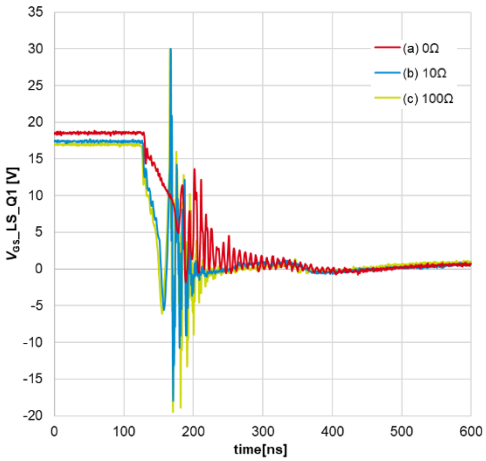


Figure 5-13. V_{GS}_Q1_low-side waveform with unbalanced R_G_Q1 and R_G_Q2

The larger the imbalance of the R_G_Q1 and R_G_Q2, the longer the oscillation duration. However, in condition (c), the oscillations do not quickly subside and in condition (c) and condition (b), there is no significant difference in the oscillation amplitude. On the other hand, in condition (a) and condition (b), the difference in the oscillation amplitude is large, and the individual gate resistance becomes unbalanced, which means that the oscillation amplitude is increased. In general, however, the gate resistance does not vary by more than 10 Ω. This indicates that the more the the gate OFF timing of Q1 and Q2 is shifted., the larger the oscillation amplitude.

D': Unbalance $V_{GS(th)}$ Q1 and Q2.

Special samples were created to unbalance $V_{GS(th)}$for this evaluation. The evaluation conditions for the evaluation items D' are as follows. To make oscillation easier to observe, the individual gate resistance was set to 0 Ω.

$I_{D, pulse}$: 128A per each (256A total)
R_G_com: 2Ω
R_G_Q1, R_G_Q2: 0Ω

Figure 5-14 shows the V_{GS}_LS_Q1 waveform during gate OFF in case $V_{GS(th)}$ is changed from (a) to (b) as below.

(a) $V_{GS(th)}$_Q1: 4.2V $V_{GS(th)}$_Q2: 4.2V
(b) $V_{GS(th)}$_Q1: 4.1V $V_{GS(th)}$_Q2: 4.8V*2

*2: It does not indicate that $V_{GS(th)}$ of MOSFET in the same lot varies within 0.7V.

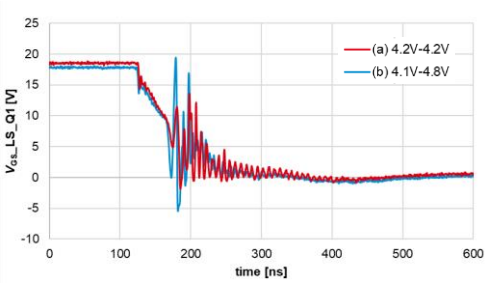


Figure 5-14. V_{GS}_Q1_low-side waveforms with unbalanced $V_{GS(th)}$

If $V_{GS(th)}$ is unbalanced, the oscillation amplitude becomes larger because the gate OFF is timed out of alignment. However, since R_G_Q1 and R_G_Q2 were 0 Ω in this evaluation, the oscillation amplitude increased. By setting R_G_Q1 and R_G_Q2 to the appropriate values, oscillations caused by $V_{GS(th)}$ variations can be suppressed.

E': Unbalance parasitic capacitances Q1 and Q2 (simulation).

This evaluation item was evaluated by simulation because it is difficult to prepare samples having specifically unbalanced parasitic capacitances. The evaluation conditions for the evaluation items E' are as follows. In the simulation,in case R_G_Q1 and R_G_Q2 are set to 0 Ω, there a long period of oscillation in the waveforms. So, the simulation was performed with 2 Ω in this time.

$I_{D, pulse}$: 128A per each (256A total)
R_G_com: 2Ω
R_G_Q1, R_G_Q2: 2Ω

E'-1: Unbalance C_{GD} Q1 and Q2.

C_{GD}-V_{DS} curve was shifted on the simulation. Figure 5-15 shows the V_{GS}_LS_Q1 waveform during gate OFF in case parasitic capacitance is changed from (a) to (c) below.

(a) C_{GD}_Q1: No change
C_{GD}_Q2: No change
(b) Increase the C_{GD} value of Q1.
C_{GD}_Q1: C_{GD} curve shifted to 10% higher capacity side.
C_{GD}_Q2: No change
(c) Decrease the C_{GD} value of Q1.
C_{GD}_Q1: C_{GD} curve shifted to 10% lower capacity side.
C_{GD}_Q2: No change

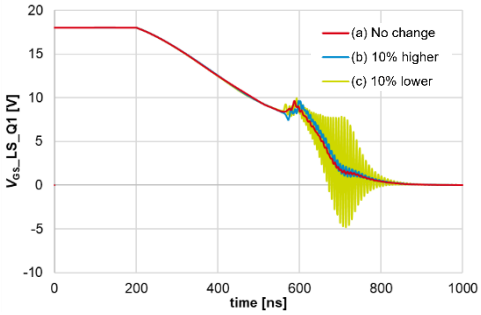


Figure 5-15. V_{GS}_Q1_low-side waveform with unbalanced C_{GD}

In condition (c), it assumes that C_{GD} is unbalanced, causing the gate OFF timing-shift, and that Q1 is oscillating because the value of C_{GD} is smaller. It should be taken care especially when using devices with a small chip size with a small absolute value of C_{GD}.

The above conclusions were made using simulations. Since the discussed property is very sensitive to the details of the physical situation, design work should be done with both simulations and physical, hardware investigations.

E'-2: Unbalance C_{GS} Q1 and Q2.

C_{GS}-V_{DS} curve was shifted on the simulation. Figure 5-16 shows the V_{GS}_LS_Q1 waveform during gate OFF in case parasitic capacitance is changed from (a) to (c) below.

(a) C_{GS}_Q1: No change
C_{GS}_Q2: No change
(b) Increase the C_{GS} value of Q1.
C_{GS}_Q1: C_{GS} curve shifted to 10% higher capacity side.
C_{GS}_Q2: No change
(d) Decrease the C_{GS} value of Q1.
C_{GS}_Q1: C_{GS} curve shifted to 10% lower capacity side.
C_{GS}_Q2: No change

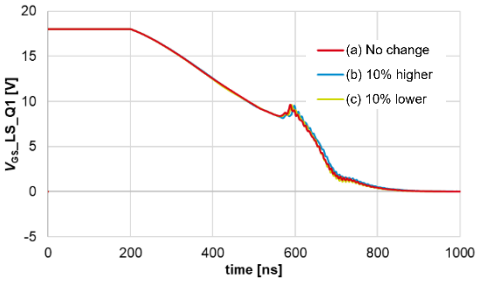


Figure 5-16. V_{GS}_Q1_low-side waveform with unbalanced C_{GS}

Even if C_{GS} is unbalanced, the amplitude of oscillation does not change.

E'-3: Unbalance C_{DS} Q1 and Q2.

C_{DS}-V_{DS} curve was shifted on the simulation. Figure 5-17 shows the V_{GS}_LS_Q1 waveform during gate OFF in case parasitic capacitance is changed from (a) to (c) below.

(a) C_{DS}_Q1: No change
C_{DS}_Q2: No change
(b) Increase the C_{DS} value of Q1.
C_{DS}_Q1: C_{DS} curve shifted to 10% higher capacity side.
C_{DS}_Q2: No change
(c) Decrease the C_{DS} value of Q1.
C_{DS}_Q1: C_{DS} curve shifted to 10% lower capacity side.
C_{DS}_Q2: No change

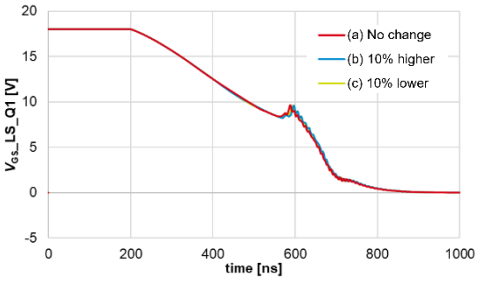


Figure 5-17. V_{GS}_Q1_low-side waveform with unbalanced C_{DS}

Even if C_{DS} is unbalanced, the amplitude of oscillation does not change.

This time, we evaluated 10% variation, but this is not an indication that MOSFETs in the same lot have generally 10% variation. However, it is desirable to use MOSFETs within the same lot for Q1 and Q2 as much as possible. Also, the actual imbalance between C_{GD}, C_{GS} and C_{DS} can occur in a complex manner.

In this simulation, we modified the parasitic capacitance by modifying Spice model. You can increase or decrease the parasitic capacitance curve by scaling Statement **X** below. For a detailed description of the Spice model, please refer to the application note "How to use thermal models " [2]. However, it should not be used as an accurate judgment of oscillation existence, because it is a simulation results. Please have a design margin on the simulation and have it verified on the actual machine.

ex) SCT4018KR

C_{GD}: C1 23 12 1p ⇒ C1 23 12 {1p*X}

C_{GS}: C2 22 33 4.857n ⇒ C2 22 33 {4.857n*X}

C_{DS}: C11 53 1 1p ⇒ C11 53 1 {1p*X}

For detailed Spice models, please refer to the link below.

SCT4018KR simulation model (rohm.com)*2

*2: This is the model as of 2023/9/25

Table 5-2 shows that results of oscillation evaluation. "V_{GS} Amplitude Difference" is the maximum value of the oscillation amplitude of the most oscillating condition minus the maximum value of the oscillation amplitude of the least oscillating condition. The larger the value, the more the necessity to take countermeasure.

Table. 5-2

Factor	Evaluation Item Number	Evaluation Item	V_{GS} Amplitude Difference[V]
A	A'-1	Unbalance L_D	0.2
A	A'-2	Unbalance L_S	12.0
A	A'-3	Unbalance L_G	6.2
A	A'-4	Unbalance L_{KS}	39.9
B	B'-1	Increase $I_{ID,\ pulse}$	6.0
B	B'-2	Reduce R_{G_com}	11.0
C	C'	Unbalance R_G_Q1 and R_G_Q2	9.9
D	D'	Unbalance $V_{GS(th)}$	5.6
E	E'-1	Unbalance C_{GD}	6.0
E	E'-2	Unbalance C_{GS}	0.2
E	E'-3	Unbalance C_{DS}	0.2

From this result, the L_S and L_{KS} imbalances of factor A affect the oscillation most. Equally designing L_S and L_{KS} are highest priority. Also, R_G_Q1 and R_G_Q2 should be set to the same value – and larger than 0 Ω. In addition, R_G_com should be larger than 0 Ω.

D and E are MOSFET characteristics. It is not possible to take countermeasures in the board design. Therefore, it is important to fully consider the board design for the factors A to C on the circuit.

6. Verification of Oscillation Countermeasures

In this section, five oscillation suppression countermeasures are developed and investigated. There are three ways to improve factors A to C of oscillation, and there are two ways to suppress oscillation by adding new parts. Although it is important to confirm at the design stage, this method can also be used when oscillation occurs at the verification stage after the completion of board design.

The countermeasures are I to V as below.

Countermeasures to improve factors A to C of oscillation

I. Balance L_S and L_{KS} in Q1 and Q2.

II. Increase R_G_com.

III. Increase R_G_Q1 and R_G_Q2.

Countermeasures to suppress oscillation by adding new parts

IV. Add chip ferrite beads to the gate line

V. Add external C_{GS}

The test conditions for the following oscillation evaluations are the same as shown in Section 4. Oscillation evaluation items .

I. Balance L_S (L_{KS}) in Q1 and Q2.

Factor A of Section5. Oscillation evaluation results revealed that the imbalance between L_S and L_{KS} affects the oscillation. Since L_S and L_{KS} are at the same electric potential, only L_S was evaluated with equal value. L_S are extracted as follows:

L_S_Q1: 10.7nH

L_S_Q2: 16.2nH

Condition (a) added 5.5nH to L_S_Q1 to make it equal length. Figure 6-1 shows the image of the added cable. In condition (c), in order to compare with condition (a), 100nH was added to L_S_Q2 in the same way as in condition (d) for the parasitic inductance of Figure 5-4. in Section5. Oscillation evaluation results A': Unbalance parasitic inductance in Q1 and Q2.

(a) Add 5.5nH to Q1 (equal value)
(b) No additions
(c) Add 100nH to Q2

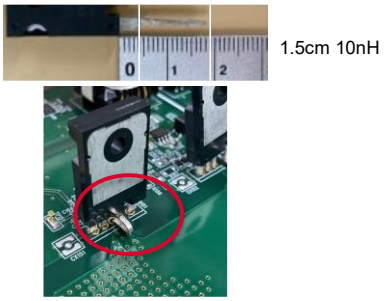


Figure 6-1. Parasitic inductance Addition (a)

Evaluation was conducted at the following conditions.

$I_{D,\ pulse}$: 128A per each (256A total)
R_G_Q1, R_G_Q2: 2Ω
R_G_com: 2Ω
$V_{GS(th)}$_Q1, $V_{GS(th)}$_Q2: 4.2V

R_G_Q1 and R_G_Q2 are set to 2 Ω, as indicated by Section 5. Oscillation evaluation results because they are required to prevent oscillation.

Figure 6-2 shows the V_{GS}_LS_Q1 waveform during gate OFF in case parasitic inductance is changed from (a) to (c).

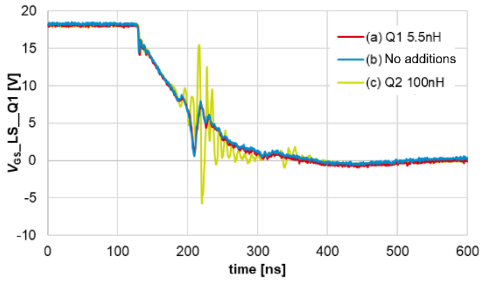


Figure 6-2. V_{GS}_Q1_low-side waveform (L_S are equal length)

On the precondition that R_G_Q1 and R_G_Q2 are inserted, oscillation can be suppressed in case L_S is made close to uniform value. However, there is no significant change in the waveform between 5nH and 0nH differences. It can thus be concluded that differences in the range of 5nH can be tolerated in this case.

Next, the absolute L_S is increased while L_S remains at the same value. An additional L_S of about 90nH was attached to both of Q1, Q2. Figure 6-3 shows the image of the added cable.

(a) Add 5.5nH to Q1 (equal length, short cable)
(d) Add 105nH to Q1and add 100nH to Q2 (equal length, long cable)

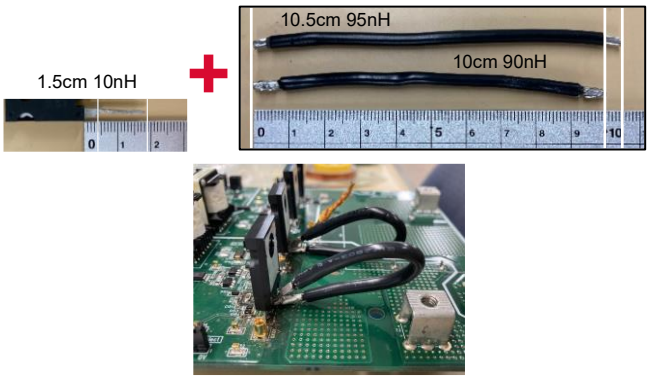


Figure 6-3. Parasitic inductance Addition (d)

Figure 6-4 shows the V_{GS}_LS_Q1 waveform during gate OFF in case parasitic inductance is changed to (a) and (d).

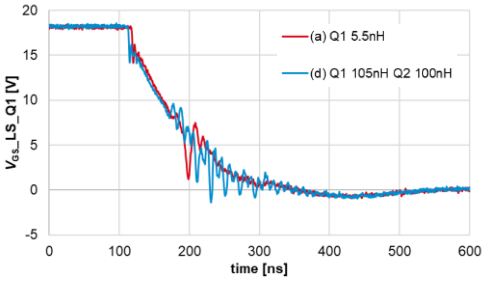


Figure 6-4. V_{GS}_Q1_low-side waveform
(Comparison of absolute L_S at equal values of L_S)

When the condition (a) is compared with the condition (d), oscillation occurs in the waveform of the condition (d) where the absolute L_S value is large. Therefore, the two L_S elements should be equivalent and designed as small as possible. However, the oscillation is smaller compared to Figure 6-2 condition (c). Therefore, the highest priority is to make L_S equal value even if the absolute L_S value is slightly larger.

II. Increase R_G_com

B'-2 of Section 5. Oscillation evaluation results shows that increasing R_G_com suppresses oscillations. However, the switching loss will increase, therefore system efficiency and heat generation must be carefully considered when selecting R_G_com.

III. Increase R_G_Q1 and R_G_Q2

As II shows, increasing R_G_com suppresses oscillation. However, you can also increase R_G_Q1 and R_G_Q2. Figure 6-

5 shows the V_{GS}_LS_Q1 waveform during gate OFF in case R_G_Q1 and Q2 are changed from (a) to (d).

$I_{D, pulse}$: 128A per each (256A total)
R_G_com: 2Ω
$V_{GS(th)}$_Q1 and $V_{GS(th)}$_Q2: 4.2V

(a) R_G_Q1 and R_G_Q2: 0Ω
(b) R_G_Q1 and R_G_Q2: 2Ω
(c) R_G_Q1 and R_G_Q2: 4.7Ω
(d) R_G_Q1 and R_G_Q2: 10Ω

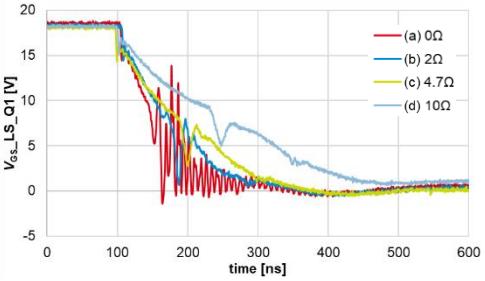


Figure 6-5. V_{GS}_Q1_low-side waveforms with increasing R_G_Q1 and R_G_Q2

Oscillation can be suppressed by increasing R_G_Q1 and R_G_Q2. However, by increasing R_G_com the switching speed becomes slower, which is effective in suppressing oscillation. In thi evaluation, increasing R_G_com and settingR_G_Q1 and R_G_Q2 to approximately 2 Ω is optimal.

IV. Add chip ferrite beads to the gate lines

The next countermeasure is to use the chip ferrite beads. The chip ferrite beads inductor can be placed in series with the gate driving line to suppress noise. Figure 6-6 shows the circuit diagram. Since no mounting pattern was provided in this evaluation, we substituted the pattern of R_G_Q1 and R_G_Q2. Figure 6-7 shows the chip ferrite beads mounting diagram.

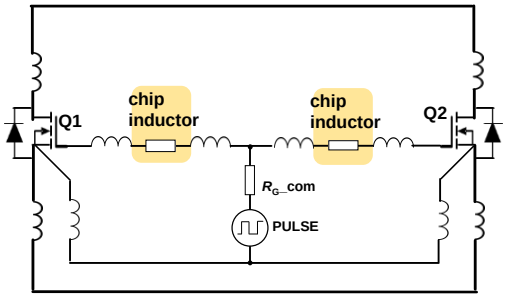


Figure 6-6. Circuit diagram with chip ferrite beads

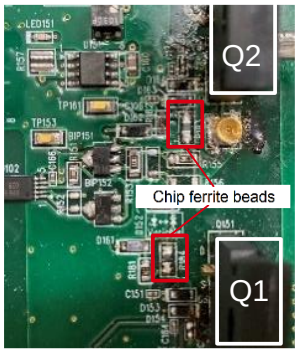


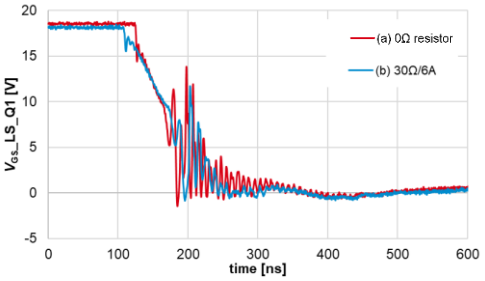
Figure 6-7. Chip ferrite beads mounting diagram

The evaluation conditions are as follows.

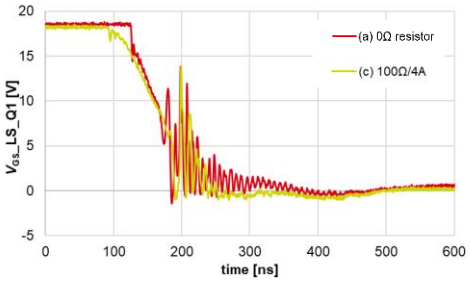
$I_{D, pulse}$: 128A per each (256A total)
R_G_com: 2Ω
$V_{GS(th)}$_Q1 and $V_{GS(th)}$_Q2: 4.2V

Figure 6-8 shows the V_{GS}_LS_Q1 waveform during gate OFF in case chip ferrite beads shown in (b) to (d) below are attached to the land pattern of the individual gate resistance. The evaluated chip ferrite beads are (b) to (d) below. All of them made by TDK.

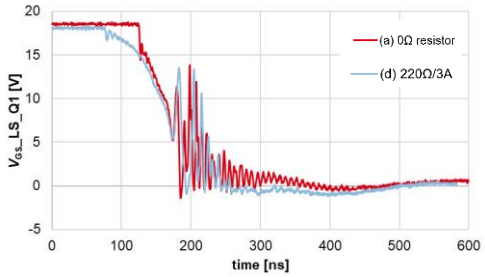
(a) R_G_Q1, R_G_Q2: No Chip ferrite beads
MCR18EZPJ000 (0Ω chip resistor)
(b) R_G_Q1, R_G_Q2: MPZ2012S300ATD25 (30Ω/6A)
(c) R_G_Q1, R_G_Q2: MPZ2012S101ATD25 (100Ω/4A)
(d) R_G_Q1, R_G_Q2: MPZ2012S221ATD25 (220Ω/3A)



(a)0Ω (b)30Ω/6A



(a) 0Ω (c) 100Ω/4A



(a) 0Ω (d) 220Ω/3A

Figure 6-8. V_{GS}_Q1_low-side waveforms measured with chip ferrite beads

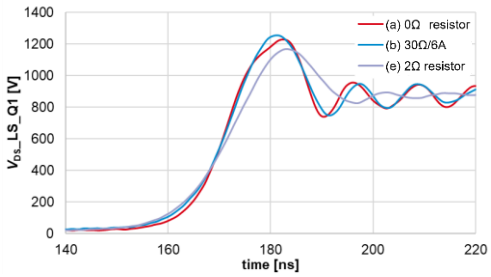


Figure 6-9. V_{DS}_Q1_low-side waveform (Compare chip ferrite beads with R_G)

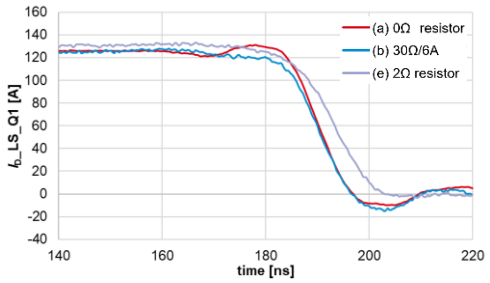


Figure 6-10. I_D_Q1_low-side waveform (Compare chip ferrite beads with R_G)

This result indicates that the chip ferrite beads in (b) are effective in suppressing oscillation.

Chip ferrite beads have a current rating. In this evaluation, we measured the charge/discharge current of the gate signal by the actual device. Consequently, we decided to select by 1A per C_{iss}=1000pF. For SCT4018KR used in this evaluation, it was approximately C_{iss}=4500pF.Therefore 5A chip ferrite beads are most suitable. In fact, more than 5A chip ferrite beads was suitable for the test.

Frequency dependent characteristics of the ferrite beads must be analyzed. It is recommended to select a device with an impedance of several Ω or more in the frequency band of oscillation.

Please note that inserting chip ferrite beads can result in increased V_{GS} surges at certain frequencies. In this evaluation, we focused on the gate OFF waveform to show that it is effective in suppressing oscillation. Be sure to check the entire V_{GS} waveform to confirm that surges do not exceed the V_{GS} rating.

Chip ferrite beads countermeasures seem to be less effective than Section III. Increase R_G_Q1 and R_G_Q2 countermeasures, but they also have advantage. Figure 6-9 shows the V_{DS}_LS_Q1 waveform during gate OFF. Figure 6-10 shows the I_D_LS_Q1 waveform during gate OFF.

(a) R_G_Q1, R_G_Q2: No Chip ferrite beads
MCR18EZPJ000 (0Ω chip resistor)
(b) R_G_Q1, R_G_Q2: MPZ2012S300ATD25 (30Ω/6A)

(e) R_G_Q1, R_G_Q2: No Chip ferrite beads
MCR18EZPJ2R0 (2Ω chip resistor)

(c) and (d) are no more effective than (b), so (c) and (d) are skipped.

The dV_{DS}/dt is almost unchanged in conditions (a) and (b), but condition (e) has a lower dV_{DS}/dt. Furthermore, dI_D/dt is almost unchanged in conditions (a) and (b), but dI_D/dt is lower in condition (e). In the condition (b), the oscillation amplitude can be suppressed without lowering dV_{DS}/dt and dI_D/dt, so there is no concern to increase switching-loss. In case the switching loss is important, the loss due to increased gate resistance and oscillation suppression can be balanced by adding a measure of chip ferrite beads in addition to the measure of gate resistance.

To summarize: When inserting chip ferrite beads into the gate line, the effect of suppressing oscillation is rather small, but it is effective in suppressing noise by reducing surge at oscillation frequency.

V. Add external C_{GS}

Finally, we introduce the countermeasures for adding an external C_{GS}. In addition to MOSFET parasitic capacitance C_{GS}, additional capacitance can be placed between the gate-source to reduce the switching-speed and suppress oscillation. Figure 6-11 shows the V_{GS}_LS_Q1 waveform during gate OFF when external C_{GS} is added.

$I_{D,\ pulse}$: 128A per each (256A total)
R_G_com: 2Ω

R_G_Q1 and R_G_Q2: 0Ω

$V_{GS(th)}$_Q1 and $V_{GS(th)}$_Q2: 4.2V

(a) No external C_{GS}

(b) External C_{GS} =1nF

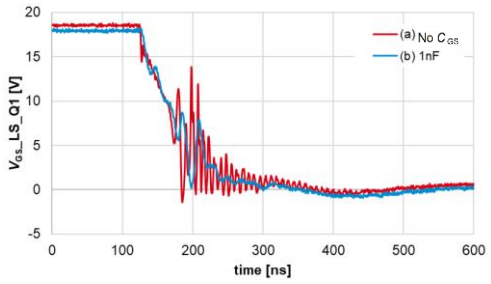


Figure 6-11. V_{GS}_Q1_low-side waveform with and withoutadd additional, external C_{GS}

Figure 6-11 shows that the oscillation obviously can be suppressed by adding external C_{GS}.

VI. Summary of counter-measure effectiveness

Finally, we have summarized the results of the oscillation suppression method in Table 6-1. V_{GS} Amplitude Difference is the value obtained by subtracting the maximum value of the oscillation amplitude of the waveform before the countermeasure and the oscillation amplitude of the condition in which the oscillation was suppressed most. The larger this value, the more effective countermeasures will be taken in this evaluation. It was most effective to increase R_G_com.

Table. 6-1

	Oscillation Countermeasures	V_{GS} Amplitude Difference[V]	Point to note
Ⅰ	Balance L_S (short and equal)	7.9	none
Ⅰ	Balance L_S (long and equal)	6.1	none
Ⅱ	Increase R_G_com	11.0	Increase switching loss
Ⅲ	Increase R_G_Q1 and R_G_Q2	7.8	Increase switching loss
Ⅳ	Add chip ferrite beads	2.0	Increase V_{GS} surge other than oscillation frequency
Ⅴ	Add external C_{GS}	6.3	Increase switching loss

If oscillations occur in case connecting MOSFETs in parallel, it is important to minimize and equalize L_S elements. This countermeasure is highly effective and does not have any major disadvantages.

If oscillations are still not suppressed, please take countermeasures with paying attention to the disadvantages.

7. Summary

The following three points should be given special attention when designing systems connecting MOSFETs in parallel.

- L_S and L_{KS} imbalance affects the oscillation most. L_S and L_{KS} should be designed to be as equal as possible.
- R_G_Q1 and R_G_Q2 should have the same value, and R_G_com should be included.
- If oscillation still occurs, external components such as chip ferrite beads and C_{GS} can be introduced.

To illustrate the above summary points, Figure 7-1 presents a circuit diagram with the critical elements highlighted.

It is possible to sufficiently suppress gate oscillation by correctly understanding the oscillation phenomenon and conducting optimum circuit board design. In the event that parallel oscillations occur, apply the described countermeasures described to ensure the power devices are operated safely within their maximum ratings.

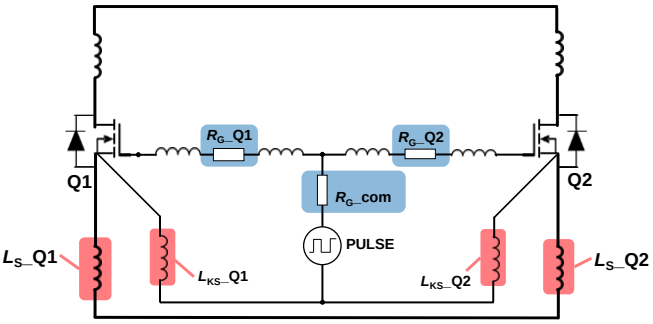


Figure 7-1. Two MOSFETs connected in parallel with critical circuit element highlighted

References:

[1] “Precautions during gate-source voltage measurement”
Application Note (No. 62AN085E Rev.002)
ROHM Co., Ltd., April 2020

[2] “How to use thermal models“
Application Note (No. 62AN113J Rev.001)
ROHM Co., Ltd., February 2020

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