Power Switching Device

Gate-source voltage behaviour in a bridge configuration

Power switching devices such as MOSFETs and IGBTs are used for various kinds of power supply applications, power supply line switching components, and other power applications. In addition, the circuit topologies used are diverse, parallel and series connections are widely used, not to mention single device use. Especially in bridge circuit configuration, in which the devices are connected in series, it is common to turn on and turn off each device alternately. Due to the current flowing and the voltage change in each device, the devices greatly affect one another. In this application note, we focus on Gate-Source voltage in MOSFET bridge configuration based on one of the simplest power circuits, a synchronous rectification boost converter to understand the switching operation in detail.

A bridge configuration of MOSFETs

A synchronous rectification boost circuit, the simplest bridge structure consisting of MOSFETs, is shown in the schematic (Figure. 1)

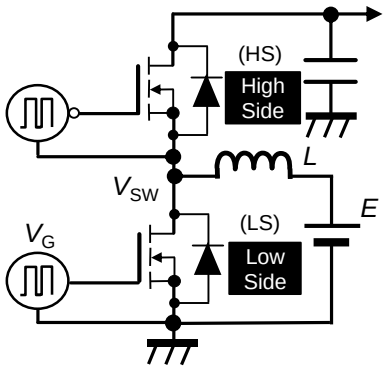

Figure 1: Synchronous rectification BOOST circuit

In this circuit, see Figure 1, the high-side (HS) and low-side (LS) MOSFETs turn on alternately. A dead time, where both transistors are in off-state, is set in order to avoid cross conduction where both devices are on. (Figure 2). This is so that you can later refer to HS and LS meaning the MOSFETs without having to say “the LS MOSFET” or “the HS MOSFET” every time later.

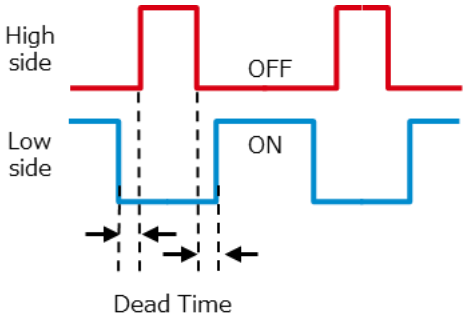

Figure 2: Gate signal (V_G) sequence

In Figure 3, the waveforms of the drain-source voltage (V_{DS}) and drain current (I_D) are sketched respectively for the HS and LS transistors shown in Figure 1. This is an example of hard-switching, where the current flowing through the inductor *L* is continuous.

The horizontal axis denotes time, and the time periods Tk (k=1~8) are defined as follows:

T1: LS is ON, and I_D of the MOSFETs varies

T2: LS is ON, and V_{DS} of the MOSFETs varies

T3: LS is ON, and I_D and V_{DS} are nearly stable

T4: LS is OFF, and V_{DS} of the MOSFETs varies

T5: LS is OFF, and I_D of the MOSFETs varies

T4-T6: Dead time, LS is OFF until HS turns ON

No. 60AN135E Rev.002
April.2020

T7: HS is ON（synchronous rectification）

T8: Dead time, HS is OFF until LS turns ON

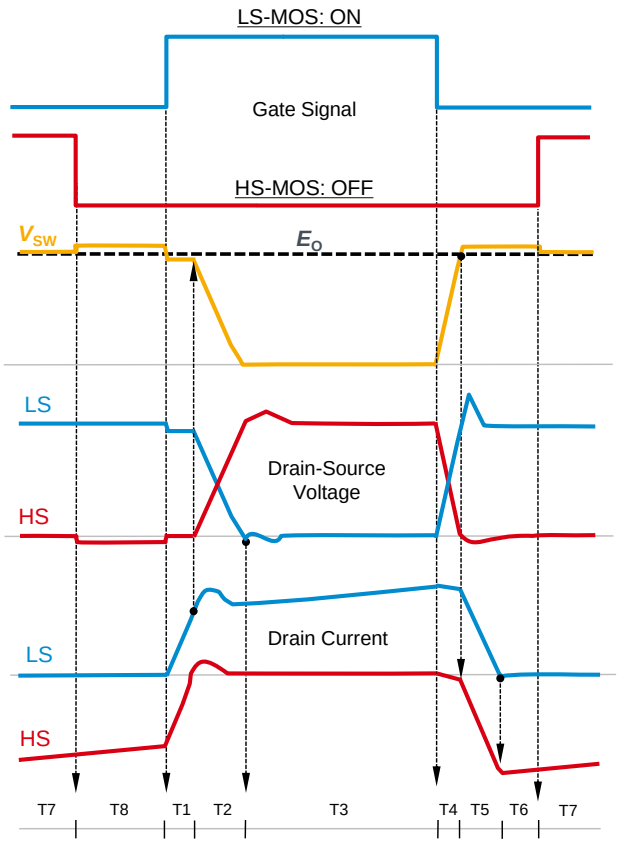

Figure 3: Voltage and current waveforms of HS and LS MOSFET.

Gate driver

In order to analyze how the changes of V_{DS} and I_D affect the gate-source voltage (V_{GS}) of transistors, an equivalent circuit for the gate drive has been provided in Figure 4.

The equivalent circuit includes: a gate signal (V_G), a gate resistance internally embedded in the MOSFET (R_{G_INT}), the source inductance of the device package (L_{SOURCE}), the inductance of the gate-driver circuit layout (L_{TRACE}), and an external gate resistance (R_{G_EXT}). Selected voltage polarities and current directions have been indicated in the diagram.

The inductance generated by the internal wiring of a transistor should also be taken into account, but this value is negligible in comparison to L_{TRACE}. Thus this inductance is ignored here.

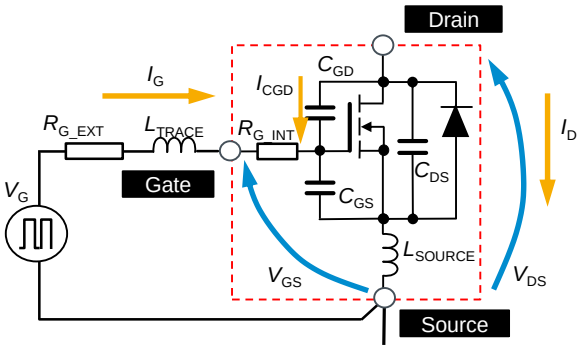

Figure 4: The equivalent circuit of a gate-drive circuit and a MOSFET.

Turn-on and -off operation

The following paragraphs describe each waveform segment as sketched in Figure 3.

When a positive supply, V_G is applied to the gate of LS to turn it on, the gate-source capacitance (C_{GS}) of LS starts to charge and V_{GS} increases. When V_{GS} goes over the threshold voltage, $V_{GS(th)}$, the drain current I_D of LS starts to flow and simultaneously the drain current I_D of HS starts to decrease (Figure 3-T1).

Finally, the HS I_D reaches zero and its body diode turns off, reducing the voltage between the HS source and the LS drain (V_{SW}). Simultaneously, the drain-source capacitance (C_{DS}) and the drain-gate capacitance (C_{GD}) of HS begins to change (Figure 3-T2). When this charging process is completed (the counterpart capacitances of LS discharge) and the V_{GS} of LS reaches V_G, the turn-on process of LS has been finished.

The V_G of LS going into the off-sate initiates the turn-off of LS (figure 3-T4). The charge stored in C_{GS} of LS is then discharged and V_{GS} of LS reaches the plateau voltage (Miller-effect domain). Then the V_{DS} of LS begins to go up, and V_{SW} rises at the same time. At this point, most of the load current still flows through LS (see Figure 3-T4). The body diode of HS is not active yet. When the charging of $C_{DS} + C_{GD}$ of LS is completed, V_{SW} goes over the supplied voltage (E), the body diode of HS turns on, and I_D of LS starts to flow through HS (see Figure 3-T5). After I_D of LS finally reaches zero, the circuit goes into the effective dead time period (see Figure 3-T6). The positive V_G is applied to the gate of HS, turning HS on and the synchronous operation begins (see Figure 3-T7).

In this sequence of the switching operation, the changes in V_{DS} and I_D of both HS and LS create various kinds of gate currents, making V_{GS} behaviour differ from the original V_G signal. Figure 5 shows what types of gate currents arise in a boost bridge configuration. Each label of (I), (I'), (II), and (III) represents an individual phenomenon that leads to a change in V_{GS}.

The resulting V_{GS} waveform is depicted in Figure 6. The numbers therein correspond to the same phenomena as those indicated in Figure 5. The dotted line in V_{GS} is an ideal waveform of the gate-source voltage signal.

The details are given in the following paragraphs.

Gate current generated by dV_{DS}/dt

As shown in Figure 4, a change in V_{DS} causes a current (I_{CGD}) to flow through C_{GD} .This current, as shown in Figure 5, divides into one current charging C_{GS} (I_{CGD1}:(II)-1) and the other current flowing into the gate-drive circuit (I_{CGD2}:(II)-2). At the early stage of V_{DS} change, the impedance of the gate-drive circuit is large, and thereby I_{CGD} mainly flows into C_{GS}. At this point, I_{CGD1} is mathematically expressed as:

$$I_{CGD} \cong I_{CGD1} = \frac{C_{GD}}{1+C_{GD}/C_{GS}} \cdot \frac{dV_{DS}}{dt} \quad (1)$$

This equation reveals that large C_{GD} and/or small C_{GD}/C_{GS} ratio increase I_{CGD1}

V_{GS} generated by dI_D/dt

The time-derivative of I_D, dI_D/dt, generates the voltage expressed as:

$$V_{Lsource} = L_{source} \cdot \frac{dI_D}{dt} \quad (2)$$

This is the event (I) and the associated current (I') flows as shown in Figure 5.

dV_{DS}/dt and dI_D/dt can take either a positive or a negative value, and thereby their consequent currents and voltages change polarity and direction, depending on whether turn-on or turn-off takes place. As shown in Figure 5, this voltage is seen by the measurement probes, but not by the device itself.

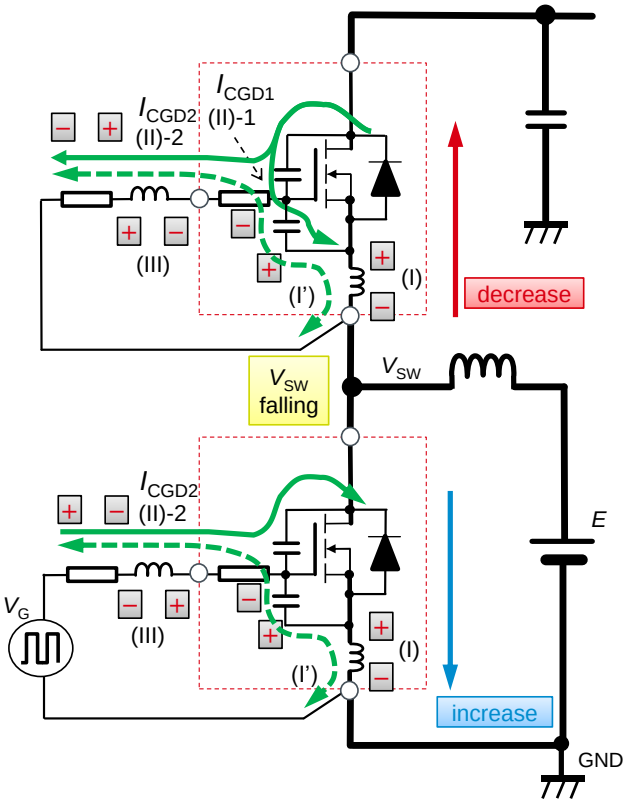

Figure 5: Gate current behaviour when LS turns on.

V_{GS} behaviour during turn-on

When LS turns on, I_D varies first, (see Figure 3-T1), and dI_D/dt >0 for both LS and HS. Thus the event (I) occurs and the electromotive force expressed by equation (2) arises in the parasitic source inductance with the polarity shown in Figure 5. This generates a current charging C_{GS} with its source side being a positive voltage. This charging polarity forces down V_{GS} of LS, and also pulls V_{GS} of HS into negative bias, observed as negative surge voltage.

When the LS I_D of LS settles, LS V_{DS} decrease (see Figure 3-T2). Thus the current, as expressed in equation (1), flows as indicated by (II)-1, and (II)-2 in Figure 5, making V_{GS} of HS go up as theoretically described by:

$$V_{SURGE2\text{-}1} = \frac{1}{C_{GS}} \int (I_{CGD1}) dt$$

$$= \frac{1}{1+C_{GS}/C_{GD}} \cdot \Delta V_{DS} \quad (3)$$

$$V_{SURGE2\text{-}2} = I_{CGD2} \cdot R_{G\_EXT} + L_{TRACE} \cdot \frac{dI_{CGD2}}{dt} \quad (4)$$

The increase in V_{GS} described in equation (3) is the major event just after V_{DS} begins to change, but the increase in V_{GS}, predicted by equation (4) may be observed with time. This shows that the behaviour of V_{GS} is affected by the ratio C_{GD}/C_{GS} of the MOSFET, the R_{G_EXT} of the drive circuit, and the parasitic inductance L_{TRACE} due to the layout of the gate-drive circuit.

As can be seen in Figure 5, I_{CGD2} in the HS-side ((II)-2) forces up V_{GS}. If the V_{GS} value goes over the threshold value it causes the so-called self-turn-on of the HS MOSFET. If this happens, both LS and HS are in on-state, generating a short-circuit current through HS and LS.

I_{CGD2} continues to flow until the turn-on of LS is completed, and the electromagnetic energy accumulates in L_{TRACE}. However, this current vanishes when the change of V_{SW} is finally completed, and thus L_{TRACE} generates a voltage as shown in Figure 5. This is event (III). This voltage can be larger than expected, because I_{CGD2} reaches several amperes in some cases, depending on the switching conditions, including R_{G_EXT}.

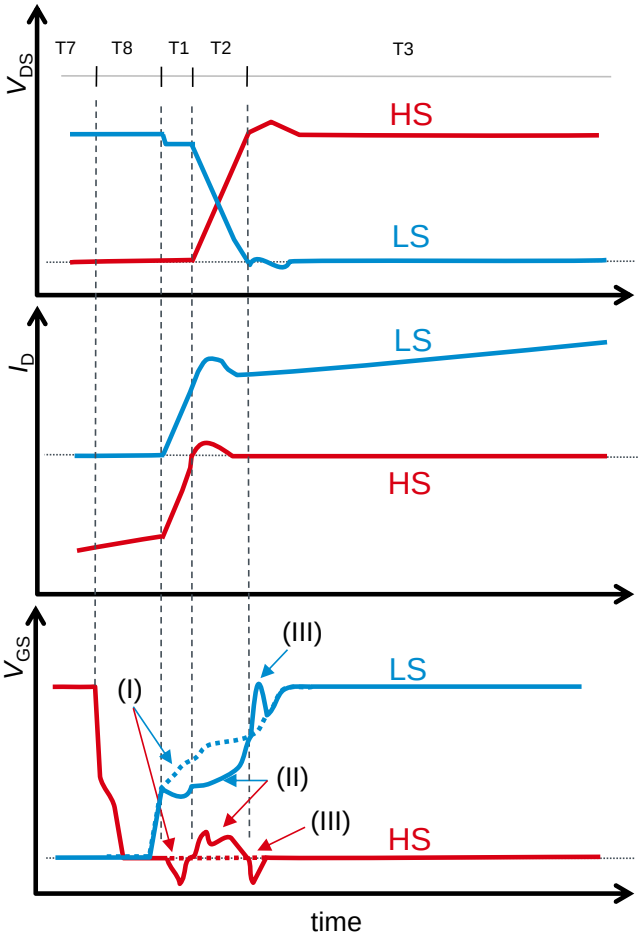

Figure 6: V_{DS}, I_D, and V_{GS} waveforms when LS turns on.

Figure 7 shows the double-pulse test results for a bridge circuit comprising ROHM devices with the LS turning on. R_{G_EXT} is 0Ω for Figure 7(a) and 10Ω for Figure 7(b).

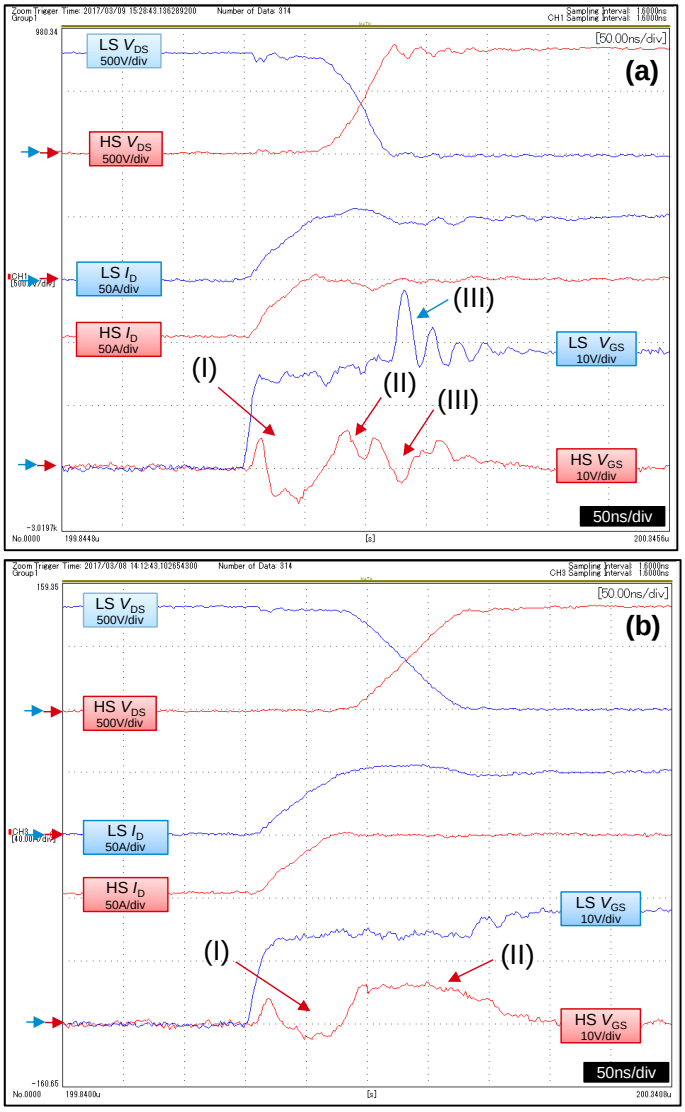

Figure 7: turn-on waveforms.
(a) R_{G_EXT}=0Ω、(b) R_{G_EXT}=10Ω

Small R_{G_EXT}, as shown in Figure 7(a), enhances the reduction in V_{GS} caused by event (I). Event (III) can be clearly recognized due to very high speed switching. 0Ω of R_{G_EXT} makes event (II) less significant, but on the other hand the unintentional increase in V_{GS}, due to event (II)-2, is seen in Figure 7(b).

These results show that a small R_{G_EXT} at HS turning off is generally recommended to inhibit the raising of V_{GS} (related to event (II)-2) inducing the self-turn-on of HS when LS is in

on-state. However, R_{G_EXT} for HS and LS are usually equal. Due to this, small R_{G_EXT} enhances the increase in dV_{DS}/dt of LS, and consequently I_{CGD} in HS rises as shown in equation (1). This increases event (II) surge of HS, as can be easily understood by use of equation (4). In order to avoid this, it is recommended that you separately set R_{G_EXT} for turn-on and turn-off. A diode as shown in Figure 8 is one of the common methods to realize this.

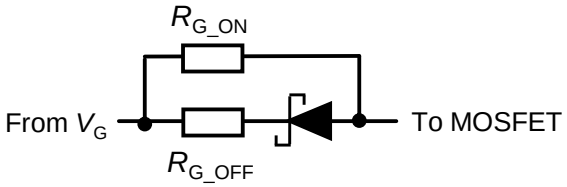

Figure 8: Adapted R_{G_EXT} circuit for different turn-on and turn-off gate resistance values

Here is another useful comment on the behaviour of V_{GS} : In Figure 7, HS V_{GS} goes positive for a moment before event-(I) occurs. This is conducted through C_{GS} by the voltage in L_{SOURCE} generated at the moment that the current relating to event (I) begins to flow.

V_{GS} behaviour during turn-off

Figure 9 shows how gate current flows when LS turns off. As we do for turn-on, each event is labelled as (IV), (V), and (VI). The fundamentals are the same for turn-off and turn-on, and the only difference is that V_{DS} and I_D change first. Each event has an equivalent one at turn-on:

turn-off	turn-on
event (IV)	→ event (II)
event (V)	→ event (III)
event (VI)	→ event (I)

Event (IV) is related to an unintentional increase in V_{GS} of LS caused by dV_{DS}/dt and a negative surge in V_{GS} of HS (see Figure 3-T4). After T4 ends, event (V) occurs because the voltage surge is caused by the energy due to I_{CGD1} as expressed in equation (1). After this, I_D starts to vary (see Figure 3-T6), and this time-derivative creates a voltage in L_{SOURCE} (equation (2)), which drives the current related to event (VI) as shown in Figure 9.

This current charges C_{GS} positively, and hence V_{GS} is raised up in HS and LS. This phenomenon opposes the decrease of V_{GS} in LS. All these events are summarized in the V_{GS} waveforms shown in Figure 10. The dotted line in V_{GS} represents an ideal gate-source voltage waveform.

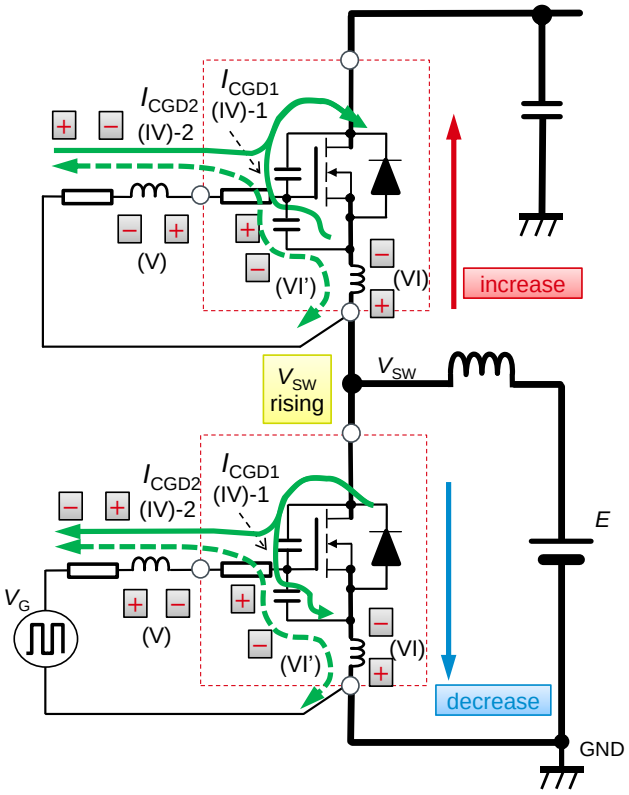

Figure 9: Gate current flow when LS turns off.

Figure 11 shows the double-pulse test results for a bridge circuit comprising ROHM devices with LS turning off. R_{G_EXT} is 0Ω for Figure 11(a) and 10Ω for Figure 11(b).

One can easily observe an event-(V) surge. The effects of event (IV) by dV_{DS}/dt are not generally significant, but the negative surge voltage in HS caused by this is often larger than the negative V_{GS} rating of SiC MOSFETs. It is therefore necessary to prepare countermeasure circuitry. A small R_{G_EXT} is generally effective to reduce the negative surge voltage in HS during turn off. However, the common R_{G_EXT} circuit as shown in Figure 8 makes event (IV) worse because R_{G_ON} is usually a highly resistive. Care should be taken to ensure that R_{G_ON} is not too big. An example of the countermeasure circuit is provided in “Gate-source voltage surge suppression methods” (*1) application note.

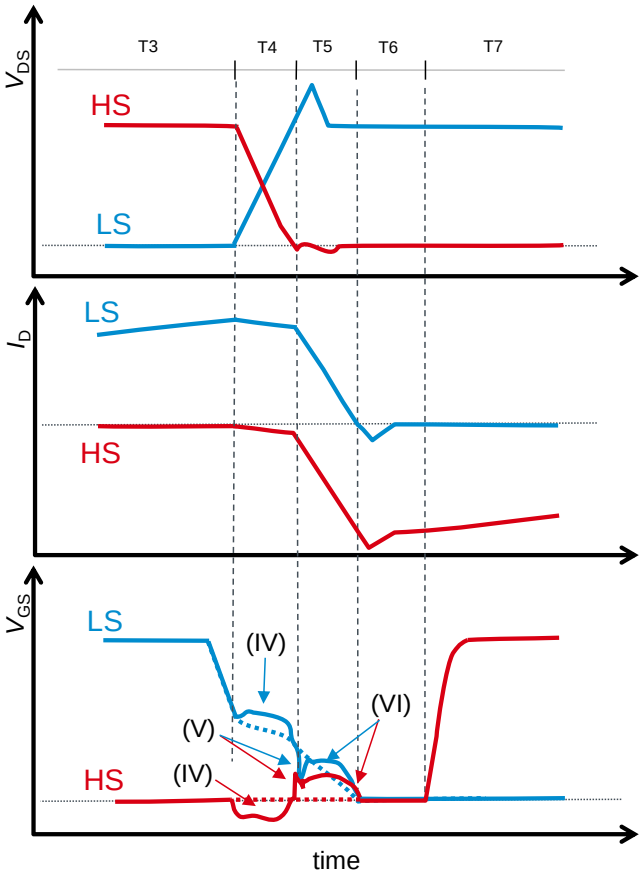

Figure 10: V_{DS}, I_D, and V_{GS} waveforms when LS turns off.

The voltage hump in V_{GS} related to event (VI) occurs a moment before the turn-off operation completes. Therefore, if HS begins to turn on, it is not serious because LS is already turned off.

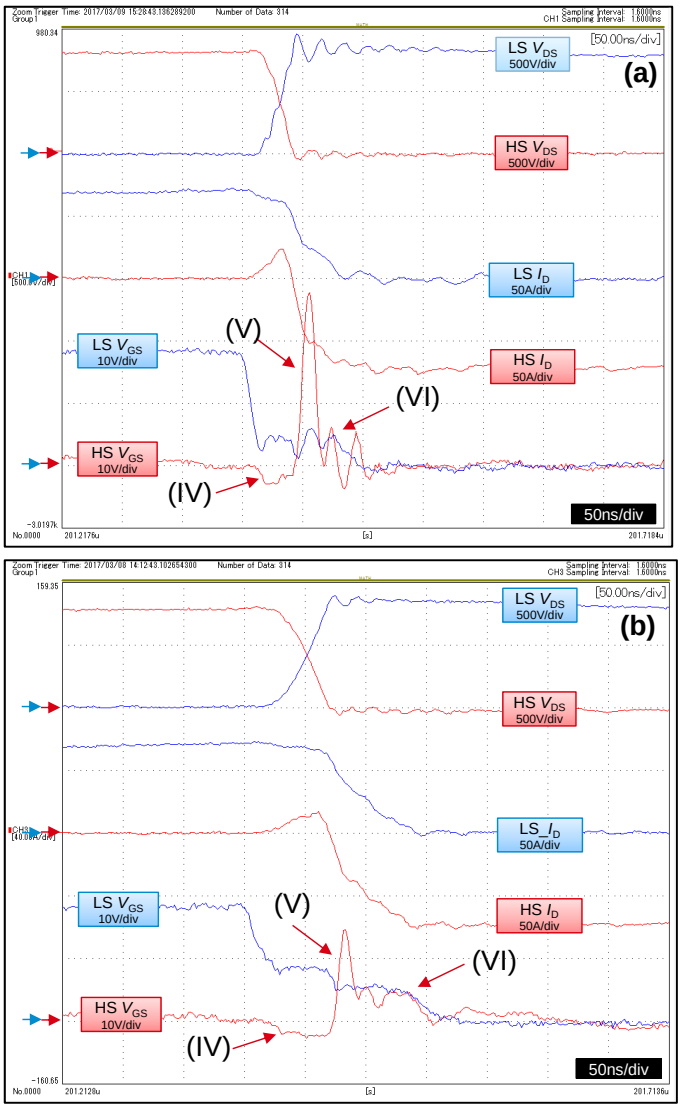

Figure 11. turn-off waveforms.
(a)R_{G_EXT}=0Ω、(b) R_{G_EXT}=10Ω

Summary

As has been described, the behaviour of V_{GS} in a bridge configuration is not trivial, because the MOSFETs interact with each other, and the gate-drive part plays an important role in determining the switching behaviour of the MOSFETs. It is therefore necessary to observe very different behaviours for different circuit board layouts even given the same circuit topology. Firstly, one should understand the fundamentals MOSFET behaviour as provided in this explanation, in order to optimise circuit performance. In this example a boost circuit with LS switching was used but a similar approach may be used for a buck converter with HS switching by replacing the function of LS and HS. These principles may in fact be applied to various circuit topologies which use hard switching.

References：

*1 Gate-source voltage surge suppression methods
Application Note (No. 62AN010ERev.002)
ROHM Co., Ltd. April 2020

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