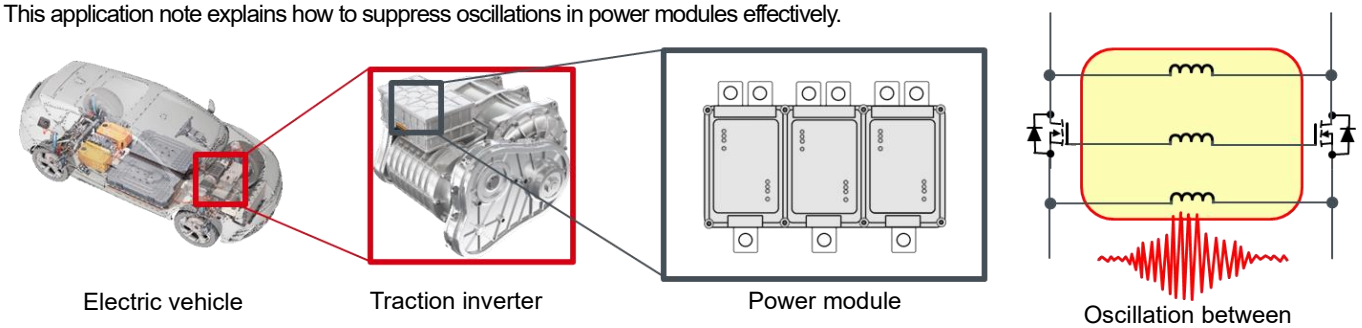
SiC MOSFET Bare Die Series

How to Suppress the Parallel Drive Oscillation in SiC Modules

SiC MOSFET is new generation power device with many excellent features compared to conventional Si devices, including high voltage, large current, high-speed drive, low loss, and high-temperature stability. In recent years, these excellent characteristics are being utilized in electric vehicles (EVs) that require higher power. In these EVs, power modules with several SiC MOSFET dies connected in parallel are increasingly being used for traction inverter circuits.

Meanwhile, using such high-speed power devices connected in parallel may cause parallel drive oscillation (hereinafter “oscillation”) between the dies. The dies may be destroyed if an oscillation occurs. Therefore, the development of countermeasures to suppress such oscillation has become a key challenge for the industry.

This application note explains how to suppress oscillations in power modules effectively.

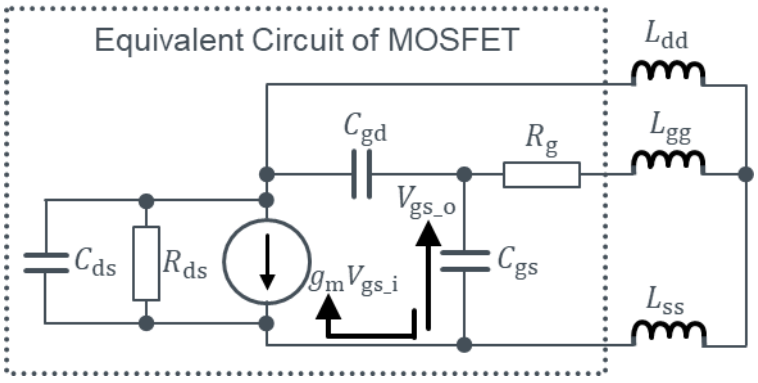


Electric vehicle　Traction inverter　Power module　Oscillation between parallel-connected dies

1. Basic theory

1-1. Mechanism of oscillation

It is known that the equivalent circuit in Fig.1 can be used to evaluate switching devices connected in parallel for the stability analysis [1]. Here, L_{dd}, L_{gg}, and L_{ss} are parasitic inductances including mutual inductances [2]. R_{ds} is a differential resistance during a switching transient period. For this circuit, a Bode diagram as shown in Fig.2 can be obtained from investigation of the open loop characteristics from V_{gs_i} to V_{gs_o} using PLECS®. It can be seen in Fig.2 that, since the second pole frequency ω_{p2} and the zero frequency ω_z are far apart, their phase falls to -180° or less between them. According to Nyquist stability criterion, an oscillation could occur with a phase of -180° or less when the gain is 0 dB. This poses an oscillation risk in modules with parallel connected dies.



L_{dd}: Drain to Drain Inductance
L_{gg}: Gate to Gate Inductance
L_{ss}: Source to Source Inductance
R_g : Gate Resistance
R_{ds}: Drain − Source Resistance (Differential Resistance)
C_{gd}: Gate − Drain Capacitance
C_{gs}: Gate − Source Capacitance
C_{ds}: Drain − Source Capacitance
g_m: Transconductance

Fig.1 Equivalent Circuit of Parallel Oscillation

No. 67AN027E Rev.001
August 2024

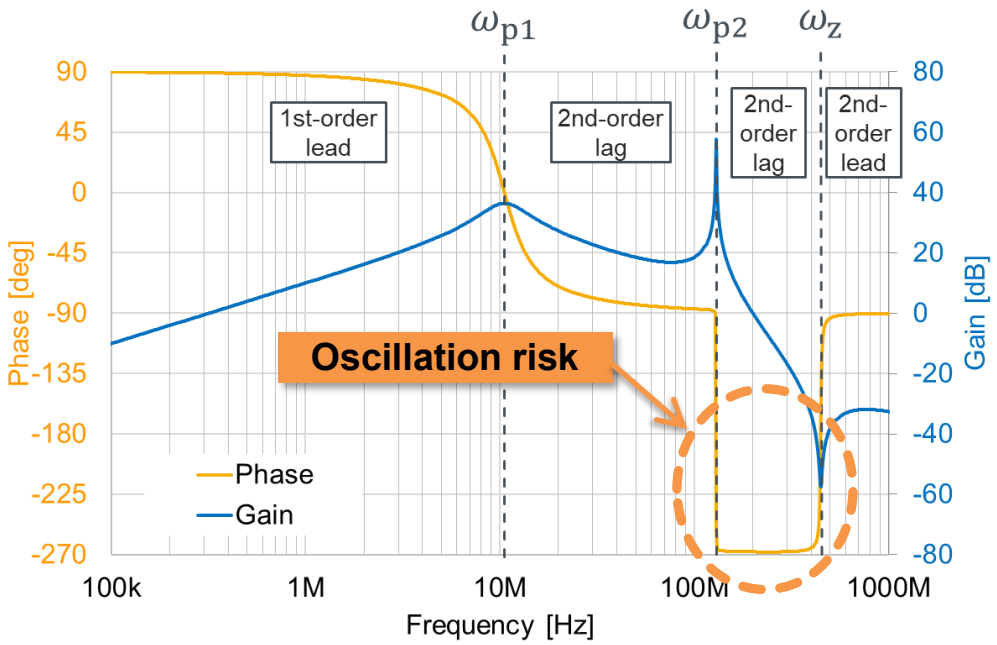


Fig.2 Simulated Bode Diagram of the Circuit shown in Fig.1

The Bode diagram in Fig.2 can be divided into the 1st-order lead, 2nd-order lag, 2nd-order lag, and 2nd-order lead areas in order starting from low frequency side according to the pole frequencies ω_{p1}, ω_{p2}, and the zero frequency ω_z. Therefore, $G(s)$, the open-loop transfer function for this system, can be expressed with the following equation:

$$G(s) = \frac{sK \cdot {\omega_{p1}}^2 {\omega_{p2}}^2}{{\omega_z}^2} \cdot \frac{(s^2 + 2\zeta_z \omega_z s + {\omega_z}^2)}{(s^2 + 2\zeta_{p1}\omega_{p1} s + {\omega_{p1}}^2)(s^2 + 2\zeta_{p2}\omega_{p2} s + {\omega_{p2}}^2)}$$

where K is the differential coefficient and ζ_{p1}, ζ_{p2}, and ζ_z are the damping factors at ω_{p1}, ω_{p2}, and ω_z, respectively. These parameters can be approximated as follows [3]. In this document, the operator "//" in ω_{p2} and ζ_{p2} represents parallel, which is defined as A//B = (A•B)/(A+B).

$$K = g_m \cdot L_{ss}$$

$$\omega_{p1} = \frac{1}{\sqrt{(L_{ss} + L_{gg})C_{gs}}} \qquad \zeta_{p1} = \frac{R_g}{2}\sqrt{\frac{C_{gs}}{L_{ss} + L_{gg}}}$$

$$\omega_{p2} = \frac{1}{\sqrt{(L_{dd} + L_{gg}//L_{ss})C_{ds}}} \qquad \zeta_{p2} = \frac{1}{2R_{ds}}\sqrt{\frac{(L_{dd} + L_{gg}//L_{ss})}{C_{ds}}}$$

$$\omega_z = \frac{1}{\sqrt{(L_{dd} + L_{gg})C_{gd}}} \qquad \zeta_z = \frac{R_g}{2}\sqrt{\frac{C_{gd}}{L_{dd} + L_{gg}}}$$

1-2. Approach for suppressing oscillations (improving phase margin)

Oscillation can be suppressed by increasing the phase margin and reducing the gain. However, it is very difficult to reduce the gain for modules with dies connected in parallel. Therefore, increasing the phase margin is most effective as a fundamental countermeasure.

Fig.3 explains why it is difficult to reduce the gain. In 2nd-order lag system, a gain peak appears if the ζ_{p2} value is smaller than $1/\sqrt{2}$. The peak height is determined by ζ_{p2} (the smaller the ζ_{p2} value, the steeper and higher the gain peak). Furthermore, the value of R_{ds} in ζ_{p2} can be as large as several kΩ since it is a differential resistance during a switching transient period as explained in 1-1. Since R_{ds} is large, the ζ_{p2} value is very small compared with $1/\sqrt{2}$. As a result, the gain peak becomes very high. As described above, it is difficult to reduce the gain due to a high gain peak. Therefore, increasing the phase margin is effective for suppressing oscillation.

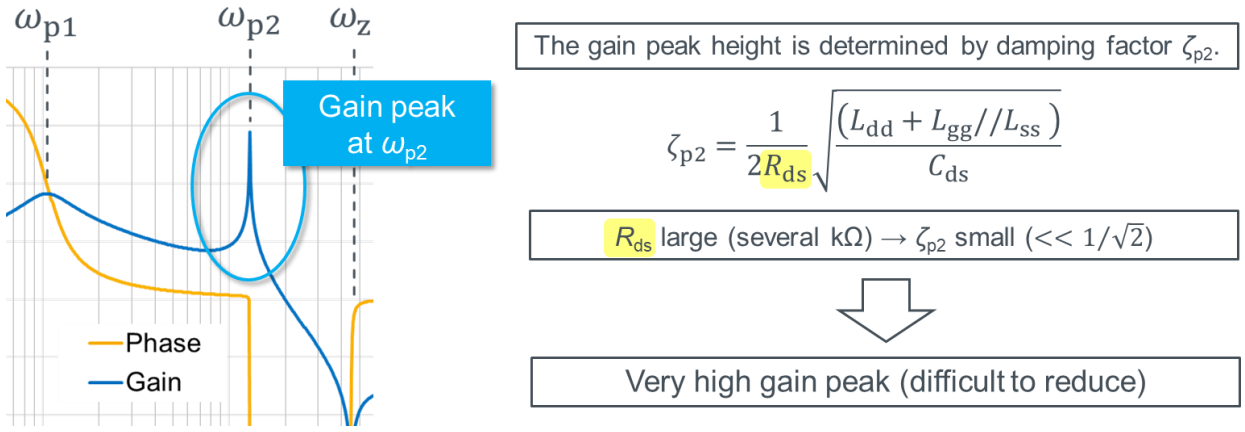


Fig.3 Explanation why it is difficult to reduce the Gain.

Now, what should be done to increase the phase margin ? As explained in 1-1, the phase falls below -180° if ω_{p2} and ω_z are far apart. In other words, the phase margin can be increased by moving ω_{p2} and ω_z closer to each other. For general modules with parallel dies, $\omega_{p2} < \omega_z$ and $\omega_{p2}/\omega_z < 1$ hold. Therefore, increasing the phase margin by moving ω_{p2} and ω_z closer to each other means increasing the ω_{p2}/ω_z ratio closer to 1.

Fig.4 shows how the phase characteristics are changed with the change in the ω_{p2}/ω_z ratio. As shown in Fig.4, if the ω_{p2}/ω_z ratio is increased, the phase margin is increased, enabling the oscillation suppression. If ω_{p2}/ω_z is improved to ≥1, no oscillation occurs, theoretically.

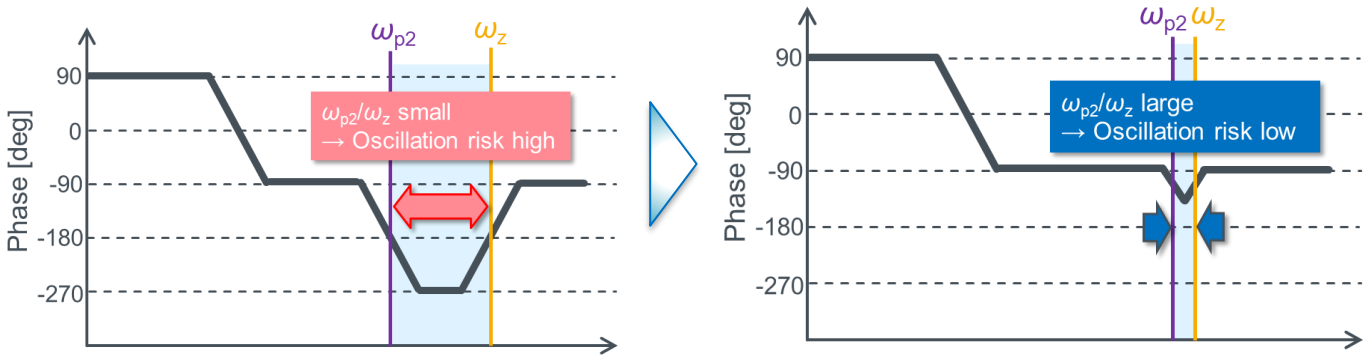


Fig.4 Phase margin improvement with increase in ω_{p2}/ω_z

Fundamental countermeasure against oscillation:
Increasing the phase margin (increasing the ω_{p2}/ω_z ratio)

1-3. Actual parameters affecting the phase margin

1-2 explains that the separation between ω_{p2} and ω_z (ω_{p2}/ω_z ratio) can significantly affect the phase margin. Now, more specifically, which parameters should be changed to change the ω_{p2}/ω_z ratio? This section provides detailed explanations about actual parameters that can affect the ω_{p2}/ω_z ratio.

As explained in 1-1, ω_{p2} and ω_z can be expressed with the following equations.

$$\omega_{p2} = \frac{1}{\sqrt{(L_{dd} + L_{gg}//L_{ss})C_{ds}}} \qquad \omega_z = \frac{1}{\sqrt{(L_{dd} + L_{gg})C_{gd}}}$$

Calculating the ω_{p2}/ω_z ratio from these equations results in the following relational expression.

$$\frac{\omega_{p2}}{\omega_z} = \sqrt{\frac{C_{gd}}{C_{ds}} \times \left(\frac{\frac{L_{gg}}{L_{ss}}}{\frac{L_{dd}}{L_{ss}} + \frac{L_{dd}}{L_{gg}} + 1} + 1 \right)}$$

From the equation of the ω_{p2}/ω_z ratio in the previous page, it can be seen that C_{gd} and L_{gg} should be increased and C_{ds}, L_{ss}, and L_{dd} should be decreased as shown in Fig.5 to increase the ω_{p2}/ω_z ratio and thereby the phase margin.

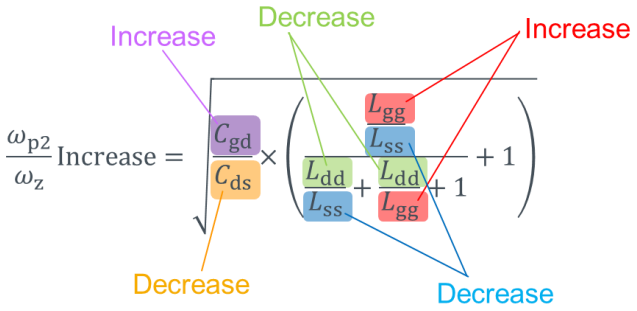


Fig.5 How to change the each parameters to increase ω_{p2}/ω_z ratio

However, for actual modules, the effect of L_{dd} on the ω_{p2}/ω_z ratio is very small compared with other parameters. Therefore, it is effective to adjust parameters other than L_{dd} to increase the phase margin.

To improve the phase margin:

Increasing C_{gd} and L_{gg} and decreasing C_{ds} and L_{ss}

Furthermore, since C_{gd} and C_{ds} are inherent capacitance in the MOSFET, it is realistically difficult to change these parameters afterward. Therefore, the most important countermeasure for suppressing oscillation is design of L_{gg} and L_{ss}, i.e., the module layout design.

The most important countermeasure for the oscillation suppression is

" Module Layout Design"

The larger the C_{gd} value, the better it is in terms of increasing the phase margin. However, as exclusive events of increase in C_{gd}, the switching-loss and the risk of self-Turn-ON are also increased, that is making the well-balanced device design more challenging.

2. Parasitic inductances in module L_{dd}, L_{gg}, and L_{ss}

2-1. Definition of L_{dd}, L_{gg}, and L_{ss}

Fig.6 shows a diagram illustrating a definition of the parasitic inductances in the module (L_{dd}, L_{gg}, and L_{ss}) that can affect the phase margin (ω_{p2}/ω_z ratio). Simply put, L_{dd}, L_{gg}, and L_{ss} are parasitic inductances that exist between the terminals of the dies connected in parallel. Since Fig.1 shows one side viewed from the middle point, the values of L_{dd}, L_{gg}, and L_{ss} in Fig.1 are half of those in Fig.6. Be aware of this point when performing the stability analysis using Fig.1.

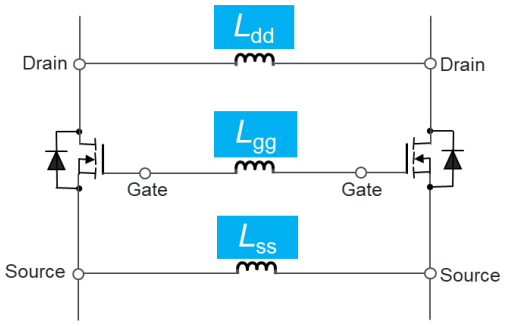


Fig.6 Definition of Each Parasitic Inductance L_{dd}, L_{gg} and L_{ss}

2-2. L_{dd}, L_{gg}, and L_{ss} in module layout

Using the module layout in Fig.7 as an example, this section explains which parts of the layout correspond to L_{dd}, L_{gg}, and L_{ss} in Fig.6 above. Although the High-side is explained as an example, the approach is the same for the Low-side. The black lines connected with the dies in the figure represent bonding wires. In addition, the negative side of the gate drive wiring is omitted for the sake of explanation (the same applies to the following layout diagrams).

In the right panel of Fig.7, the parts shown in red for L_{gg}, blue for L_{ss}, and green for L_{dd} correspond to the respective parasitic inductances. L_{gg} is nearly equal to the parasitic inductance of the wires. L_{ss} is a combined inductance of the wires connected with the dies and the copper foil part that connects them. L_{dd} is a combined inductance of the two paths (upper and lower) circumventing the gate pin.

For a SiC MOSFET die, the electrodes (Gate, Drain, and Source) are generally placed as shown in Fig.8.

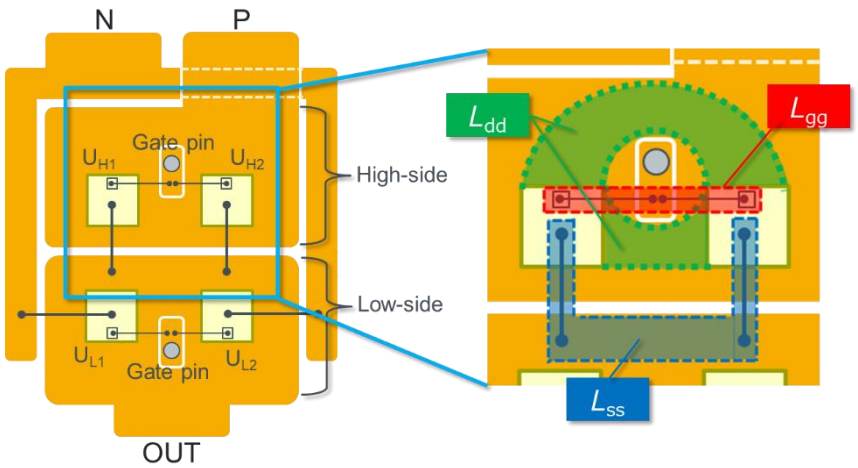


Fig.7 Example of Each Parasitic Inductances on an actual Module Layout

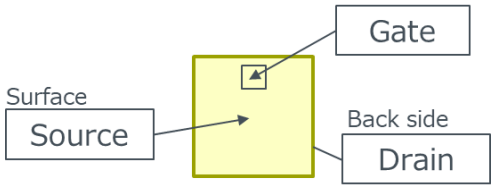


Fig.8 Typical Electrode Arrangement in a SiC MOSFET Die

3. Summary

- Oscillation can be suppressed by increasing the phase margin and reducing the gain. However, increasing the phase margin is most effective as a fundamental countermeasure (because it is difficult to reduce the gain due to the occurrence of a gain peak of the 2nd-order lag at the second pole frequency ω_{p2}).
- The ω_{p2}/ω_z ratio is an indicator of the phase margin. The larger the ω_{p2}/ω_z ratio, the higher the phase margin, resulting in more stability.
- To increase the phase margin by increasing the ω_{p2}/ω_z ratio, increase C_{gd} and L_{gg} and decrease C_{ds} and L_{ss} conversely.
- It is difficult to adjust C_{gd} *and* C_{ds} afterward because they are inherent capacitances in the device. Therefore, in order to increase the phase margin, it is important to appropriately design the parasitic inductances in the module (i.e., its layout).

4. References

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