SiC MOSFET

SiC MOSFET Layout Design Considerations

SiC MOSFETs are used as switching devices in power conversion applications. With their fast switching capabilities, they are operated at exceedingly high speeds. However, various countermeasures are needed to prevent surges in gate-source and drain-source voltages and false-point arcs in bridge configurations. This application note describes considerations for board layout design using SiC MOSFETs in discrete packages.

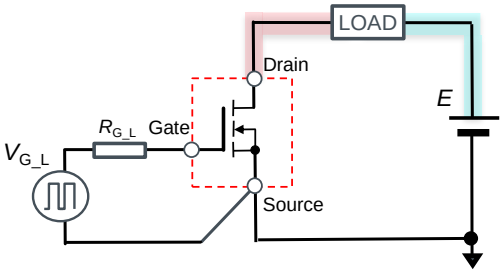
1. Coexistence of high and voltage circuits and drive circuits

SiC MOSFETs convert high voltages to levels required for by the interconnected load or system. A voltage-type drive circuit is typically used to turn on and off the high-voltage circuit by driving the gate terminals of the SiC MOSFET with around 15 to 20 V. Therefore, on a board where SiC MOSFETs are mounted, there is usually a mixture of high-voltage circuits and low-voltage drive circuits.

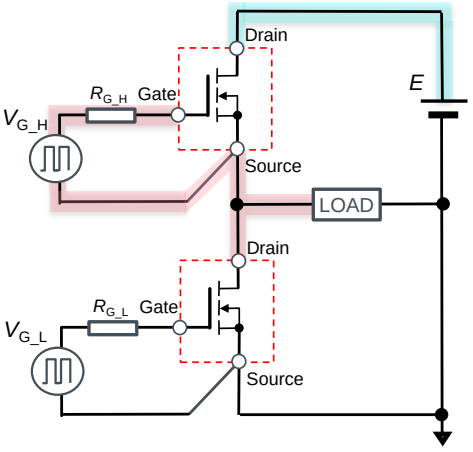
Figure 1 shows typical converter topologies using SiC MOSFETs. Figure (a) is a single-ended type, (b) is a half-bridge type, and (c) is a full-bridge type. The blue shaded area in the figure is the high-voltage part with respect to ground (▼), and the red area highlights low voltage circuitry that is exposed to high-speed switching between high-voltage and ground potentials. To minimize the effect of radiated noise due to current changes and high dv/dt, it is necessary to partition the high-voltage circuit from the drive circuit as much as possible.

In addition, due to the high dv/dt, common mode currents tend to flow. Parasitic capacitances and parasitic inductances must be considered. Furthermore, since heat dissipation of SiC MOSFETs is also an important design element, it is necessary to design a board layout that considers the cooling method. Manufacturing and assembly ease should also be considered during design.

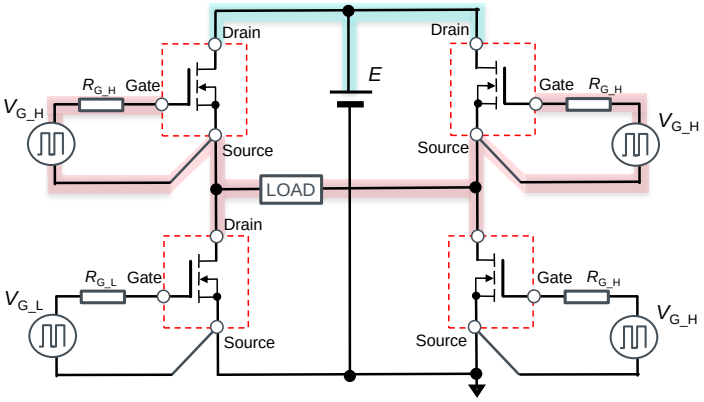
This document details points to be considered when designing the board layout to maximize the performance of fast switching SiC MOSFETs.



(a) Single-ended type



(b) Half-bridge type



(c) Full-bridge type

Figure 1: Circuit example using SiC MOSFETs

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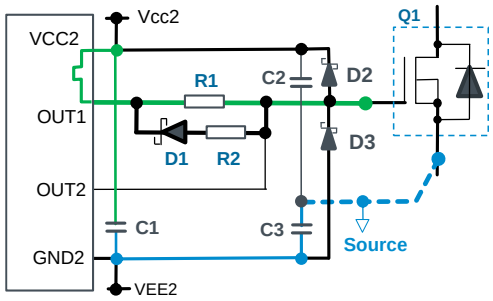
2. Minimization of drive circuit signal wiring length

The drive circuit is defined here as the circuit between the gate drive integrated circuit (IC) and SiC MOSFET. Its wiring inductance generates positive and negative surges due to the gate current generated during switching operation [1]. Therefore, the parasitic inductance must be minimized as much as possible by shorting the wiring length. The return path from the SiC MOSFET to the gate drive IC should be placed directly below the gate signal line from the gate drive IC to the SiC MOSFET as a full-area GND layer.

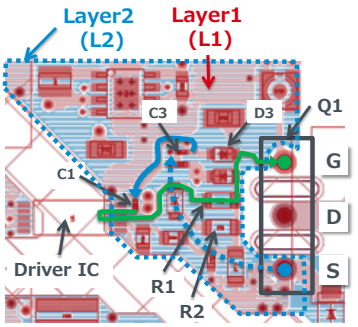
Indeed, the GND return path layer should occupy a different PCB layer than the layer of the gate signal. Minimizing the path and area of the gate current loop will reduce parasitic capacitances and inductances. As result, the circuit will be more robust against electrical noise during switching of SIC MOSFET.

Figure 2 shows the drive circuit and its layout on ROHM's evaluation board for fourth generation SiC MOSFETs, P04SCT4018KE-EVK-001 [2]. This evaluation board uses a 3-pin MOSFET, i.e., in a TO-247N package.

The SiC MOSFET drive power is propagated in the space formed by the outward, green path from the BM61S41RFV-C gate drive IC and the return blue path from the SiC MOSFET.



(a) Driving circuit



(b) Layout

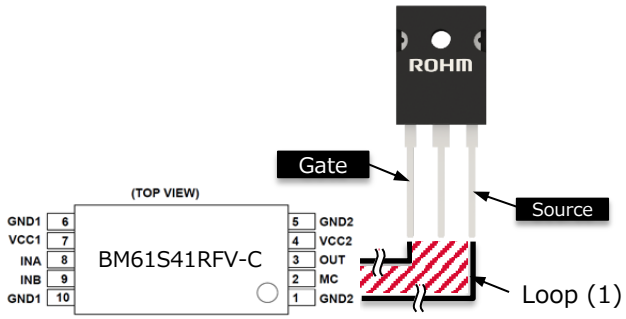
Figure 2: TO-247N driver circuit and layout example

To efficiently integrate R1 and R2, wiring from the OUT1 terminal to the gate (G) terminal of the SiC MOSFET is placed on the top layer (Layer1). The wiring from the source (S) terminal of the SiC MOSFET to the GND2 terminal of the gate drive IC is completed on bottom layer (Layer2), directly below Layer1.

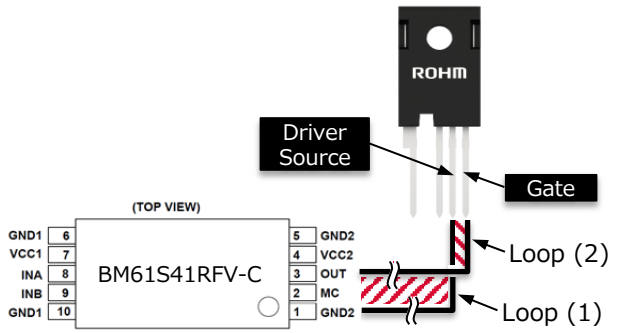
The drive circuit shown here uses a gate drive IC that does not have a dedicated terminal for negative bias voltage, VEE2, even though the design includes a negative bias power supply. So, the return path passes through Layer2 to bypass capacitor C3, and then through C3 mounted the GND2 terminal of the gate driver IC. Both C3 and the gate driver IC are located on Layer1.

3. Gate drive IC pin assignment challenges

In the case of the commonly used 3-pin TO-247N, the G and S terminals are on opposite sides of the package, and the separation between return path and drive signal can only be reduced to an extent. Therefore, radiation noise due to large current change flowing between D and S of SiC MOSFET is large and induces unwanted voltages in the gate drive circuit. The gate drive IC is not affected by noise with a copper pour in Layer2 utilized in the gate current return from the S terminal to the gate drive IC.



(a) TO-247N



(b) TO-247-4L

Figure 3: Example of wiring layout for drive circuit

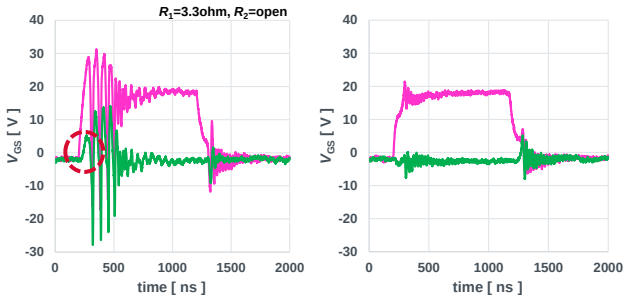
In many cases, conventional gate drive ICs have pin assignments that allow the TO-247N to be laid out with the driver circuit on a single surface, as shown in Figure 3(a). While the TO-247-4L, a 4-pin package, can greatly improve switching performance, it has pin assignments opposite to those of the driver IC, as shown in Figure 3(b). The wires to gate and source terminals cross and, thus, cannot be laid out in a single plane or PCB layer. Please note that the BM61S41RFV-C offers GND2 pins on both sides of the OUT pin, eliminating this issue.

Luckily, the induced voltages due to the loops (1) and (2) formed by the OUT and GND2 signals are of opposite polarity. For a successful design, the areas of loops 1 and 2 must be equal and minimized as much as possible. This is because the dI_D/dt of TO-247-4L is exceptionally large, and therefore, the induced magnetic flux change, $d\Phi/dt$, crossing the loop area will generate a voltage electromotive force. Then, a positive or negative surge voltage proportional to this loop area is induced between G and S of the SiC MOSFET, causing oscillation that may lead to device breakdown. Therefore, to minimize the loop area formed by the OUT and GND2 signals, the return path from the SiC MOSFET to the gate drive IC should be a copper pour on Layer2.

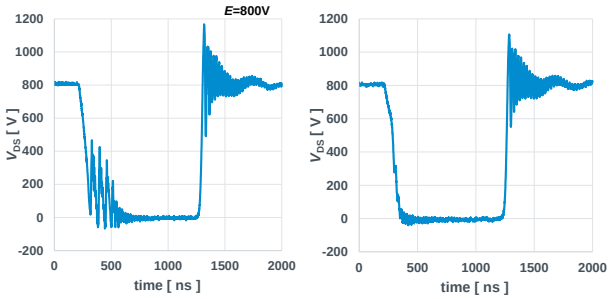
Figure 4 shows measurements of a comparison using a poorly designed layout (left side) and well-designed layout (right side). The switching waveforms are measured from a circuit in a bridge configuration, like Figure 1(b). The poorly designed layout uses a simple wire for the return path and the well-designed layout uses a copper pour for the return path. The low-side SiC MOSFET is switched, and waveforms are collected in which (a) shows gate-source voltages, (b) shows the low-side MOSFET drain-source voltage, and (c) is the drain current waveform of the low-side MOSFET.

Fig. 4(a) shows the gate voltage waveforms of both low-side (pink) and high-side (green) waveforms. The high-and low-side gate voltage of the poorly-designed layout rises during the turn on transient of the low side MOSFET, as marked with a red dotted circle. This has the effect of causing the high-side MOSFET, which should be turned off, to turn on, causing a short circuit for a short time duration.

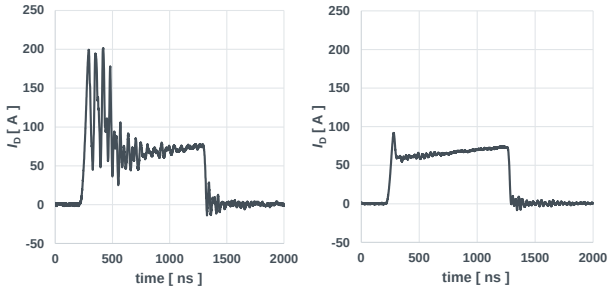
The high-side MOSFET current flows and the corresponding increased plateau voltage causes the high-side MOSFET to turn off, after which severe voltage oscillations appear in the gate-source voltage waveform. The waveforms in the right plots, from the well-designed PCB, exhibit almost zero oscillatory behavior.



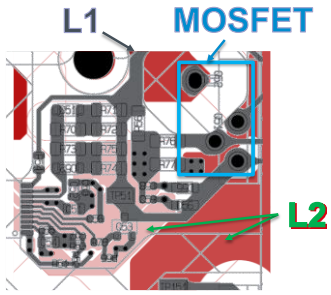
(a) Gate-source voltage waveforms from low-side (pink) and high-side (green) devices



(b) Drain-source voltage waveform



(c) Drain current waveform



(d) Poor layout example, with a non-solid return path

Figure 4: Switching waveforms during using (left) poorly-designed and (right) well-designed layouts

4. Gate surge protection component location priorities

SiC MOSFETs are often used with narrower margins in the gate driving voltage rating range than silicon MOSFETs. When used in a bridge configuration, voltage surges that exceed the gate rating occur if gate surge countermeasures are not implemented. Therefore, it is highly recommended to include gate surge protections in the hardware design. Gate surge protection circuits include the following [3].

- Active miller clamp
- Diode clamp, for both positive surge and negative surge
- Capacitor between MOSFET gate and source terminals

There are two types of active miller clamp circuits. One is built into the gate drive IC, and another is an external-type with a MOSFET for active miller clamping, both of which require a wiring length of no more than approximately 20 mm away from the SiC MOSFET, to remove a short gate surge period of approximately several tens of ns.

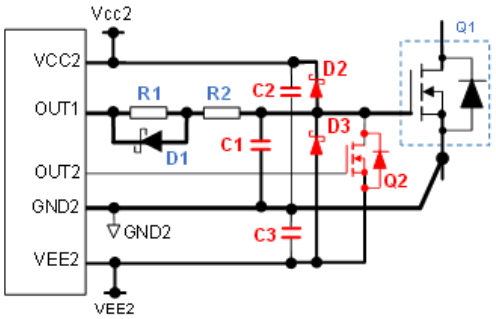
The specification of the diode clamp circuit is important. It is necessary to select a diode integrated in a small, low inductance package. Additionally, a bottom-electrode type is more suitable than a gull-wing type.

The order of priority for layout near SiC MOSFETs is defined:

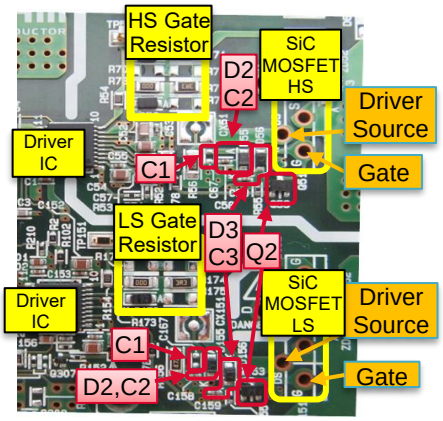
1. Active miller clamp circuit
2. Clamp diode for negative surge
3. Clamp diode for positive surge
4. Gate-source capacitor

Figure 5 shows an example of a gate surge protection circuit on a half bridge evaluation board for TO-247-4L package and a picture of the board [4]. An isolated gate driver is used for each MOSFET. An external MOSFET (Q2) is included to realize an external-type active miller clamp. A clamp diode (D3) and its bypass capacitor (C3) for negative surge, a clamp diode (D2) and its bypass capacitor (C2) for positive surge, and a gate-source capacitor (C1) are placed according to the order of priority defined above.

Figure 6(a) shows the L1 layer layout and Figure 6(b) shows the L2 layer layout, showing the active miller clamp circuit path via Q2 to VEE2 (yellow) and the negative surge clamp diode path via D3 and C3 to VEE2 (orange). The protection circuit location is selected to minimize the distance between the SiC MOSFET gate and driver-source pins.

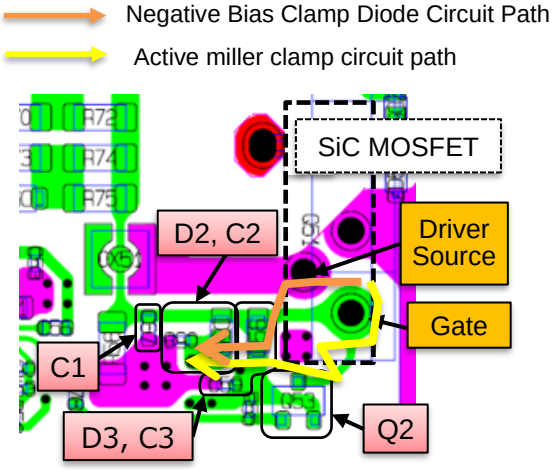


(a)

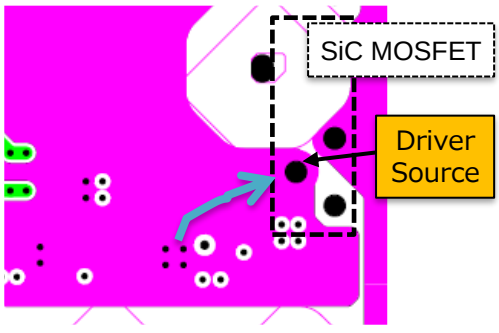


(b)

Figure 5: Gate surge protection circuit and layout example



(a) Gate current outward path on Layer1



(b) Gate current outward path on Layer2

Figure 6: Gate surge protection circuit path (round trip)

5. Drive and high voltage circuit separation

As shown in Figure 1, SiC MOSFETs are switched between the high-voltage power supply *E* and GND in a bridge circuit. High-impedance circuits and general logic circuits operating at 5 V or 3.3 V are susceptible to radiation noise, generated in the switching area where large currents are repeatedly turned on and off, and to common-mode noise due to high dv/dt. So, the gate drive circuit and the high-voltage area should be physically separated as much as possible.

Figure 7 shows an example layout for a bridge circuit when two SiC MOSFETs in the TO-247-4L package are used in parallel for each switch position. The right side is the high-voltage side, and the left side is the low-voltage, gate driving side.

The dashed green line in Figure 7 illustrates how the high- and low-voltage domains are separated. Furthermore, the gate drive circuit return path is formed by the L2 layer, connected as a single-point at the driver source (DS) pin.

The area surrounded by bold red lines is the switching area, which switches between *E and* GND at high speed. The pattern layout of the switch node (OUT) should overlap as little as possible with the layout of *E* and GND sections. This is because additional, parasitic capacitance is formed in proportion to the overlapped area between PCB layers.

In this MOSFET bridge circuit, this parasitic capacitance would act in parallel to the SiC MOSFET output capacitance, C_{oss}, leading to increased switching losses.

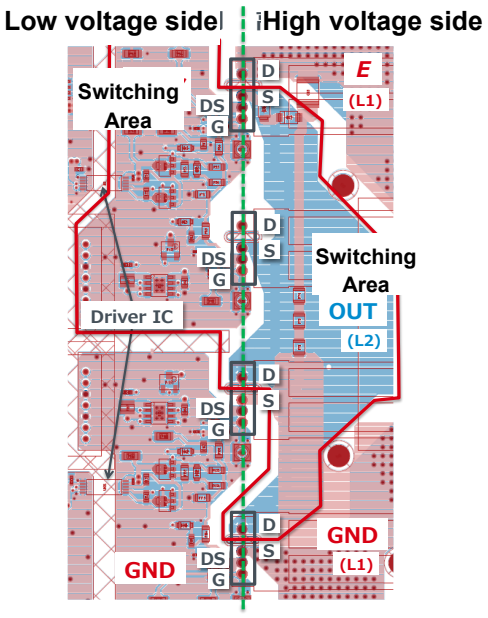


Figure 7: Layout example when SiC MOSFETs in TO-247-4L packages are connected in parallel

6. Isolated power supply precautions

Unless a non-isolated method such as a bootstrapping is used to drive high-side MOSFETs, an isolated power supply is required. Normally, an isolation transformer would be included in the power supply for the high-side MOSFET. For this approach, the charging and discharging current of the coupling capacitance formed between transformer primary and secondary windings must be minimized.

Figure 8 shows the common-mode current path through the high-side drive power supply. Normally, the primary control signal side (▽), and the secondary high-voltage side (▼) are separated from frame GND (⏚). A common-mode current is the current flowing through the coupling capacitance of the high-side MOSFET during the switching transient along the red dashed line shown in the figure.

The switching speed of SiC MOSFETs is much faster than that of silicon MOSFETs, resulting in a large dV_{DS}/dt. The peak value of the common mode current is proportional to this dV_{DS}/dt and can reach several amperes. The common-mode current not only induces malfunction of the primary circuit and primary power supply, V_{CC1}, but may also cause unexpected system malfunctions impacting controllers on the primary side.

In such cases, connecting the GND of the primary side (▽) and the secondary side (▼) as shown in the dashed blue line in the figure may suppress the common mode current flowing to ground and eliminate the problem.

The standard primary-to-secondary coupling capacitance of isolation transformers used for isolated power supplies is 10 pF or less. 5 pF or less is preferable for SiC MOSFET switching applications.

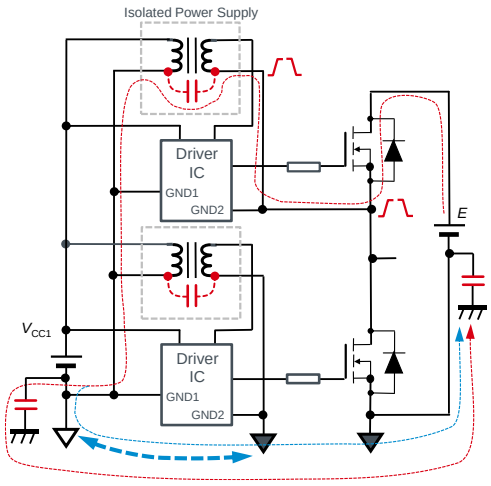


Figure 8: Common-mode current path through the high-side drive power supply

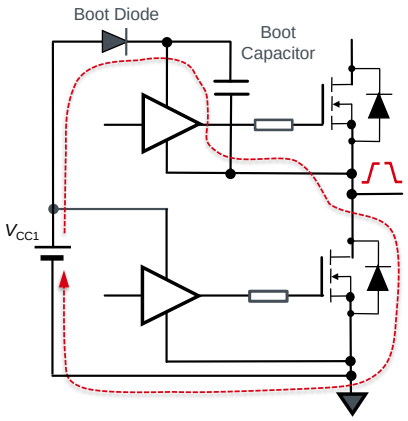


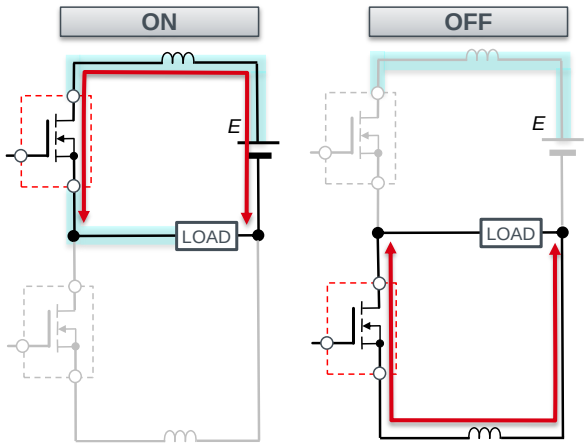
Figure 9: Charging path to the bootstrap capacitor

For bootstrapping, the bootstrap capacitor charging path requires attention. This path is shown in Figure 9. To charge the bootstrap capacitor, the GND of the power supply that supplies the charging current, V_{CC1}, must be connected to the GND of the high-voltage circuit. To minimize the effect of noise on the high-voltage circuit side, a single-point ground is applied near the source terminal of the low-side MOSFET.

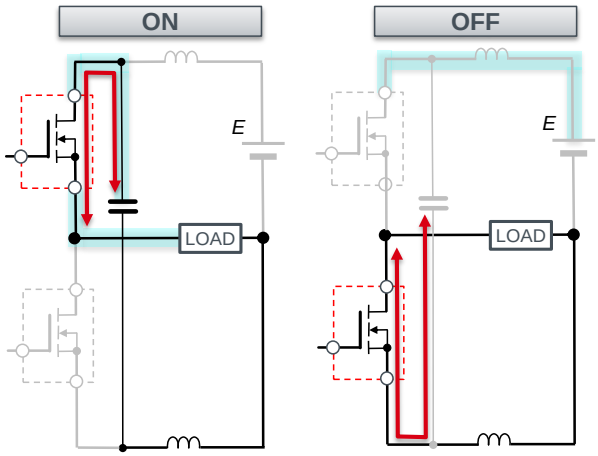
7. High-voltage power supply integration

During the turn off transient of the SiC MOSFET, over voltages occur due to stray inductances in the power loop and high di/dt. To minimize this, DC link capacitors, such as film capacitors and multi-layer ceramic capacitors, are included as bypass capacitors to minimize this stray inductance, reducing the surge voltage applied to the SiC MOSFETs.

Figure 10 illustrates switching current paths with and without DC link capacitors. Figure 10(a) shows the case without DC link capacitor and (b) shows the case with DC link capacitor. The red lines indicated by the arrows show the switching of current paths during ON and OFF transitions. Note: The wiring to and from LOAD is regarded as part of the LOAD and is not affected by DC link capacitors because the switching operation of the SiC MOSFET does not manipulate the current through LOAD.



(a) Without DC link capacitor



(b) DC link capacitor available

Figure 10: Switching current path switching

As the figure shows, placing DC link capacitors as close as possible to SiC MOSFETs minimizes the wiring inductance. Of course, the selected DC link capacitor(s) should have a minimal equivalent series inductance (ESL). It is furthermore desirable to lay out DC link capacitor on the same PCB as the SiC MOSFETs.

For dimensioning the DC link, the values shown in Equation (1) for capacitance $C_{DC\ link}$ and Equation (2) for ripple current $I_{DC\ link}$ should be used as a guide.

$$C_{\mathrm{DC\ link}} > \frac{I_{D(MAX)}}{\Delta V_E} t_r \quad (1)$$

$$I_{\mathrm{DC\ link,rms}} > I_{D(MAX)} \sqrt{\frac{t_r}{T_s}} \quad (2)$$

$I_{D(MAX)}$: Maximum load current

ΔV_E: Allowable voltage drop

t_r: Rise time

T_s: Period of MOSFETs switching frequency ($1/f_{sw}$)

$I_{D(MAX)}$ is the peak drain current flowing in SiC MOSFET at turn-on. ΔV_E is set to a value of about 1~2% based on the level of the high-voltage power supply *E*. t_r is a value under actual usage conditions and can be extracted from a datasheet.

Equation (1) is a guide for turn-on. Surge suppression should be considered separately for turn-off. For more information, please refer to "How to Design Snubber Circuits" [5].

Equation (2) is derived as only flowing constant I_{D_MAX} during t_r. There is no current flowing except during the t_r period.

8. Summary

SiC MOSFETs exhibit high-speed switching characteristics, even in high-voltage circuits. The breadth of their application is expanding, with their use a wide variety of circuits becoming common.

High-speed switching operation is prone to generate noise and other issues. The PCB layout of SiC MOSFET driver circuits and high-voltage circuits is particularly important to suppress these issues from the design stage. This report summarized these points. This application explained design criteria for the patterns and tracks on the board.

To extend the study of PCB layout for fast switching semiconductors, the reader is directed to a related reference, "PCB Layout Techniques of Buck Converters" [6].

References

[1] "Gate to Source Voltage Behavior in a Bridge Configuration"
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[2] "4th Generation SiC MOSFET Half Bridge Evaluation Board Product Specifications"
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[5] "Snubber circuit design methods"
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[6] "PCB Layout Techniques of Buck Converters"
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