SiC MOSFET

Gate-Source Voltage Surge Suppression Methods

Power semiconductors such as MOSFETs and IGBTs are used as switching components for various power supply applications and power lines. SiC MOSFETs, which have been increasingly adopted in recent years, operate at such a high-speed that changes the voltage and current during switching cannot be ignored due to the effects of the package inductance of the device itself and the wiring parasitic inductance of the surrounding circuits. In particular, the gate-source voltage may cause an unexpected positive or negative surge when the voltage or current of the device itself varies, thus, various countermeasures have been investigated. Therefore, this application note aims to present the best countermeasures while clarifying the causes of the surge that occurs between gate and source of the MOSFET.

Surge in Gate-Source Voltage

In the application note “Gate-source voltage behaviour in a bridge configuration” *1, we explained in detail the surge of gate-source voltage that occurs when switching device is turned on or turned off in a bridge configuration. Surge is generated not only on the switching side (LS) of the circuit but also on the non-switching (HS) depending on the voltage and current change of the switching side.

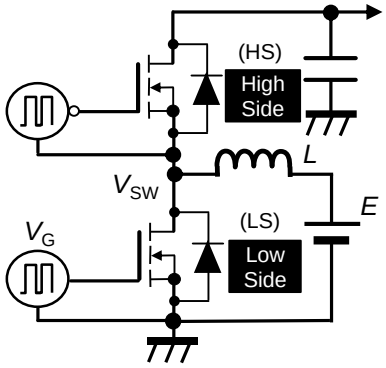


Figure 1: Synchronous rectification BOOST circuit

Figure 2 and Figure 3 show the behaviour of the gate-source voltage when LS is turned on and off, respectively. The horizontal axis denotes time, and the time periods Tk(k=1~8) are defined as follows:

T1: LS is ON, and I_D of the MOSFETs varies
T2: LS is ON, and V_{DS} of the MOSFETs varies
T3: LS is ON, and I_D and V_{DS} are nearly stable
T4: LS is OFF, and V_{DS} of the MOSFETs varies
T5: LS is OFF, and I_D of the MOSFETs varies
T4-T6: Dead time, LS is OFF until HS turns ON
T7: HS is ON（synchronous rectification）
T8: Dead time, HS is OFF until LS turns ON

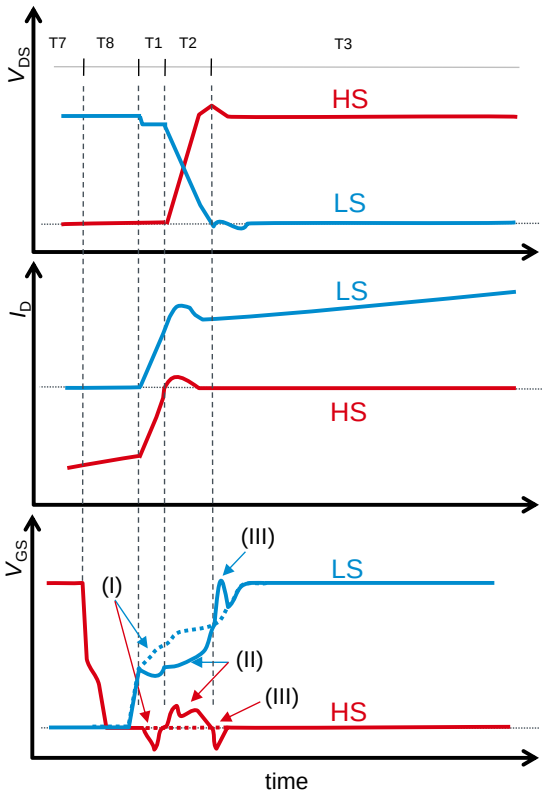


Figure 2. Gate-source voltage behaviour (turn-on)

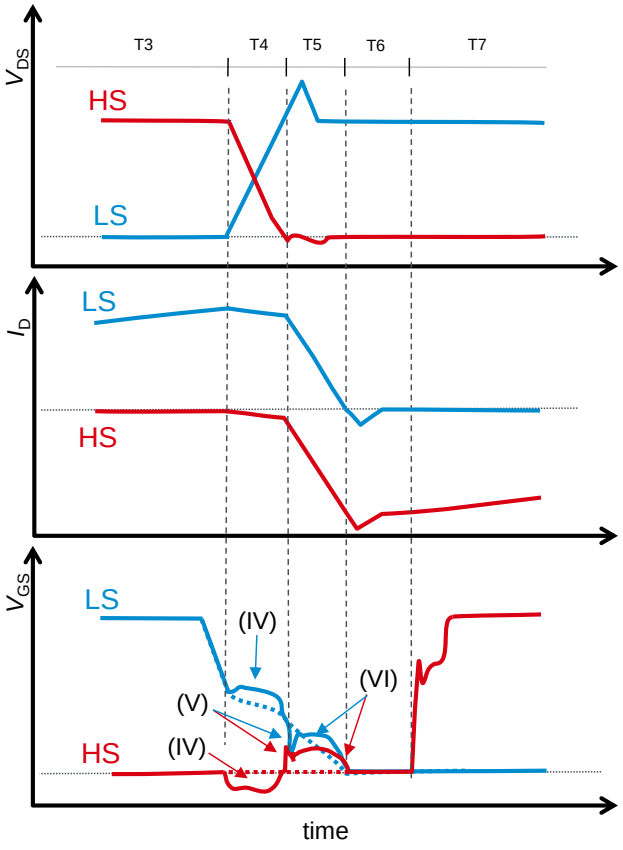


Figure 3. Gate-source voltage behavior (turn-off)

Event (I) to (IV) shown in Figure 2 and Figure 3 are caused by the following factors:

Event (I), (VI): Change in I_D of the MOSFET (dI_D/dt)
Event (II), (IV): Change in V_{DS} of the MOSFET (dV_{DS}/dt)
Event (III), (V): Change in V_{DS} stopped

Surge Suppression Circuit

As explained in the previous section, the positive surge of the gate-source voltage (V_{GS}) occurs on both the switching side and the non-switching side. However, the major concern is on the non-switching side (Figure 2 Event (II)). This is because, since the switching side is already turned on, if the positive surge voltage on the non-switching side exceeds the gate threshold voltage ($V_{GS(th)}$) of the MOSFET, self-turn-on occurs and a through current flows. However, because the trans-conductance of a SiC MOSFET is smaller than that of a Si-based MOSFET, excessive through current does not flow immediately. Therefore, even if a through current flows, there is basically no problem if the cooling capacity is sufficient and the $T_{j(max)}$ of the MOSFET is not exceeded. However, since it affects the overall system efficiency and is not in a favourable state, it is necessary to add a surge suppression circuit to avoid the voltage exceeding the $V_{GS(th)}$ of the MOSFET.

An example of the surge suppression circuit is shown in Figure 4.

In the same figure, a surge suppression circuit is added to a general MOSFET drive circuit, and its function is shown in Table 1.

In addition, VCC2 and VEE2 are the power on and power off for the drive circuit, respectively. OUT1 is the ON/OFF signal for the MOSFET, OUT2 is the control signal for Miller clamp, and GND2 is the GND of the drive circuit. Figure 4(a) shows the circuit when VEE2 is in use, and Figure 4 (b) shows the circuit when it is not in use.

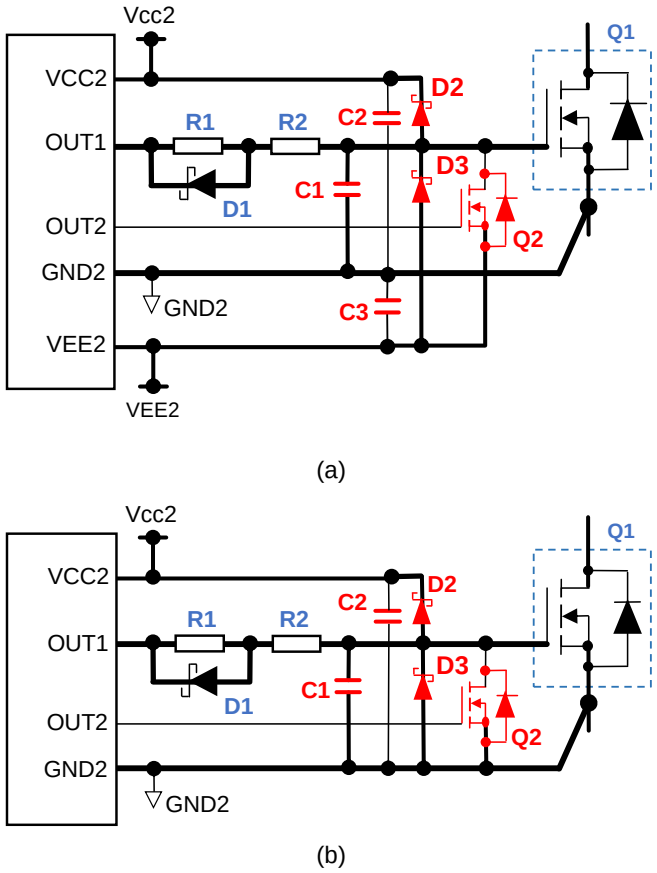


Figure 4. Positive surge suppression circuit
(a) Negative bias (with VEE2), (b) 0V bias (without VEE2) drive

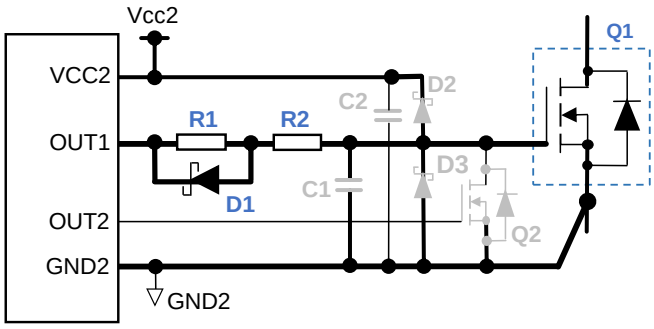
Table 1. Surge suppression circuit and its function

Function	Symbol	Details
Positive surge suppression	D2 (C2)	Positive surge suppression when switching side is turning on. (C2 is bypass capacitor)
Negative surge suppression	D3(C3)	Negative surge suppression on switching side and non-switching side. (C3 is bypass capacitor)
Positive surge suppression	Q2	Positive surge suppression on non-switching side.
Self-turn-on prevention	C1	Positive surge suppression on non-switching side

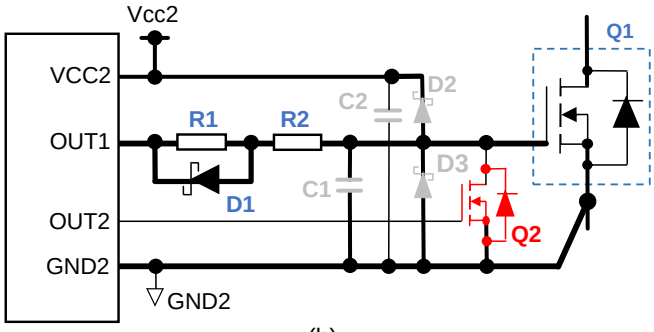
Since D2 and D3 normally absorb pulses of several ns and voltage need to be clamped at as low as possible, Schottky barrier diodes (SBD) are used. In addition, it is more effective to use low impedance bottom electrode type package such as SOD-323FL.

Positive Surge Voltage Countermeasures

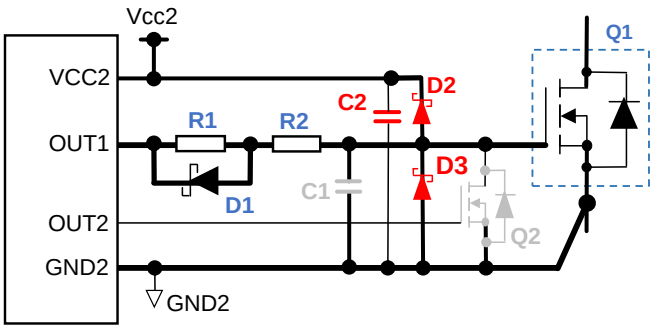
To suppress the positive surge of the non-switching side V_{GS} at event (II) shown in Figure 2, Q2 or C1 shown in Table 1 can be used.



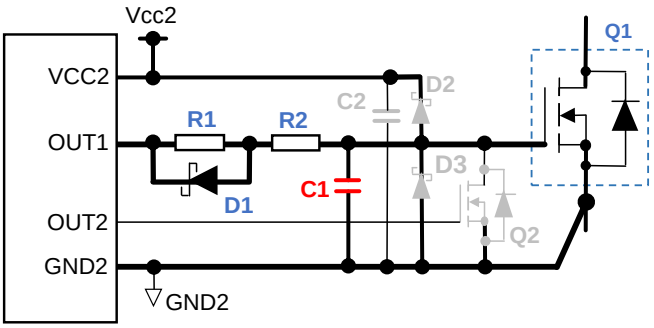
(a)



(b)



(c)



(d)

Figure 5. Surge suppression circuits verification

(a) no surge suppression circuit,

(b) Miller clamp MOSFET only,

(c) Clamp SBD only,

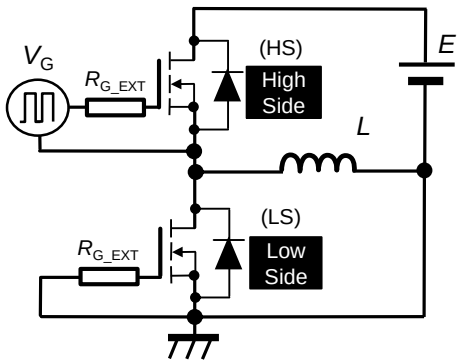
(d) Self-turn-on prevention capacitor only

In order to verify the effect of the surge suppression circuits, we implemented the circuit individually and observed the waveforms. ROHM's SiC MOSFET (SCT3040KR) was used for this purpose. Figure 6 shows the outline and general specifications of SCT3040KR.

V_{DSS}	1200 V
$R_{DS(on)}$	40 mΩ
I_D	55 A
P_D	262 W

Figure 6. SCT3040KR (4L) outline and general specifications

As shown in Figure 5, the effect of each circuit, (a) is no surge suppression circuit, (b) is Miller clamp MOSFET (Q2) only, (c) is clamp SBD (D2, D3, C2) only, and (d) is Self-turn-on prevention capacitor only was verified by performing the double pulse test shown in Figure 7.



E: 800V, L: 250uH, R_{G_EXT}: 10Ω

Figure 7. Double pulse test circuit

The waveforms at turn-on are depicted in Figure 8, the rows from the top to bottom display: switching side gate-source voltage (V_{GS_HS}), non-switching side gate-source voltage (V_{GS_LS}), drain-source voltage (V_{DS}), and drain current (I_D) for each surge suppression circuit: (a)no surge suppression circuit, (b)MOSFET for Miller clamping only, (c) SBD for clamping only, (e) Miller clamp MOSFET + clamp SBD using the surge suppression circuit shown in Figure 4(b).

As can be seen in Figure 8, it is clear that the positive surge voltage cannot be suppressed in the case where there is (a) no countermeasure circuit and in the case of (c) clamping SBD only is added. It can be observed that V_{GS_LS} rises and greatly exceeds the $V_{GS(th)}$, and I_D is larger compared to the ones with countermeasure circuits. This phenomenon, the so-called self-turn-on occurs at the non-switching side (in this case, LS MOSFET). It is therefore essential to implement countermeasure (b) to prevent this phenomenon.

However, to implement this countermeasure circuit, it is necessary to have a control signal for Miller clamp circuit drive. This signal needs to distinguish the drive timing while monitoring the V_{GS} voltage. Usually, this signal is equipped in the driver IC, but if you are using a driver IC without this driving function, the countermeasure (b) cannot be implemented.

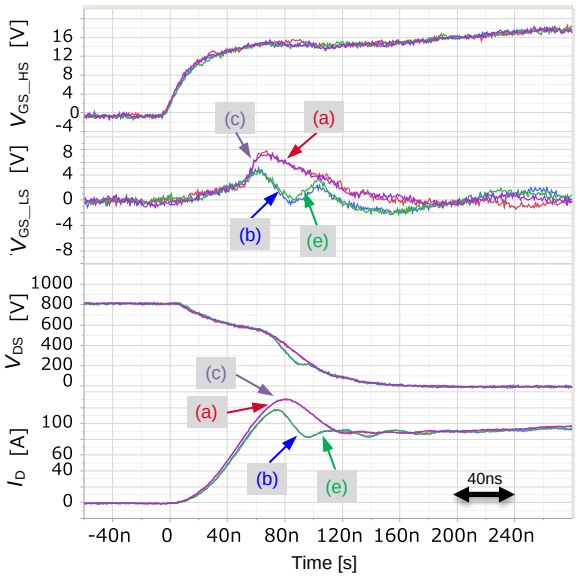


Figure 8. Turn-on waveforms

(a) no surge suppression circuit, (b)Miller clamp MOSFET only, (c)clamping SBD only, (e)Miller clamp MOSFET+ clamping SBD

In that case, alternatively you may add a self-turn-on prevention capacitor between gate and source of the MOSFET as shown in Figure 5(d) to suppress the surge.

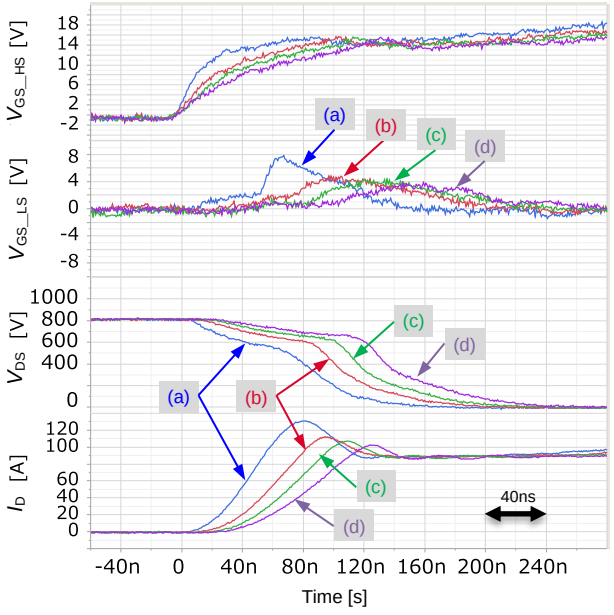


Figure 9.Turn-on waveforms when self-turn-on prevention capacitor is added

(a) no surge suppression circuit, (b) 2.2nF, (c) 3.3nF, (d) 4.7nF

Figure 9 shows the turn-on waveform when self-turn-on prevention capacitor is added. It can be observed that the rise of the V_{GS_LS} is smaller as well as the turn on surge of the I_D in (b), (c), and (d) when the capacitor is added compared to (a) no surge suppression circuit.

However, as can be seen from the I_D waveform, adding a self-turn-on ON prevention capacitor slows the turn-on operation and increases the switching loss. Therefore, it is important to select the value as small as possible. In this evaluation, 2.2nF was used, and it showed a sufficient effect.

Negative Voltage Surge Countermeasures

The negative surge during turn-off of the non-switching side V_{GS} at event (IV) shown in Figure 3 can be suppressed by using Q2 or D3 shown in Table 1.

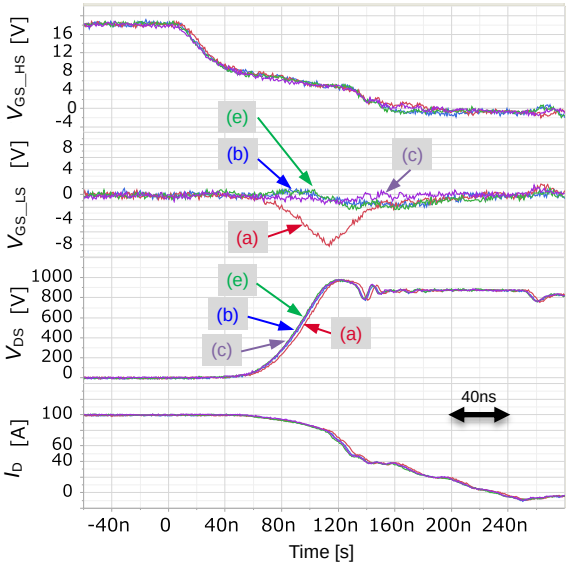


Figure 10. Turn-off waveforms

(a) no surge suppression circuit, (b) Miller clamp MOSFET only,

(c) Clamping SBD only, (e) Miller clamp MOSFET + clamping SBD

The waveforms at turn-off are depicted in Figure 10, like the one shown in Figure 8, the rows from the top to bottom display: switching side gate-source voltage (V_{GS_HS}), non-switching side gate-source voltage (V_{GS_LS}), drain-source voltage (V_{DS}), and drain current (I_D) for each surge suppression circuit: (a)no surge suppression circuit, (b)Miller clamp MOSFET only, (c) clamping SBD only, (e) Miller clamp MOSFET + clamp SBD, using the surge suppression circuit shown in Figure4(b). As can be observed from the waveforms, negative surge can be suppressed by using either one of the surge suppression circuits.

Moreover, as can be observed from the turn-off waveforms in Figure 11, negative surge cannot be suppressed by adding self-turn-on prevention capacitor. Therefore, if the surge suppression circuit (b) cannot be implemented, it is necessary to optimize the overall system efficiency by using the surge suppression circuits (c) and (d) together.

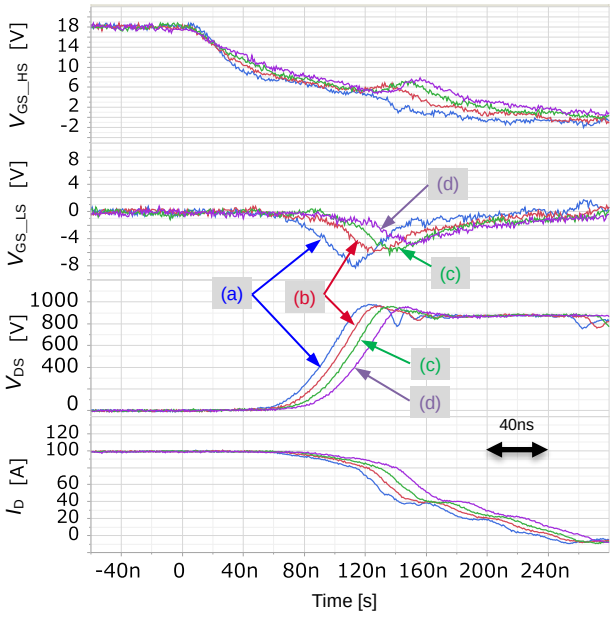


Figure 11. Waveforms at turn off when self-turn-on capacitor is added

(a) no surge suppression circuit, (b) 2.2nF, (c) 3.3nF, (d) 4.7nF

Precautions on suppression circuit layout

Figure 12 shows a layout example of the surge suppression circuit.

On this board, two MOSFETs (LS and HS) are arranged in a bridge configuration, and the gate terminal and driver source terminal are assigned below each MOSFET. The V_{GS} surge suppression circuit is placed closest to each gate terminal and connected at the shortest distance.

Figure 13 shows the layout of the surge suppression circuit. When multiple surge suppression circuits are implemented, the mounting position must first be determined with the highest priority given to the Miller clamp MOSFET (Q2). Next, the negative surge clamping SBD (D3) and its bypass capacitor

(C3), followed by the placement of the positive surge clamping SBD (D2) and its bypass capacitor (C2), and finally the-turn-on prevention capacitor (C1). This is because the distance where the Miller clamp MOSFET is placed greatly influences the suppression effect due to the wiring inductance, even by placing it a few centimeters away.

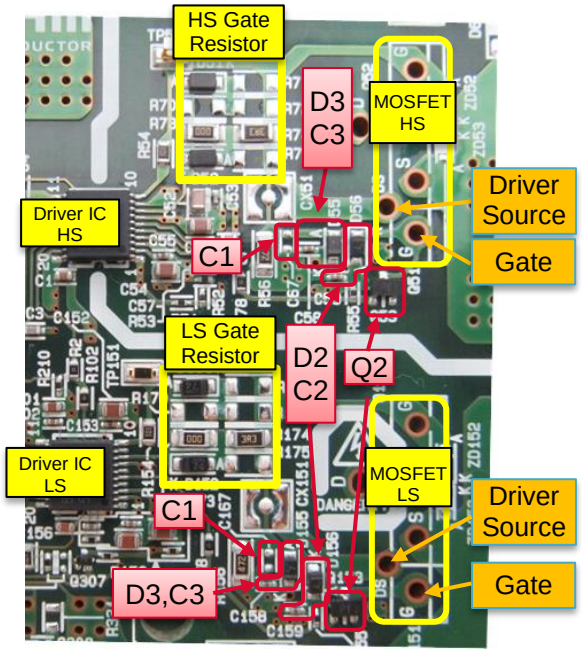


Figure 12. Layout example of the surge suppression circuit

Moreover, the wiring length of the surge suppression circuit return line (return line to the driver source terminal) and the loop created by the surge suppression circuit wiring should also be taken into account. This is because EMC noise generated in the I_D is large due to the effect of high-speed switching of the SiC MOSFET. It is therefore crucial to make the wiring loops as short as possible to prevent them from radiating the EMC noise.

The evaluation board used for this application note has a four-layer structure, and its return line is placed in the entire layer 2. By doing so, the return line can be placed directly under the surge suppression circuit, thus, minimizing the loop area.

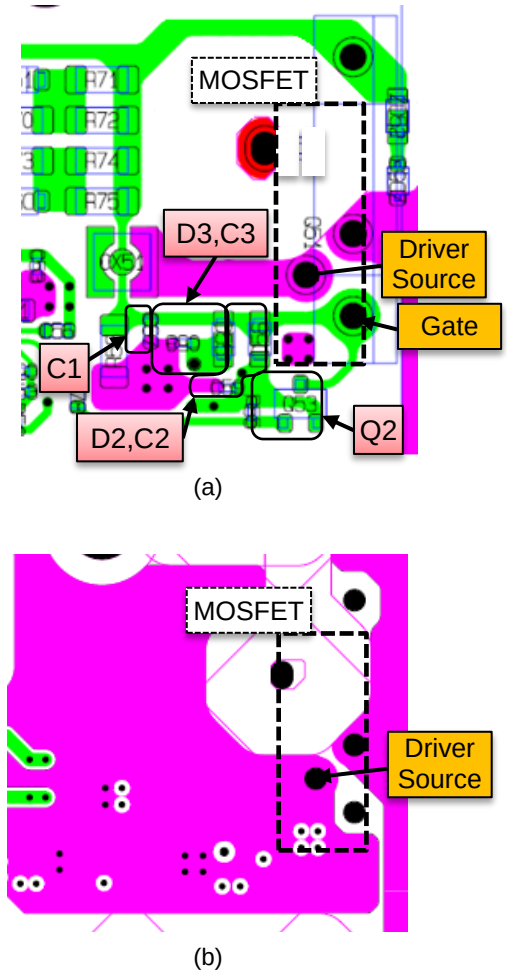


Figure 13. Surge suppression circuit layout
(a) Layer 1, (b) Layer 2

Note that the bypass capacitor for clamping the SBD is not required if the impedance from the drive power supply is sufficiently low, but in general the power supply source is often far, and the bypass capacitor is placed near the SBD. It is necessary to enable the SBD to operate with low impedance. In addition, as an indication, use a capacitor (0.1uF, 1.0 x 0.5mm size) with resonance point in tens of MHz band.

As described above, the gate signals of the SiC MOSFETs with the bridge configuration operate while the MOSFETs are related to each other, generating an unexpected voltage surge in the gate-source voltage. In addition, various countermeasures are required for the surge suppression,

involving the layout of the board and the surrounding components to be selected. We hope that you will be able to select the best countermeasures for your design using the methods presented in this application note.

Reference：

*1 Gate-source voltage behaviour in a bridge configuration
Application Note (No. 60AN135ERev.002)
ROHM Co., Ltd. April 2020

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