Application Note

MOSFET Series

Reduction in Switching Loss of Phase-Shift Full-Bridge Converter using PrestoMOS™ R60xxVNx series

Phase-shift full-bridge (PSFB) DC-DC converters are widely used in power supplies for various industrial equipment represented by servers and communication base stations as well as energy storage systems for solar power generation. Furthermore, with the rapid popularization of electric vehicles (EV) in recent years, the applied fields of PSFB have been expanding more and more such as charging stations for the EV.

PSFB converter feature many advantages including the following.

- For the primary side full bridge circuit, the switching loss is reduced with the zero-voltage switching (ZVS) operation.
- The primary side input can be isolated from the secondary side output.
- A relatively high power (a few kW and more) can be handled.

However, the circuit design is more difficult compared with general hard switching DC-DC converters, and the expected performance may not be realized if the circuits are not designed properly in accordance with the switching characteristics of the MOSFET to be used.

This application note describes the basic operation about PSFB converter first. After that it explains the switching characteristics of the primary side MOSFET, and points for optimizing the circuit design. We expect that understanding these will help you to fully deliver the performance of PrestoMOS™ R60xxVNx series, which are ROHM's super junction MOSFET (SJ-MOSFET) for PSFB converter.

1. Application examples of PSFB converter

Figure 1 shows application examples of PSFB converter. PSFB converters are widely used for systems that require "isolation", "high power", and "highly power conversion efficiency", such as power supplies for various industrial equipment represented by servers and communication base stations, energy storage systems for renewable energy represented by solar power generation, and EV charging systems (charging stations). It is used for high power applications from several hundred watts to more than 10 kW as a general power zone. (It is unsuitable for lower power applications than this zone from the perspectives of cost, mounting space, and other factors.) Furthermore, PSFB converters can be used not only for unidirectional operations, but also for bidirectional applications by employing the synchronous rectification system for the secondary side rectifying circuit.

Power supplies

for industrial equipment such as servers

Solar power generation systems

EV charging stations

Figure 1. Application examples of PSFB converter

2. Basics of PSFB converter

2-1. Basic circuit configuration

Figure 2 shows the basic circuit diagram of PSFB converter. The primary side of PSFB converter is generally configured with a full bridge circuit using four power switching devices (such as MOSFETs and IGBTs). In PSFB converter, the ZVS operation is achieved by properly providing phase shifts for the timings of turning ON and OFF these power switching devices.

The leakage inductance of the transformer is generally used as a resonance inductor on the primary side of PSFB converter. However, an external inductor may be added in series to the transformer in order to extend the range of the ZVS operation. In this application note, it is presupposed that the circuit uses such a serially added inductor (L_s). In addition, the leg composed of Q1 and Q2 (the red part in Figure 2) is referred to as "the leading leg" while the leg of Q3 and Q4 (the blue part in Figure 2) is referred to as "the lagging leg". The reasoning behind these names of the respective legs is explained in Section 2-2 below.

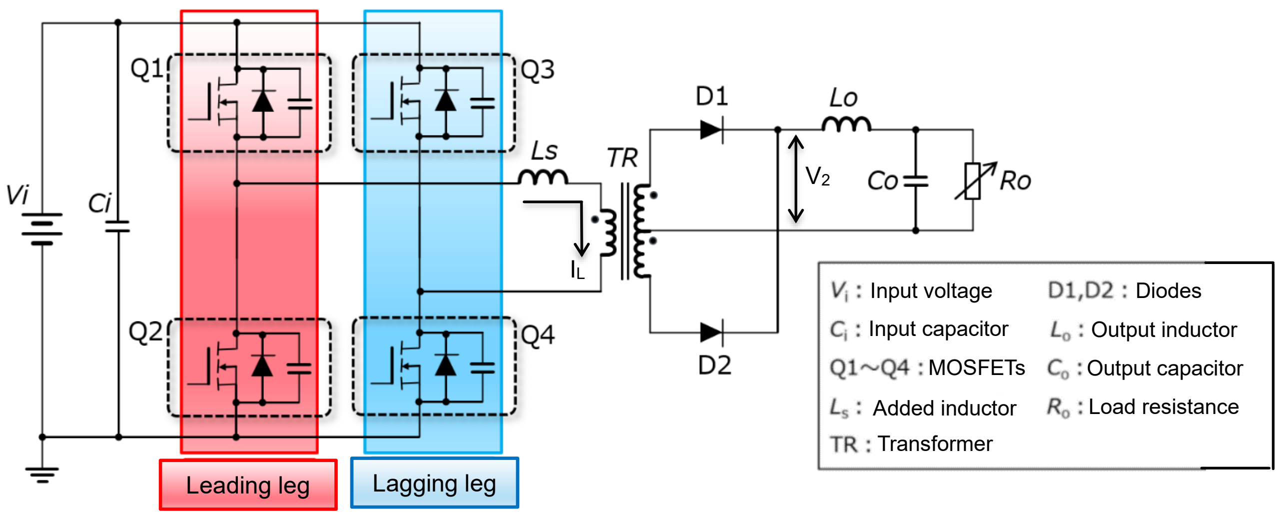


Figure 2. Basic circuit diagram of PSFB converter

2-2. Basic operation waveforms

Figure 3 shows an example of the operation waveforms of PSFB converter. As can be seen in the figure, after the ON/OFF states of Q1 and Q2 are switched, the ON/OFF states of Q3 and Q4 are switched with a certain phase delay. Accordingly, Q1 and Q2 are generally referred to as "the leading leg" while Q3 and Q4 are referred to as "the lagging leg". For details of the operations of Q1 to Q4, refer to the explanations provided in the ROHM application note "Benefits given by PrestoMOS™ series for the Phase-Shift Full-Bridge"[1].

If you look at Figure 3 in detail, you can see that the waveforms of the leading and lagging legs are not identical. In other words, they are not simply the same waveforms with a shifted phase. The difference in the current waveforms after turning ON should be noted. Q1 in the leading leg and Q4 in the lagging leg are used in an example for explanation. For Q1 in the leading leg, there is a certain time margin after turning ON until the direction of inductor current I_L (drain current I_D) is inverted. However, for Q4 in the lagging leg, the current is inverted in a short time after turning ON. Therefore, there is less time margin until the current inversion compared with Q1 in the leading leg. This is one of the factors that make the ZVS operation more likely to be incomplete in the lagging leg (the details are explained in Section 2-3 below).

The switching loss is increased if the ZVS operation at turning ON is incomplete. Therefore, it is very important to accomplish the ZVS operation sufficiently at turning ON in the lagging leg in order to reduce the switching loss of PSFB converter.

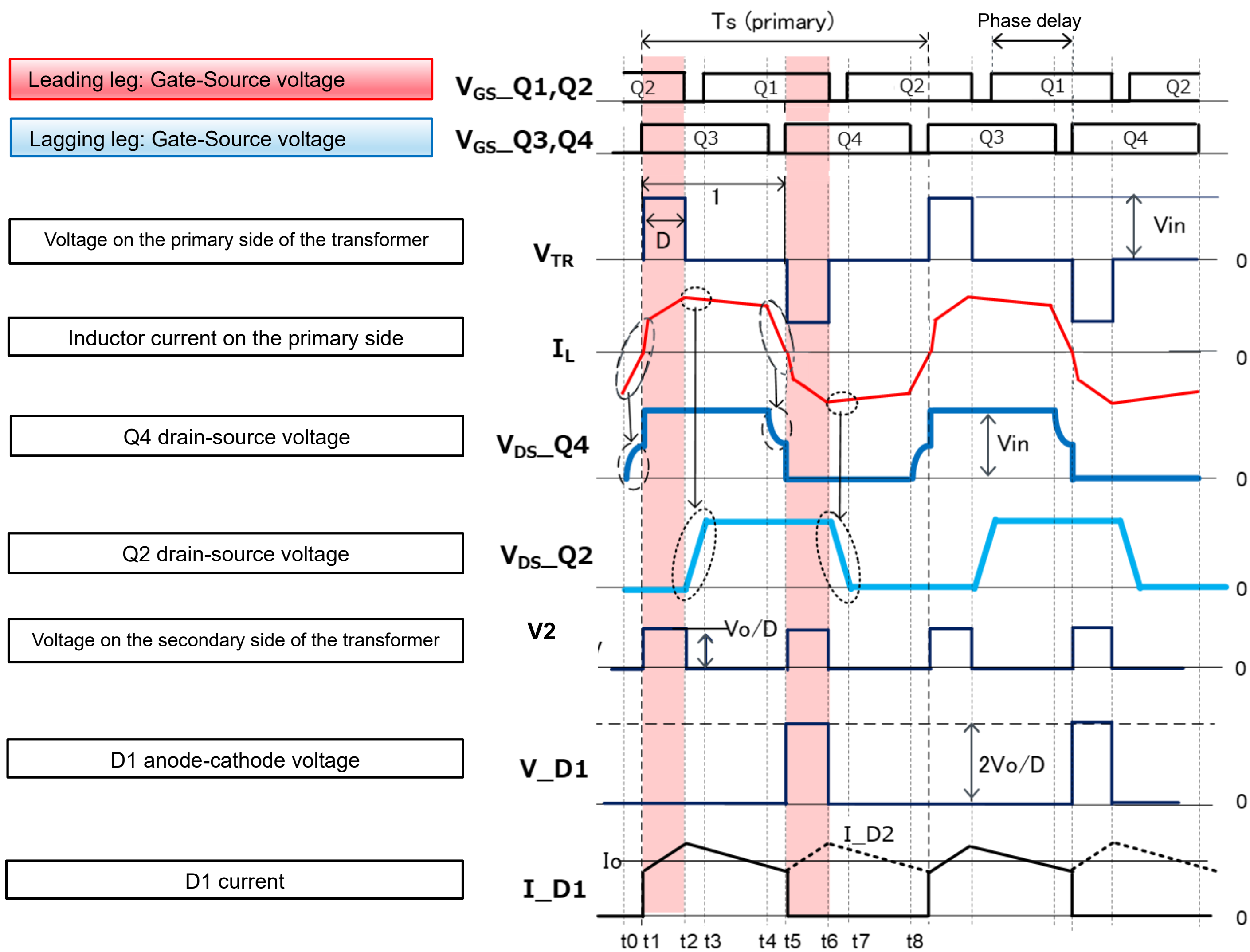


Figure 3. Example of the operation waveforms of PSFB converter

2-3. ZVS operation (turning ON) in PSFB and attentions

Figure 4 shows the steps of the ZVS operation in PSFB converter. The process in which the lower arm starts from the OFF state (*Coss* charged) and reaches the ON state (channel conducted) is used as an example for explanation. As can be seen in Figure 4, turning ON is the ZVS operation in PSFB converter. The operations in steps 1 to 4 are basically the same for the leading and lagging legs. However, as explained in Section 2-2 above, the time after step 4 in Figure 4 until the current direction is inverted (source to drain direction → drain to source direction) is significantly shorter in the lagging leg compared with the leading leg. In other words, in the lagging leg, the turn ON loss is increased if the discharging of MOSFET parasitic capacitance *Coss* is not completed to turn ON the channel within this short period until this current inversion. Therefore, an attention is required. Care must be taken especially under a light load, because the energy of *Ls* to discharge *Coss* $(1/2 \times L_s I^2)$ is lower compared with a heavy load, making the discharging more likely to be incomplete. Furthermore, since the device characteristics such as the turn ON speed depend on the MOSFET to be used, it is very important to make adjustment in accordance with the device characteristics (the details are explained in Chapter 3).

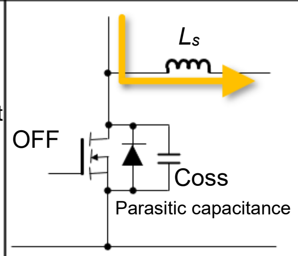
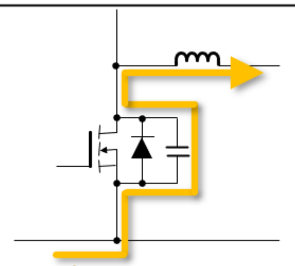
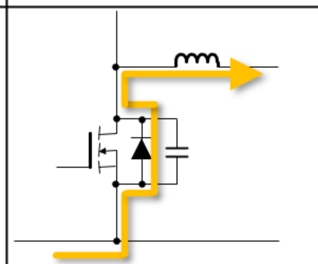
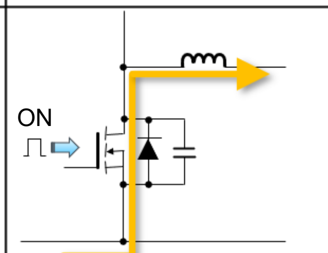
STEP	1	2	3	4
Current path	 L_s OFF Coss Parasitic capacitance	 Coss discharged	 Body diode conducted	 ON Channel conducted (source → drain direction)
Comment	• Upper arm ON (Channel conducted) • Lower arm OFF (*Coss* charged)	• Upper arm is turned OFF. The current continues to flow in the direction of the arrow due to *Ls*. • Simultaneously, the discharge from *Coss* of the lower arm is started (V_{DS} of the lower arm starts falling)	Once the discharge from *Coss* of the lower arm is completed, the conduction of the body diode is started.	After that, the lower arm is turned ON. At this time, the ZVS can be accomplished because V_{DS} is nearly 0 V.

Figure 4. Schematic diagram of the ZVS operation in PSFB converter

2-4. Conditions for accomplishing ZVS and importance of turn ON timing

As explained in Section 2-3, the turn ON operation of PSFB converter uses the energy of *Ls* to discharge *Coss*. Therefore, if this energy of *Ls* exceeds the charging energy of C_{oss} and there is a sufficient time for discharging, drain-source voltage V_{DS} becomes nearly 0V and the ZVS is accomplished. The ZVS is an ideal soft switching operation in PSFB converter, making the turn ON loss nearly zero. In the lagging leg, the condition for accomplishing this ZVS is generally expressed as Equation (1). Here, I_{L1} represents the inductor current when switching Q3 and Q4 ON/OFF in the lagging leg, and E_{oss_Q3} and E_{oss_Q4} represent the energies required for completing the charging and discharging of output capacitances *Coss* of Q3 and Q4, respectively.

$$\frac{1}{2}L_S I_{L1}^2 > E_{OSS\_Q3} + E_{OSS\_Q4} \cdots\cdots\cdots\cdots (1)$$

Equation (1) shows that it is more difficult to accomplish the ZVS when the load is light because I_{L1} is smaller compared with the case when the load is heavy, and that the ZVS can be accomplished more easily when the load is increased.

The condition for accomplishing the ZVS in the leading leg of the MOSFET can be generally expressed as Equation (2), where *n* is the ratio of the numbers of windings of the transformer. I_{L2} represents the inductor current when switching Q1 and Q2 ON/OFF in the leading leg, and E_{oss_Q1} and E_{oss_Q2} represent the energies required for completing the charging and discharging of *Coss* of Q1 and Q2, respectively.
Equation (2) shows that the ZVS operation can be accomplished more easily in the leading leg compared with the lagging leg, because the energy in the load inductance on the secondary side (*Lo*) also contributes to the charging and discharging of *Coss*.

$$\frac{1}{2}(L_S + n^2 L_O) I_{L2}^2 > E_{OSS\_Q1} + E_{OSS\_Q2} \cdots\cdots\cdots\cdots (2)$$

As described above, especially in the lagging leg under a light load, the discharging from *Coss* tends to be incomplete (V_{DS} remains). With this residual voltage of V_{DS}, the switching loss is increased if turning ON is too early. On the other hand, if turning ON is too late, the channel cannot be turned ON before the current inversion as explained in Section 2-3, the turn ON loss is increased in this case as well. Therefore, for PSFB converter, it is very important to adjust the turn ON timing especially in the lagging leg under a light load (the details are explained in Chapter 3 with introduction of an example of actual adjustment).
Naturally, such adjustments can be simplified if it is possible to design *Ls* to be sufficiently large so that the ZVS operation is always accomplished even in the light-load range. However, constraints such as the mounting area make it generally difficult to set a sufficiently large *Ls* in most cases.

3. Device characteristics and adjustment example to turn ON timing

3-1. Gate resistance *Rg_source* and power conversion efficiency

Figure 5-(a) shows the results of the power conversion efficiency evaluation for different conditions of the gate resistance on the turn ON side (*Rg_source*) ((1): 82Ω, (2): 120Ω, (3): 220Ω). Figure 5-(b) shows the turn ON waveforms in the lagging leg under conditions (1) to (3) at output power Pout=1kW. The device used is PrestoMOS™ R6055VNZ4, which is a product in ROHM's latest generation of the high-speed recovery type SJ-MOSFET. Figure 5-(a) shows that the efficiency is significantly varied with the values of *Rg_source* (a maximum of approximately 0.5% change between conditions (1) and (3)).

The turn ON waveforms in Figure 5-(b) show that the discharging of *Coss* is not completed under any conditions, and approximately 150V of voltage remains between the drain and source. As explained in Section 2-4, the ZVS operation generally tends to be incomplete like this in the lagging leg of PSFB converter. The smaller the value of *Rg_source*, the shorter the time until this residual voltage falls to nearly 0 V (t_f), decreasing the turn ON loss accordingly. Therefore, the efficiency is the highest under condition (1). (However, if *Rg_source* is decreased further, the efficiency is decreased due to an increase in the surge.)

As explained in Chapter 2, this residual voltage is observed if the discharging is incomplete or the turn ON timing is too early. In an ideal ZVS operation, the residual voltage of V_{DS} is not observed generally.

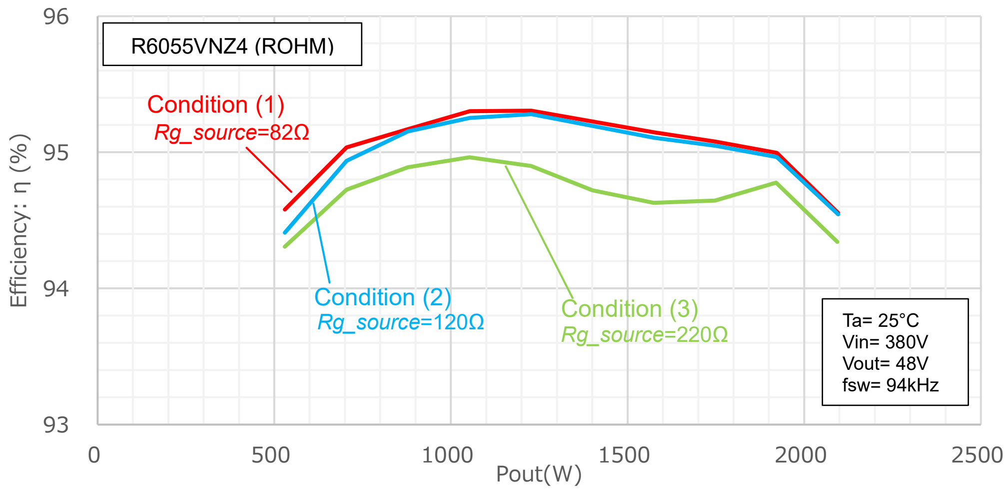
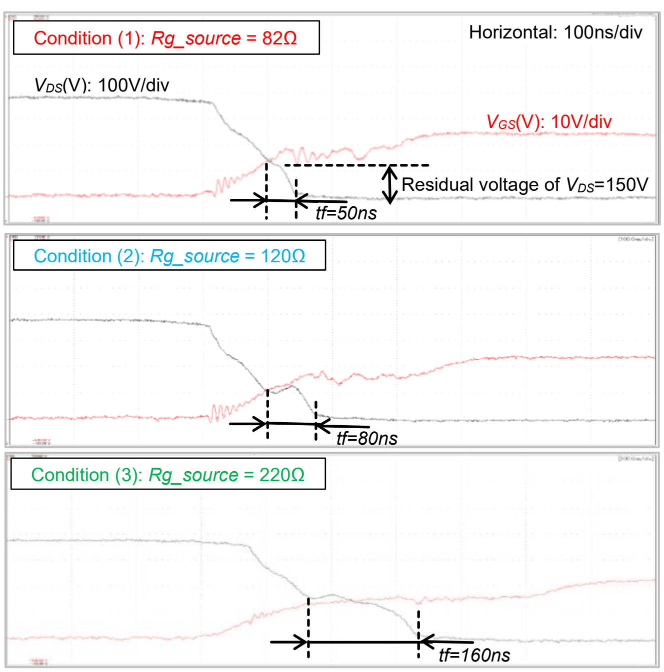


Figure 5-(a). Results of the efficiency evaluation for different values of *Rg_source*



Short *tf* (time until the residual voltage of V_{DS} falls)
→ Smallest turn ON loss

Slightly longer *tf* compared with condition (1)
→ Turn ON loss is also slightly increased compared with condition (1)

Significantly longer *tf* compared with condition (1)
→ Turn ON loss is significantly increased compared with condition (1)

•The same dead time (*DT*) setting for conditions (1) and (2) (200ns*).
•For the evaluation of condition (3), the dead time is decreased to 150ns* to avoid the risk of breaking down due to through current.
* When Pout = 1 kW

Figure 5-(b). Turn ON waveforms under conditions (1) to (3) at Pout=1kW (lagging leg)

3-2. Dead time (*DT*) and power conversion efficiency

Figure 6-(a) shows the results of the power conversion efficiency evaluation for different dead times in the lagging leg (*DT_lag*). The value of *Rg_source* is set as *Rg_source*=82Ω, which provided the highest efficiency in Section 3-1. The device used is ROHM R6055VNZ4, which is the same SJ-MOSFET as Section 3-1. Figure 6-(a) shows that the efficiency is the highest under condition B (*DT_lag*=300ns), and is significantly decreased if the dead time is increased or decreased by only 100ns from this condition. Furthermore, this difference in the efficiencies is more stood out under a lighter load, and the difference is decreased when the load is increased. As explained in Chapter 2, when the load is heavier, the energy of *Ls* to discharge the *Coss* is increased and the operation approaches an ideal ZVS, decreasing the turn ON loss to nearly zero. As a result, the influence of *DT_lag* is decreased.

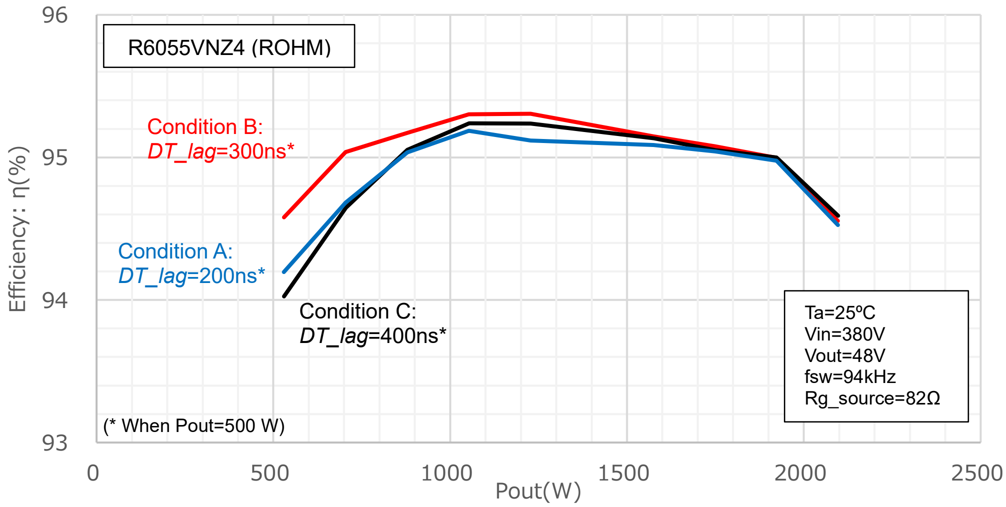


Figure 6-(a). Results of the efficiency evaluation for different dead times (*DT*)

Next, Figure 6-(b) shows the turn ON waveforms in the lagging leg under these conditions at output power Pout=500W. It can be seen that the turn ON loss is the smallest under condition B (*DT_lag*=300ns) because the residual voltage of V_{DS} is the lowest (≈ 220 V). Since *DT_lag* is shorter under condition A compared with condition B, the time for the discharging is shorter and the residual voltage of V_{DS} is higher, increasing the turn ON loss. *DT_lag* is longer under condition C compared with condition B. Therefore, the channel is turned ON too late against the current inversion, causing the discharged *Coss* to be recharged (V_{DS} rises again). The turn ON loss is also larger in this case compared with condition B. Based on these results, it can be understood that adjusting the balance is very important for the dead time setting under a light load.

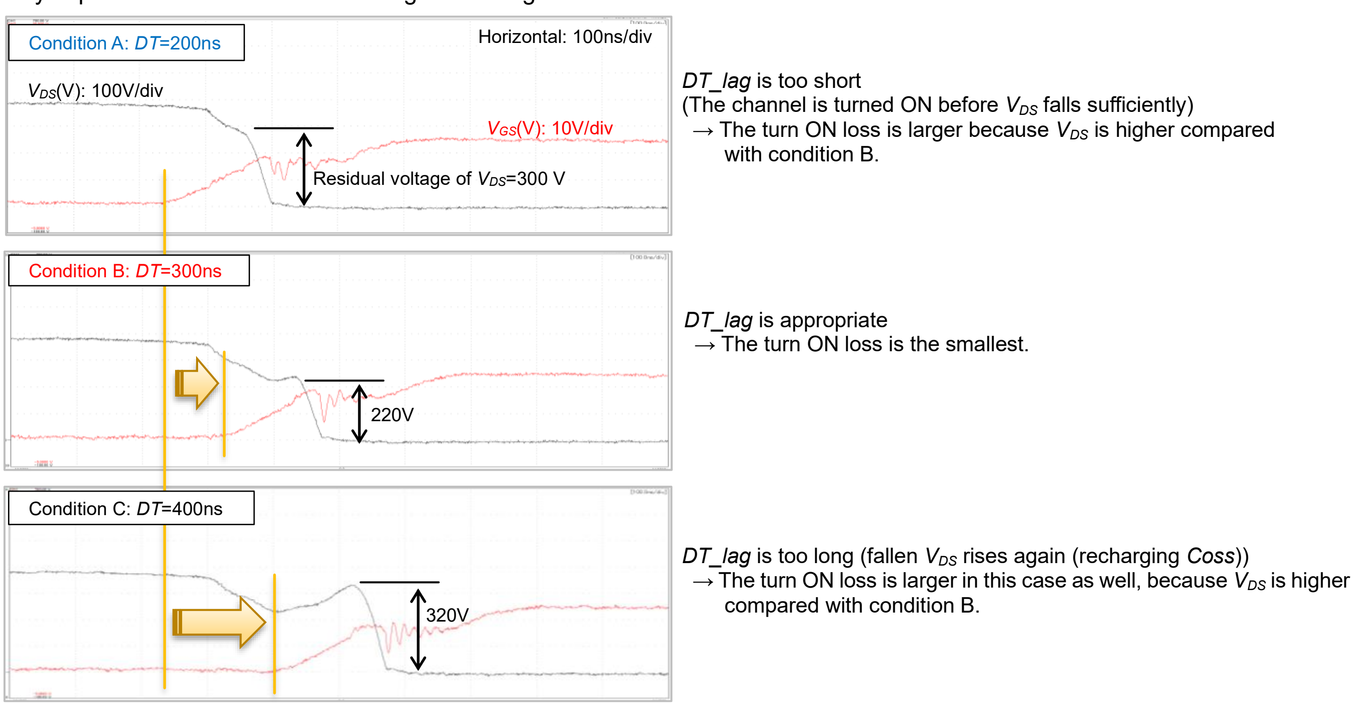


Figure 6-(b). Turn ON waveforms of the lagging leg under conditions A to C (at Pout=500W)

3-3. Dead time setting for the leading leg (*DT_lead*)

Section 3-2 explained the importance of the balanced setting for *Rg_source* and the dead time of the lagging leg (*DT_lag*), which determine the ON timing, in order to reduce the turn ON loss in the lagging leg under a light load. In contrast, as explained in Section 2-2, the ZVS operation is relatively easy in the leading leg because there is a sufficient time before the current inversion and the Coss can be discharged sufficiently (V_{DS} can fall sufficiently) compared with the lagging leg. Furthermore, as explained with Equation (2) in Section 2-4, since the load current on the secondary side also contributes to the discharging in the leading leg, the ZVS operation can be accomplished more easily compared with the lagging leg from this aspect as well.

Figure 7 shows an example of the turn ON waveforms in the leading leg at Pout=500W. As described above, V_{DS} has fallen to nearly 0V when the conduction of the body-diode is started. Therefore, the ZVS is accomplished if turning ON is completed within the section from this point to the current inversion. Figure 7 shows that such a section is significantly longer in the leading leg compared with the lagging leg, resulting in a wider range where *DT_lead* can be adjusted. Therefore, generally set a longer *DT_lead* for the leading leg compared with the lagging leg so that no through current occurs. (*DT_lead*=800ns in Figure 7 is more than two times longer than the setting for the lagging leg.)

As can be seen from the V_{GS} waveform in Figure 7, no plateau region is generally observed in the turn ON waveform of V_{GS} during a complete ZVS operation.

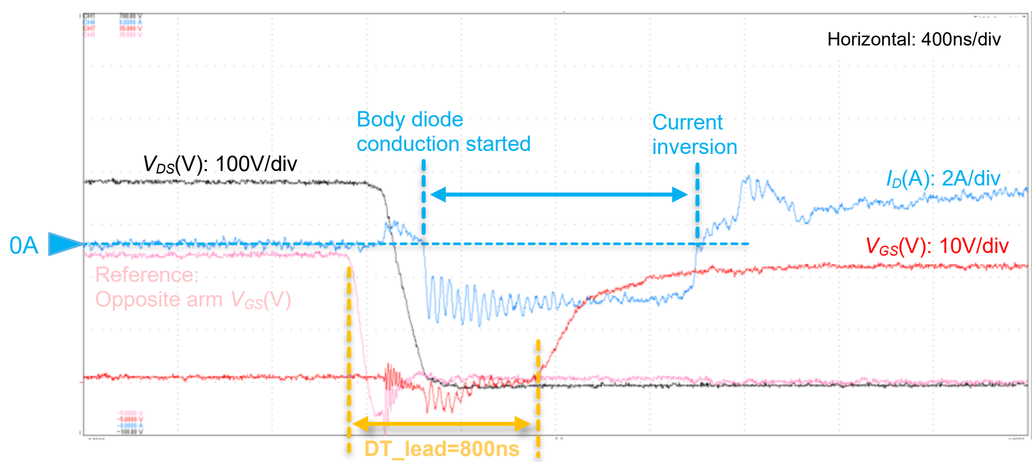


Figure 7. Example of the turn ON waveforms in the leading leg (Pout=500W)

4. Difference in proper conditions according to device characteristics (Comparison with another manufacturer)

Figure 8 shows the results of comparing the power conversion efficiencies between ROHM R6055VNZ4 described above and a product in the same Ron class from another manufacturer (MOSFET-A).

For *Rg_source* and *DT_lag* of R6055VNZ4, the conditions that resulted in the highest efficiency in Chapter 3 are employed. The conditions of *Rg_source* and *DT_lag* of MOSFET-A are adjusted so that the highest efficiency is obtained in the same way as described in Chapter 3 for R6055VNZ4. It can be seen that, although these devices are products in the same Ron class, the difference in the conditions of *Rg_source* is especially significant. This can be attributed to a significant difference in the switching characteristics of these devices. Generally, Qg is the characteristics relevant to the switching. Among them, Qgd have a significant influence on the turn ON loss under conditions in which V_{DS} remains. Therefore, adjustment to the Qgd interval is especially important. Figure 9 shows a comparison of Qg characteristics between R6055VNZ4 and the MOSFET-A. It is shown that Qg characteristics, especially Qgd, of these devices are significantly different. The value of Qgd of MOSFET-A is less than a half of that of R6055VNZ4 (18nC compared to 43nC). Therefore, it is necessary to increase the *Rg_source* value of MOSFET-A more than two times compared with the R6055VNZ4's one in order to optimize the turn ON timing which is the most important in the lagging leg of PSFB converter. As a reference, the Qg characteristics of MOSFET-B is provided, which is a product in the same Ron class from another manufacturer. In contrast to MOSFET-A, its Qg value is larger than that of R6055VNZ4. Therefore, the adjustment to the turn ON timing is important because the switching characteristics are generally different even among products that belong to the same Ron class.

Returning to the comparison of the power conversion efficiencies, Figure 8 shows that the efficiency of R6055VNZ4 is increased when the load is decreased (approximately 0.4% higher at Pout=500W). This result of R6055VNZ4 is a significant advantage in applications that require a stable and highly efficiency over a wide load range, such as those in compliance with the 80PLUS computer power supply standards.

In summary, ROHM R6055VNZ4 shows one of the industry's best switching characteristics and low Ron characteristics simultaneously. Therefore, a highly power conversion efficiency can be expected in PSFB converter. However, as explained in Chapter 3, it is very important to optimize the turn ON timing in order to fully deliver the excellent device performance of R6055VNZ4 in PSFB converter.

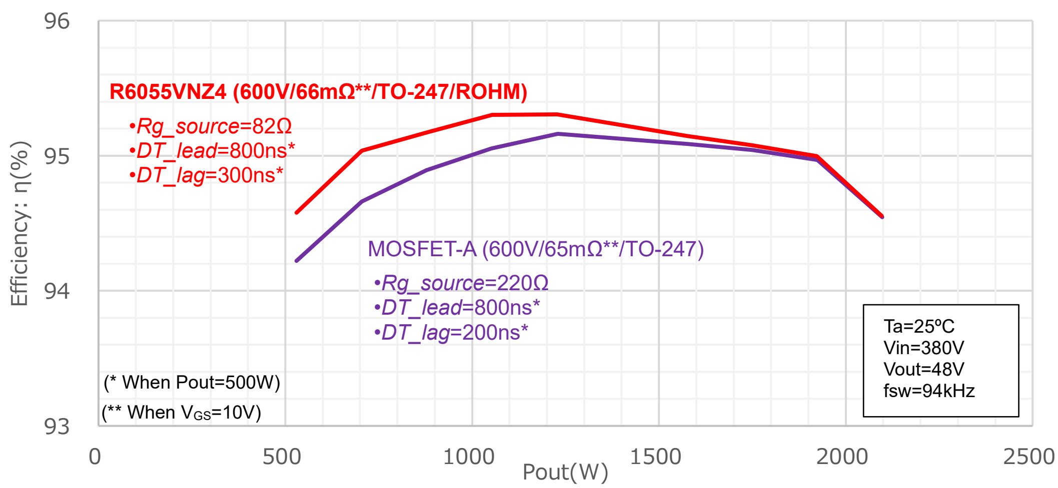


Figure 8. Result of comparison of efficiencies

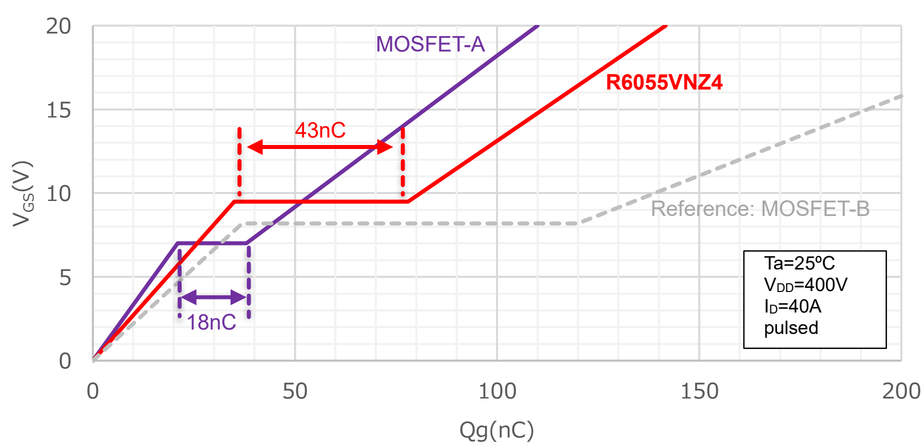
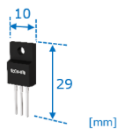
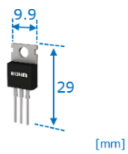
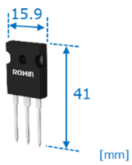


Figure 9. Comparison of Qg characteristics

5. R60xxVNx series lineup

Figure 10 shows the lineup of the PrestoMOS™ R60xxVNz series in ROHM's latest generation of high-speed recovery type SJ-MOSFET. In addition to R6055VNZ4 used for this evaluation, a broad Ron lineup is available for PSFB converter in various load regions. Furthermore, this series features one of the industry's best performances for the high-speed recovery. Therefore, it is ideal for topologies that require a high-speed recovery performance, including Totem-Pole PFC, various types of inverters, and motor drivers as well as PSFB converter. Specifications other than the following will be added gradually. Please feel free to contact us.

Package	Part No.	V_{DS} (V)	I_D (A)	Ron Typ. (mΩ) V_{GS}=15V	Ron Typ. (mΩ) V_{GS}=10V	Qg Typ. (nC) V_{GS}=10V	Trr Typ. (ns)
TO-220FM 	R6018VNX	600	10	170	188	27	68
	R6024VNX	600	13	127	138	38	80
	R6035VNX	600	17	95	99	50	92
TO-220AB 	R6024VNX3	600	24	127	138	38	80
	R6035VNX3	600	35	95	99	50	92
TO-247 	R6055VNZ4	600	55	59	66	80	112
	R6077VNZ4	600	77	42	46	108	125

• For details of the specifications, check with the data sheet, etc.
• Note that the specifications are subject to change without notice.

Figure 10. Lineup of PrestoMOS™ R60xxVNx series

6. Summary

• In the PSFB converter, the ZVS operation is more difficult in the lagging leg under a lighter load. Therefore, reducing the turn ON loss under such circumstances improves the power conversion efficiency.

• To reduce the turn ON loss described above, it is important to adjust *Rg* and the dead time (*DT*) so that the turn ON timing is optimized. In addition, it is also important to make adjustment for each device, because the switching characteristics generally different from each MOSFET to be used.

• PrestoMOS™ R60xxVNx series in ROHM's latest generation have industry-leading switching performance as high-speed recovery type SJ-MOSFET and low Ron characteristics simultaneously. Therefore, a highly power conversion efficiency can be expected in the PSFB circuits.

7. References

[1] Benefits given by PrestoMOS™ series for the Phase-Shift Full-Bridge
Application Note (No.61AN028J, Rev.002) ROHM Co., Ltd.,

Notes

1) The information contained herein is subject to change without notice.

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