Super Junction MOSFET series

Benefits given by PrestoMOS™ series for the Phase-Shift Full-Bridge

Power supplies that can handle high power, such as servers and on-board chargers, generally employ a full bridge circuit. In particular, Phase-Shift Full-Bridge (hereafter PSFB) circuit can perform a zero-voltage switching (hereafter ZVS) operation when switching devices, such as Super-Junction MOSFETs (SJ-MOSFETs) or IGBTs, are turned ON. Therefore, the switching loss can be further reduced compared with general hard switching converters, making the PSFB circuit suitable for handling higher power.

This application note describes the basic operation of the SJ-MOSFET in the PSFB circuit, and explains the importance of the recovery characteristics of the MOSFET's body diodes. This application note also presents the results of a comparison of the power conversion efficiencies in an actual PSFB circuit between PrestoMOS™, which is a high-speed recovery type SJ-MOSFET included in ROHM's lineup, and products from other manufacturers, showing that this series is very useful in the PSFB circuit.

1. Basic configuration of PSFB circuit

Figure 1 shows the basic configuration of the PSFB circuit. To establish ZVS operation, the leakage inductance of the transformer is used as a resonance inductor. However, an inductor may be added in series to the transformer in order to extend the range of ZVS operation. In this application note, it is presupposed that the circuit uses such a serially added inductor (L_s).

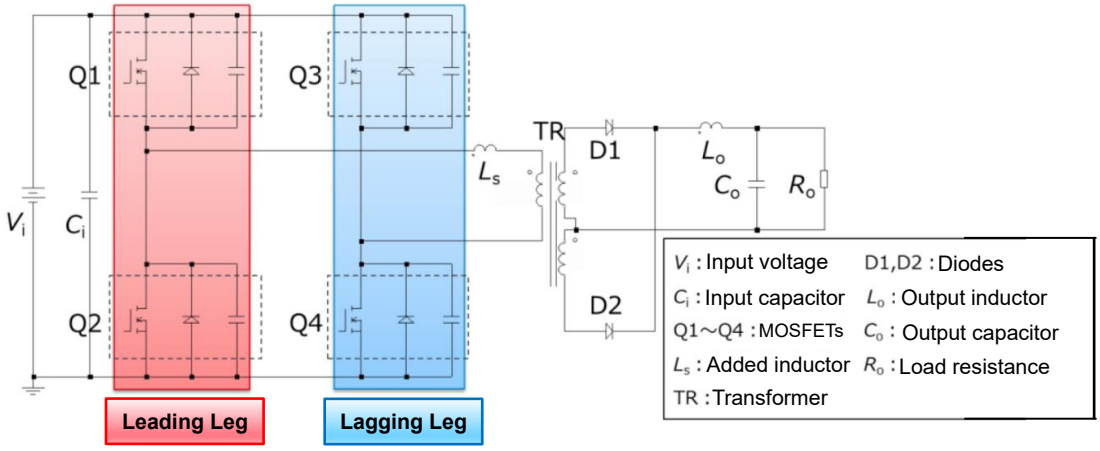

Figure 1. Basic circuit diagram of the PSFB circuit

Figure 2 shows the timing chart of switching devices Q1 to Q4 in the PSFB circuit. The numbers under the chart represent the operation modes in the PSFB circuit.

As can be seen in the chart, after the ON/OFF states of Q1 and Q2 are switched, the ON/OFF states of Q3 and Q4 are switched with a certain phase delay. Accordingly, the leg of Q1 and Q2 is generally referred to as the leading leg, while the leg of Q3 and Q4 is referred to as the lagging leg.

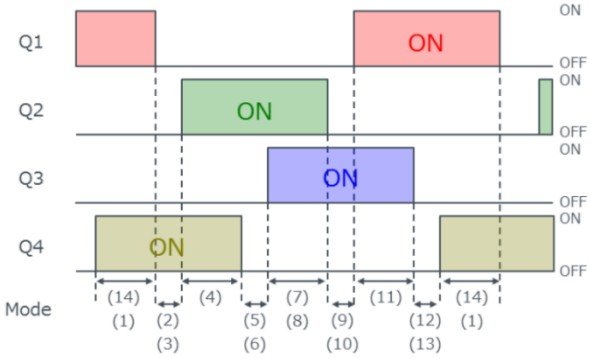

Figure 2. Timing chart of Q1 to Q4

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2. Basic operation of PSFB circuit

ZVS operations in the PSFB circuit consists of discharging the stored electric charges from output capacitance *C*oss of the MOSFET as the switching device, conducting the body diode and decreasing drain-source voltage V_{DS} to nearly zero, and then turning ON the MOSFET.

Figure 3 shows the waveforms of the drain currents of Q1 to Q4 and the current flowing through the primary side of the transformer in the PSFB circuit. When the direction of the current flowing from the drain to the source is regarded as positive, it can be confirmed that each of Q1 to Q4 has a period during which the drain current flows in the negative direction, i.e., a period during which a forward current flows through the body diode. For example, the section of Mode (7) represents such a period for Q3. During this period, ZVS operation can be achieved by turning ON the MOSFET because V_{DS} is nearly zero.

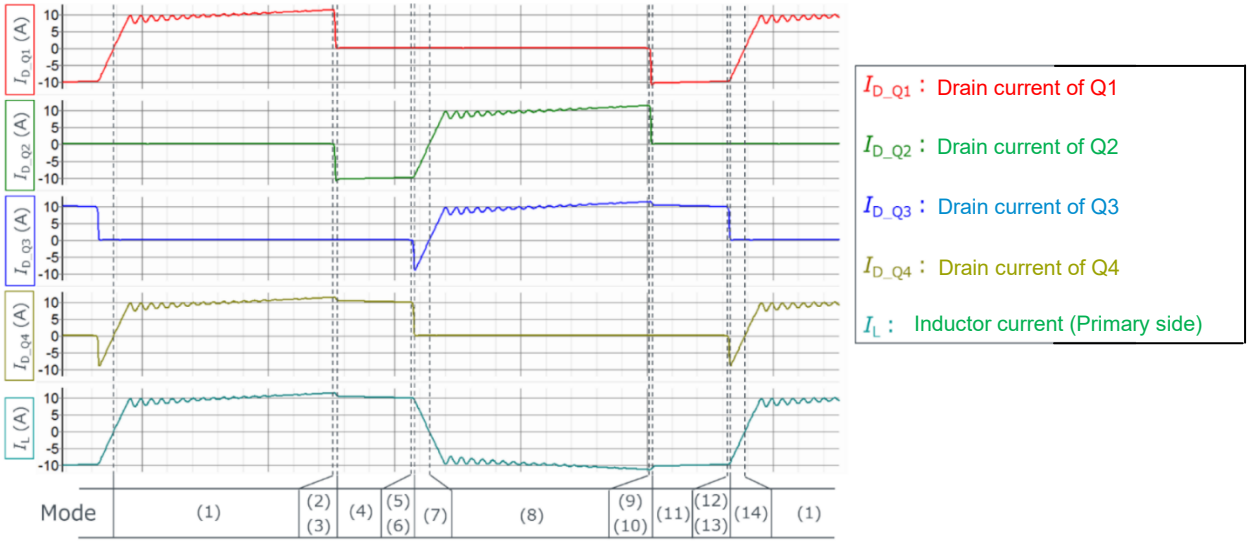
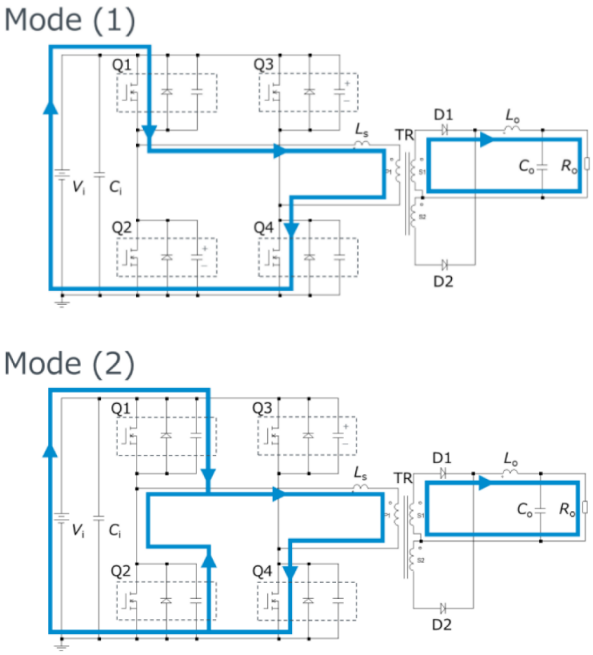


Figure 3. Waveforms of the drain currents of Q1 to Q4 and the current flowing through the primary side of transformer

In Figure 3, it can be seen that the leading and lagging legs have different current waveforms, not just their phases are shifted. The difference in the waveforms between the two legs can be explained by considering the current path for each Modes (1) to (14) shown in Figures 2 and 3. Figures 4 to 7 below show the current path for each mode and explain how the current waveforms as shown in Figure 3 are caused.

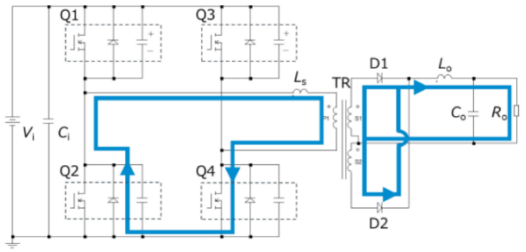


Mode (1)
- Q1 and Q4 are ON state, while Q2 and Q3 are OFF state.
- Since Q2 and Q3 are OFF state, the output capacitances of Q2 and Q3 (C_{oss_Q2} and C_{oss_Q3}) are charged.
- Input voltage V_i is applied to the primary side of the transformer.
- As a current flows through L_s, this energy is stored in L_s.

Mode (2)
- Only Q1 is turned OFF.
- Since Q1 is turned OFF, output capacitance C_{oss_Q1} is charged. This decreases the electric potential on the drain side of Q2, causing C_{oss_Q2} to start discharging simultaneously.

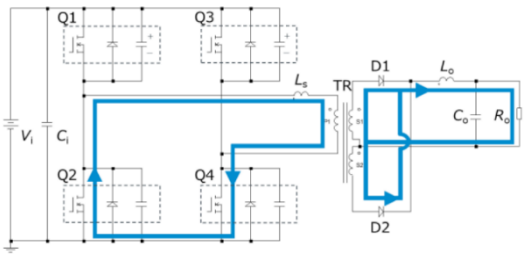
Figure 4. Current paths for Modes (1) to (2)

Mode (3)



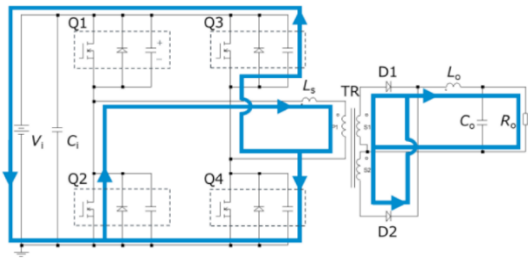
Mode (3)
- If the energy remains in L_s after charging of C_{oss_Q1} and discharging of C_{oss_Q2} are completed, current flows through the body diode of Q2 (D_{Q2}) and the freewheeling operation is started.
- While the freewheeling operation, the electromagnetic energy isn't delivered to the secondary side. However, the current keeps flowing due to the work of L_o. Since the current direction due to L_o is forward for D1 and D2, the current flows through both diodes.

Mode (4)



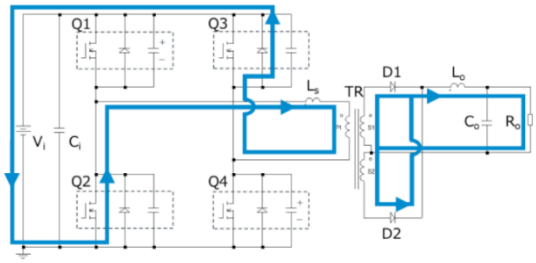
Mode (4)
- Q2 is turned ON. Since D_{Q2} is conducting at this time, the drain-source voltage of Q2 (V_{DS_Q2}) is nearly 0V. Therefore, ZVS operation is achieved, and the turn-ON loss is nearly zero.

Mode (5)



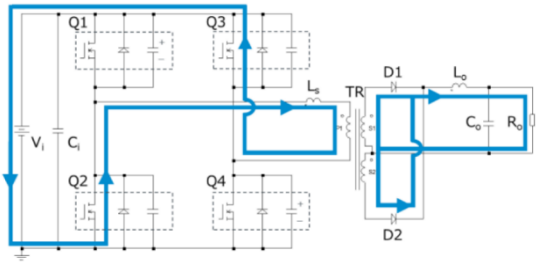
Mode (5)
- Q4 is turned OFF.
- Since Q4 is turned OFF, the output capacitance of Q4 (C_{oss_Q4}) is charged. The source side electric potential of Q3 is increased simultaneously, and discharging output capacitance C_{oss_Q3}.

Mode (6)



Mode (6)
- If energy remains in L_s after charging of C_{oss_Q4} and discharging of C_{oss_Q3} are completed, the current flows through the body diode of Q3 (D_{Q3}) and the freewheeling operation is started.

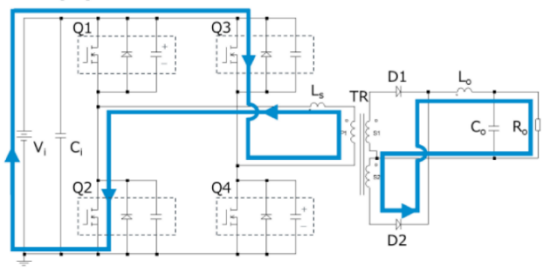
Mode (7)



Mode (7)
- Q3 is turned ON. Since D_{Q3} is conducting at this time, the drain-source voltage of Q3 (V_{DS_Q3}) is nearly 0V. Therefore, ZVS operation is achieved, and the turn-ON loss is nearly 0.
- When Q3 is turned ON, L_s rapidly releases energy. Since the voltage direction is reversed from I_L in Modes (1) to (6), the current direction is rapidly inverted.

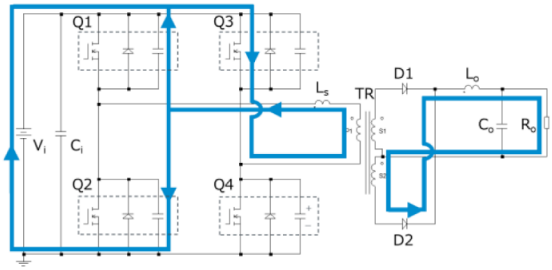
Figure 5. Current paths for Modes (3) to (7)

Mode (8)



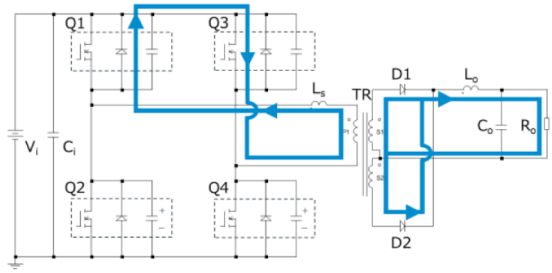
Mode (8)
- Q2 and Q3 are ON state, while Q1 and Q4 are OFF state.
- Therefore, C_{oss_Q1} and C_{oss_Q4} are charged.
- V_i is applied to the primary side of the transformer in the opposite direction from Mode (1).
- As the current flows through L_s, energy is stored in L_s.

Mode (9)



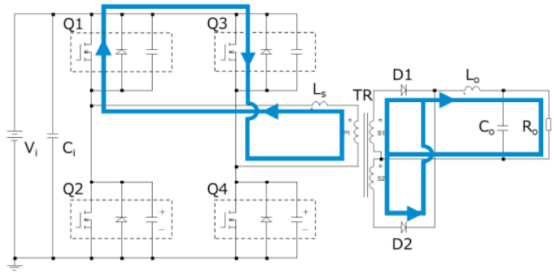
Mode (9)
- Q2 is turned OFF.
- Since Q2 is turned OF, C_{oss_Q2} is charged. Simultaneously, C_{oss_Q1} is discharged.

Mode (10)



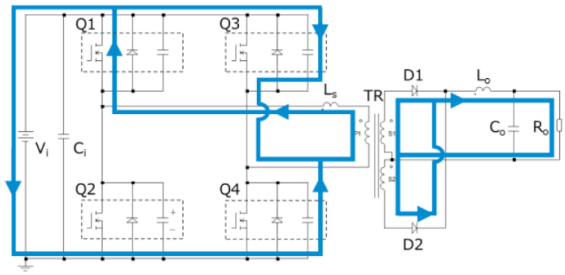
Mode (10)
- If energy remains in L_s after charging of C_{oss_Q2} and discharging of C_{oss_Q1} are completed, the current flows through the body diode of Q1 (D_{Q1}) and the freewheeling operation is started.
- While the freewheeling operation, the electromagnetic energy isn't delivered to the secondary side. However, the current keeps flowing due to the work of L_o. Since the current direction due to L_o is forward for D1 and D2, the current flows through both diodes.

Mode (11)



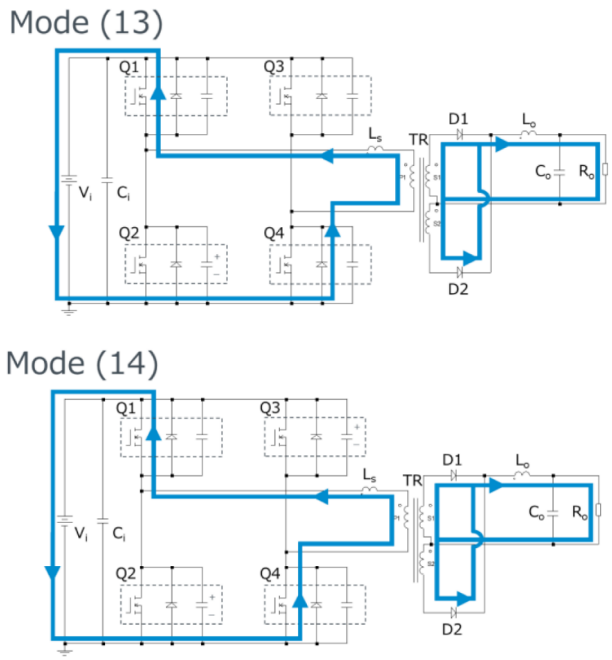
Mode (11)
- Q1 is turned ON. Since D_{Q1} is conducting at this time, the drain-source voltage of Q1 (V_{DS_Q1}) is nearly 0V. Therefore, ZVS operation is achieved, and turn-ON loss is nearly zero.

Mode (12)



Mode (12)
- Q3 is turned OFF.
- Since Q3 is turned OFF, C_{oss_Q3} is charged. Simultaneously, C_{oss_Q4} is discharged.

Figure 6. Current paths for Modes (8) to (12)



Mode (13)
• If energy remains in L_S after charging of C_{oss_Q3} and discharging of C_{oss_Q4} are completed, the current flows through the body diode of Q4 (D_{Q4}) and the freewheeling operation is started.

Mode (14)
• Q4 is turned ON. Since D_{Q4} is conducting at this time, the drain-source voltage of Q4 (V_{DS_Q4}) is nearly 0V. Therefore, ZVS operation is achieved, and turn-ON loss is nearly zero.
• L_S rapidly releases energy. Since the voltage is applied so that the current flows in the opposite direction from I_L in Modes (8) to (13), the current direction is rapidly inverted.

Figure 7. Current paths for Modes (13) to (14)

As explained specifically for Modes (7) and (14), turning ON the MOSFET in the lagging leg connects the input power supply and L_S in series, rapidly reducing the energy in L_S. Since this action does not occur in the leading leg, the difference in the current waveforms occurs between the leading and lagging legs as a result (the channel conduction time is generally longer for the lagging leg). As can be seen from this fact, a difference in the power losses occurs between the MOSFET of the leading and lagging legs. Therefore, care must be taken regarding this point in the thermal design.

3. Cautions for PSFB circuit under light load

3-1. Conditions for establishing ZVS and importance of dead time

As explained in Chapter 2 for operation modes (5) and (6) as well as (12) and (13), the charging and discharging of the MOSFET cannot be completed if the energy stored in L_S is lower than the energy stored in C_{oss} of the MOSFET in the lagging leg. Therefore, ZVS operation cannot be achieved. In other words, taking Mode (5) as an example, a condition for achieving ZVS can be expressed as Equation (1) below. Here, I_{L1} represents I_L when Mode (4) ends. E_{oss_Q3} and E_{oss_Q4} represent the energies required for completing the charging and discharging of the output capacitances of Q3 and Q4, respectively.

$$\frac{1}{2}L_S I_{L1}^2 > E_{OSS\_Q3} + E_{OSS\_Q4} \cdots\cdots\cdots (1)$$

Equation (1) shows that ZVS operation is difficult to be achieved at light load because I_{L1} is small, and can be achieved more easily as the load is increased.

On the other hand, the MOSFET in the leading leg delivers energy to the secondary side via the transformer when C_{oss} is charged and discharged. Consider a condition for establishing ZVS with the energy balance as described above. Taking Mode (2) as an example and assuming that the ratio of the windings numbers of the transformer is n, the condition for establishing ZVS in the leading leg can be expressed as Equation (2) below. Equation (2) shows that ZVS operation can be easily achieved in the leading leg, because the energy in the load inductance on the secondary side also contributes to the charging and discharging.

$$\frac{1}{2}(L_S + n^2 L_O) I_{L2}^2 > E_{OSS\_Q1} + E_{OSS\_Q2} \cdots\cdots\cdots (2)$$

Here, I_{L2} represents I_L when Mode (1) ends. E_{oss_Q1} and E_{oss_Q2} represent the energies required for completing the charging and discharging of C_{oss} of Q1 and Q2, respectively.

For an actual circuit operation, a period of dead time is generally set to prevent short circuiting between the upper and lower arms. As described above, the charging and discharging of the MOSFET may not be completed, i.e., V_{DS} may remain, particularly in the lagging leg under a light load. Therefore, the turn ON loss in the lagging leg could be increased depending on the dead time setting. Consequently, the dead time setting under a light load is especially important for the lagging leg in the PSFB circuit.

Figure 8 shows the schematic diagram of the turn ON waveforms with appropriate and inappropriate dead times.

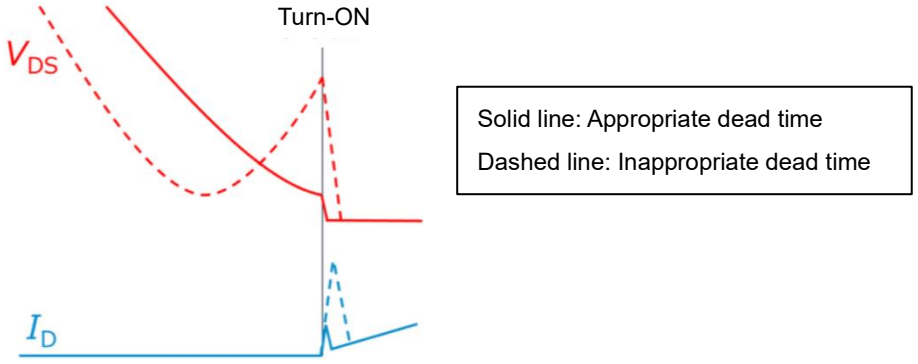


Figure 8. Schematic diagram of MOSFET's turning ON in the lagging leg under a light load

Furthermore, if the dead time is inappropriate, a large drain current (I_d) may be observed instantaneously. There are two possible reasons for this as follows.

(1): Gate-source voltage V_{GS} follows the change in V_{DS} and temporarily exceeds threshold voltage V_{th} (erroneous turn-ON), resulting in an observation of through current.

(2): The charging current to C_{oss} of the MOSFET on the other arm is observed.

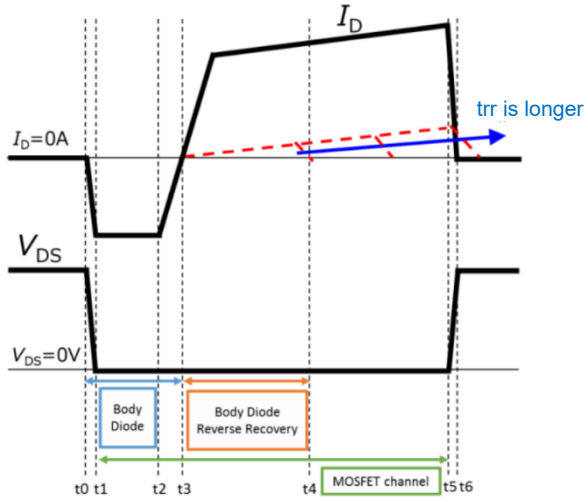
The charging current to C_{oss} in the latter generally occurs during the hard switching operation. The through current due to the erroneous turn ON in the former can be prevented by appropriately setting the ratio of the gate-drain capacitance (C_{gd}) and the gate-source capacitance (C_{gs}) of the MOSFET.

The ratio of C_{gd} and C_{gs} is appropriately designed for PrestoMOS™. Therefore, a reduction in the switching loss can be expected by preventing the through current.

3-2. Cautions for parasitic bipolar transistor

Generally, the recovery time of the body diode (t_{rr}) of the MOSFET becomes longer in the PSFB circuit under a light load. This is because V_{DS} applied to the body diode is nearly 0V during the recovery period in the PSFB circuit, delaying the release of electric charges. In the PSFB circuit. If this recovery current remains when the MOSFET is turned OFF, the parasitic bipolar transistor may be erroneously turned ON, causing the MOSFET to be destroyed [1].

Figure 9 shows the relationship of recovery time t_{rr}, the conduction time of I_D, and the erroneous turn ON of the parasitic bipolar transistor in the leading leg. As V_{DS} is decreased under a lighter load, t_{rr} is extended as shown with the dashed line in red. If t_{rr} becomes longer than the conduction time of I_D, the remaining recovery charges may erroneously turn ON the parasitic bipolar transistor and destroy the MOSFET.



t0 to t1: Output capacitance of the MOSFET is discharged and the forward current starts flowing through the body diode.

t1 to t2: Body diode is conducting during this period.

t2 to t5: MOSFET is ON state.

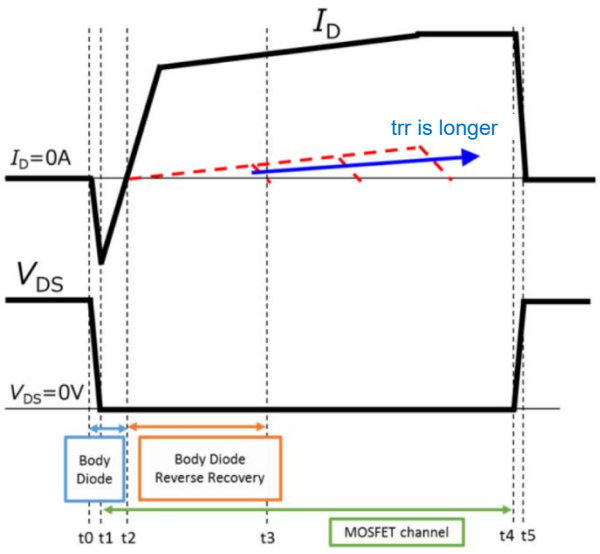
t2 to t4: Recovery current of the body diode flows during this period. This period is extended as V_{DS} is decreased.

t5 to t6: MOSFET is turned OFF. If the recovery current still remains at this time, the parasitic bipolar transistor may be erroneously turned ON and the MOSFET may be destroyed.

Figure 9. Relationship of recovery time t_{rr}, conduction time of I_D, and erroneous turn ON of parasitic bipolar transistor in leading leg

Based on the above considerations, it is preferable to select MOSFET with a short t_{rr} for the PSFB circuit. PrestoMOS™ series show one of the industry's best performances for the high-speed recovery. Therefore, these issues are unlikely to occur with PrestoMOS™ series.

Also for the lagging leg, the parasitic bipolar transistor may be erroneously turned ON during the turn OFF. However, as explained in Chapter 2, the effect of the increase in t_{rr} is smaller, because the conduction time of I_D is longer in the lagging leg compared with the leading leg (Figure 10). In other words, the risk of MOSFET breaking down by erroneously turning ON the parasitic bipolar transistor is lower in the lagging leg compared with the leading leg.



t0 to t1: Output capacitance of the MOSFET is discharged and the forward current starts flowing through the body diode.

t0 to t1: Body diode is conducting during this period.

t1 to t4: MOSFET is ON state.

t1 to t3: Recovery current of the body diode flows during this period. This period is extended as V_{DS} is decreased.

t4 to t5: MOSFET is turned OFF.
Since the conduction time of I_D is longer compared with the leading leg, the recovery current is less likely to remain during the turn OFF (the parasitic bipolar transistor is less likely to be turned ON erroneously).

Figure 10. Relationship of recovery time t_{rr}, conduction time of I_D, and erroneous turn ON of parasitic bipolar transistor in lagging leg

5. Results of efficiency evaluation

Based on the explanations above, it can be understood that PrestoMOS™ with a short t_{rr} is useful in PSFB circuit. Next, Figure 11 shows the results of an evaluation of the power conversion efficiency using an actual power supply circuit. A power conversion efficiency is one of the most important indicators of for power supplies. As the MOSFET of Q1 to Q4, PrestoMOS™ with an on-resistance of approximately 200mΩ is compared with products of the same class from other manufacturers.

As can be seen in Figure 11, R6018VNX in the latest generation of the PrestoMOS™ products resulted in the highest efficiency across the entire load range. This shows that the R60xxVNX series products have industry-leading switching performance as high-speed recovery type SJ-MOSFET, and are ideal for PSFB circuit.

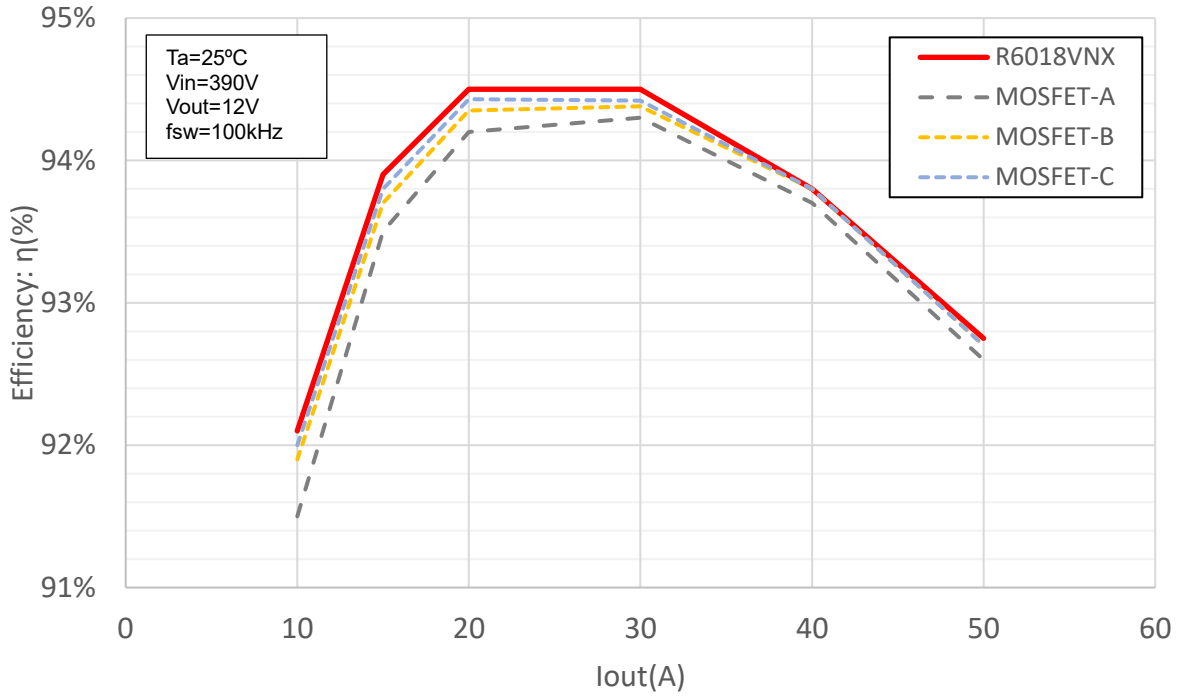


Figure 11. An example of power conversion efficiency vs. output current characteristics of PSFB circuit

6. Summary

- Under a light load, ZVS operation is difficult to achieve for the MOSFET in the lagging leg. Therefore, the turn-ON loss is more likely to be increased. To reduce this turn-ON loss, it is generally important to set the dead time appropriately.
- In the leading leg under a light load, if t_{rr} of the body diode of the MOSFET is too long, the parasitic bipolar transistor of the MOSFET may be erroneously turned ON. Therefore, for the PSFB circuit, it is important to select a MOSFET for which the body diode has a short t_{rr} characteristics.
- PrestoMOS™ R60xxVNx series in ROHM's latest generation have industry-leading switching performance as high-speed recovery type SJ-MOSFET, and therefore are ideal for the PSFB circuit.

7. Reference

[1] L. Saro, et al., "High-Voltage MOSFET Behavior in Soft-Switching Converter: Analysis and Reliability Improvements," International Tel-communication Conference, San Francisco, 1998.

Notes

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