Operational Amplifier Series

Oscillation of Op-Amp Caused by Capacitive Load

Contents:

1. Frequency characteristics of op-amp

Term descriptions

• Gain frequency characteristic:

The gain of an amplifier circuit has a frequency characteristic.

This characteristic is determined by the phase compensation capacitance and terminal capacitance of the inside of the op-amp, the parasitic capacitance of the circuit board, and the circuit constant.

• Phase frequency characteristic:

This characteristic represents the difference in phase between the input and output waveforms of the op-amp. Similarly to the gain, it is affected by the characteristics, the circuit constant, and the parasitic capacitance of the op-amp.

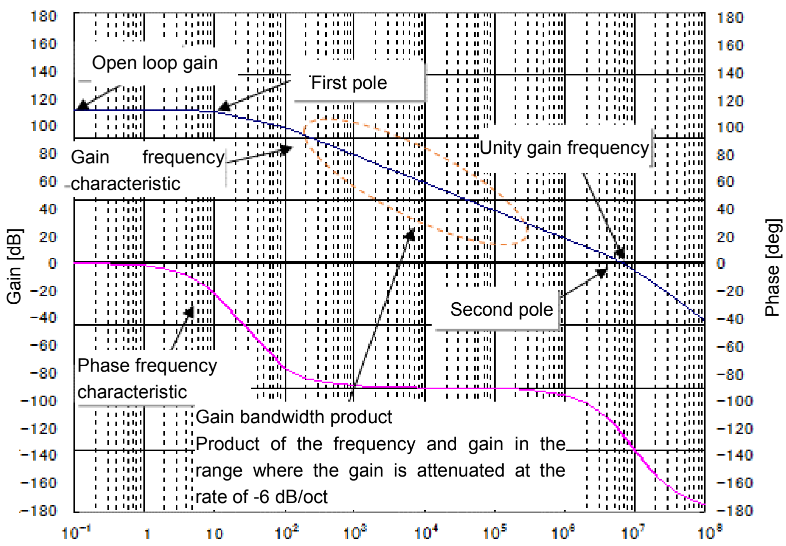


Figure 1. Example of open loop frequency characteristics of op-amp

• Open loop gain (Av):

The open loop gain represents the voltage gain for direct current.

• Unity gain frequency (f_T):

The frequency at which the gain is 0 dB (1times) is referred to as the unity gain frequency.

• Gain bandwidth product (GBW):

The frequency characteristic of an amplifier circuit shows an attenuation at the rate of -6 dB/oct per pole. The product of the gain and frequency at an arbitrary point in the range where the -6 dB/oct attenuation occurs is referred to as the gain bandwidth product. This product represents the frequency bandwidth within which the op-amp can be used for small signals.

Gain bandwidth product [Hz] = Frequency [Hz] × Gain [times]

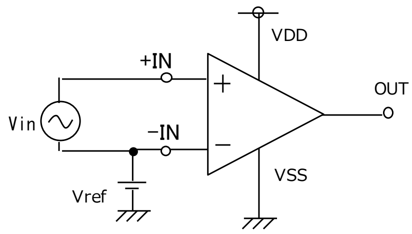


Figure 2. Measurement circuit (schematic diagram)

• First pole:

This is the first of several poles. The amplitude is attenuated at the rate of -6 dB/oct per single pole. Phase delay begins to increase when the frequency reaches 1/10 of the first pole frequency. The delay increases by 45deg at the first pole frequency and by 90deg when the frequency reaches 10 times that of the first pole frequency.

• Second pole:

This is the second of several poles. The attenuation rate increases to -12 dB/oct. In addition to the phase delay from the first pole, the phase delay further increases by 45deg at the second pole frequency and by 90deg when the frequency reaches 10 times that of the second pole frequency.

Note: -6 dB/oct = attenuation by -6 dB when the frequency is doubled. (oct = octave)

• Phase margin:

The difference in phase between the input and output signals at the frequency where the gain is 0 dB (1times) is referred to as the phase margin. The phase margin is an indicator of the margin level and is designed to have a value between 40deg and 60deg.

In an inverting amplifier circuit, the difference in phase between the input and output θ1 is the gain margin. The phase of an inverting amplifier circuit begins at 180deg.

Since the phase of a non-inverting amplifier circuit begins at 0deg, the gain margin is the margin level from 180deg, namely 180deg + θ2.

Phase margin of inverting amplifier circuit: θ1

Phase margin of non-inverting amplifier circuit: 180deg + θ2

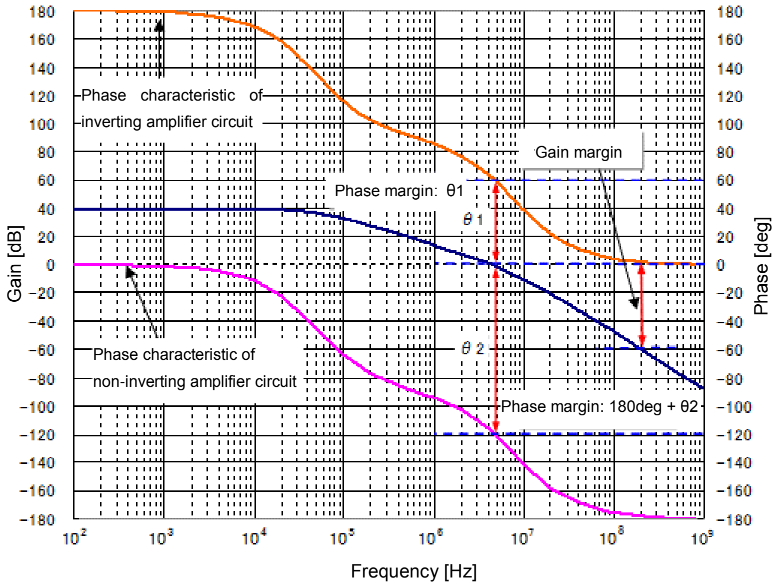


Figure 3. Example of frequency characteristics of inverting (non-inverting) amplifier circuit 40 dB* (100 times)

• Gain margin:

The gain margin is the margin level for the gain to 0 dB at the frequency where the phase delay reaches 180deg. Typically, the gain margin is designed to be 7 dB or larger. The gain margin is used as an indicator of the margin level similarly to the phase margin.

* The open loop gain of an op-amp is very large near a direct current (100 dB or larger). Applying a DC feedback from the output with a resistor stabilizes the output DC voltage.
When measuring the gain frequency characteristics, the gain of the inverting or non-inverting amplifier circuit is set to about 40 dB in order to perform the measurement stably. Since the characteristics at frequencies higher than the first pole frequency range are equivalent, the phase and gain margins can be read from this graph.

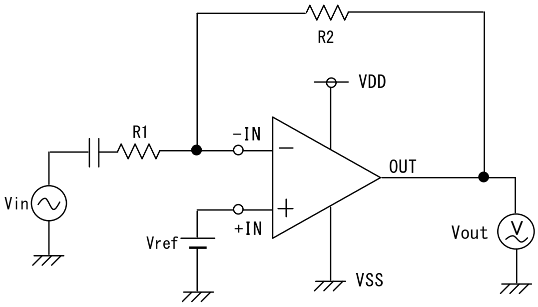


Figure 4. Inverting amplifier circuit

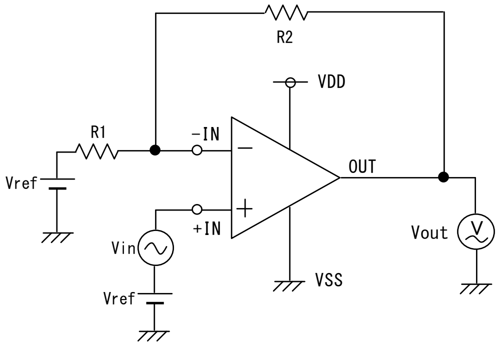
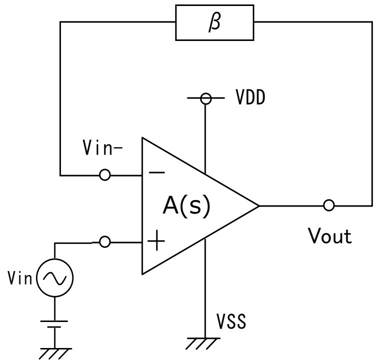


Figure 5. Non-inverting amplifier circuit

2. Phase delay and oscillation

This section describes one of the most general concepts for oscillations caused by Phase delay, the Barkhausen stability criterion.
The transfer function of a negative feedback circuit is determined in Figure 6.

$$A(s)(V_{in} - V_{in-}) = V_{out}$$
$$V_{in-} = \beta V_{out}$$



A(s): transfer function of op-amp
s = jω, ω = 2πf,
f: frequency, β: loop gain
Figure 6. Negative feedback circuit

From the two equations above, the transfer function is determined as follows.

$$\frac{V_{out}}{V_{in}} = \frac{A(s)}{1+\beta A(s)}$$

Point
- When the phase is delayed by 180deg, the condition becomes identical to the state when a positive feedback is applied, causing an oscillation.

We focus on the denominator of the transfer function, 1 + βA(s).
When β•A(s) = -1, the denominator is zero and the gain becomes infinity.
This means that the transfer function diverges when β•A(s) = -1.
In other words, β•A(s) = -1 implies that the signal returned via a negative feedback is inverted (phase delay of 180deg), equivalent to the condition when a positive feedback is applied. Therefore, the circuit becomes unstable, causing an oscillation.

The following are a summary of oscillation conditions when the loop gain is 1times. (The loop gain of 1times represents an unity feedback.)

$$|\beta A(s)| = 1$$
$$\angle \beta A(s) = -180\text{deg}$$

Here ∠βA(s) is the phase delay. When s = jω1 and the loop gain βA(ω1) = 1, a phase delay of 180deg causes an oscillation with the angular frequency of ω1.

> Point
>
> There are two indicators of stability: the phase and gain margins. The phase margin indicates how much margin remains from the phase delay of 180deg when the gain is unity (0 dB). The gain margin indicates how much the gain is attenuated from unity when the phase delay is 180deg (phase margin of 0deg).

The phase delay is caused by the presence of the poles. We explain the reasoning using the frequency characteristics of an RC filter as an example.

Consider the transfer function of an RC filter as shown in Figure 7. Figure 8 shows that a pole is caused by capacitance in the transfer function (the first characteristic).

This pole produces a phase delay of 45deg at the pole frequency fc, and a phase delay of about 90deg when the frequency is about 10times that of the pole frequency.

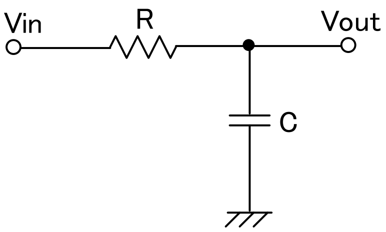


Figure 7. RC filter circuit

> Point
>
> - One pole produces a phase delay of 90deg.
> - The pole frequency depends on the capacitance value.
> - Even with a high pole frequency, the phase begins to delay when the frequency reaches 1/10 of the pole frequency.

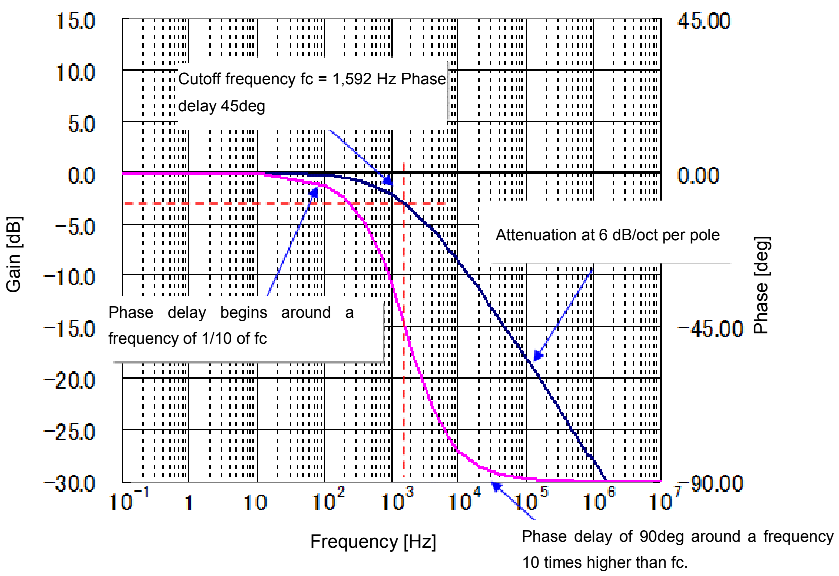


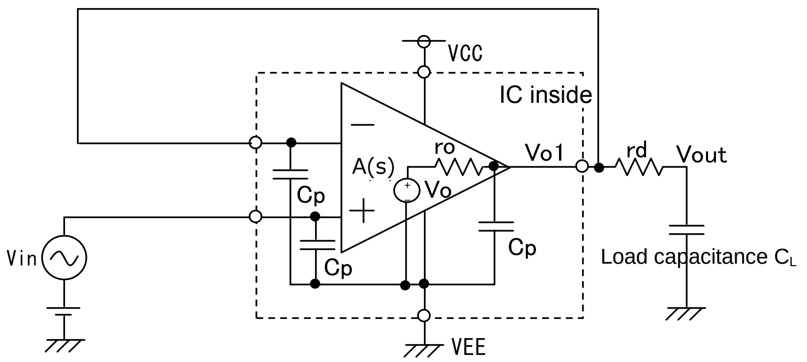
Figure 8. Frequency characteristics of RC filter

R = 1kΩ, 0.1 μF, fc = 1,592 Hz

> Transfer function of RC filter
>
> $$\frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{1}{1+j\omega RC}$$
>
> Signal amplitude
>
> $$H(\omega) = \frac{1}{\sqrt{1+(\omega RC)^2}}$$
>
> Phase
>
> $$\theta = -ArcTan(\omega RC)$$
>
> From the transfer function of the RC filter, the pole and cutoff frequencies are described as follows.
>
> $$\omega_0 = \frac{1}{RC} \quad f_c = \frac{1}{2\pi RC}$$

3. Cause of phase delay in op-amp

We consider the causes of phase delay in op-amps, including the load capacitance.



A(s): transfer function of op-amp, s = jω, ω = 2πf

f: frequency, ro: output impedance, Cp: parasitic capacitance of terminal, C_L: load capacitance

Figure 9. Unity feedback circuit

Point

- Pole caused by the output impedance and the parasitic capacitance of the terminals
- Pole caused by the output impedance and the load capacitance (intentionally provided)
- Pole caused by the feedback resistor and the parasitic capacitance of the input terminal when an amplifier circuit is configured

From the transfer function of the circuit in Figure 9, we explain the cause of phase delay for an unity feedback circuit (voltage follower), which is most susceptible to oscillations.

$$A(s)(V_{in} - V_{o1}) = V_o$$

$$V_{o1} = \frac{\frac{1}{sC_p}}{r_o + \frac{1}{sC_p}} = \frac{1}{1 + r_o C_p s} V_o$$

From the equations above, the transfer function is described as follows when the output impedance (ro) and the terminal capacitance are taken into account (Cp represents the total of parasitic capacitances).

$$\frac{V_{o1}}{V_{in}} = \frac{A(s)}{1 + r_o C_p s + A(s)} = \frac{1}{1 + \frac{1 + C_p r_o s}{A(s)}}$$

A pole is formed by Cp and ro.
This effect is considered in the op-amp design.

In the equation above, assuming Cp = Cp + C_L gives the transfer function when the load capacitance is connected.

$$\frac{V_{o1}}{V_{in}} = \frac{A(s)}{1 + r_o (C_p + C_L) s + A(s)} = \frac{1}{1 + \frac{1 + (C_p + C_L) r_o s}{A(s)}}$$

A pole is formed by Cp + C_L and ro.
Cp varies little since it is the parasitic capacitance inside the IC. However, the frequency where the pole occurs is reduced if the load capacitance C_L is large.

4. Stability confirmation method (amplifier circuit)

As an actual example, we show the variations in the phase and frequency characteristics according to the value of the load capacitance C_L for the BA2904.

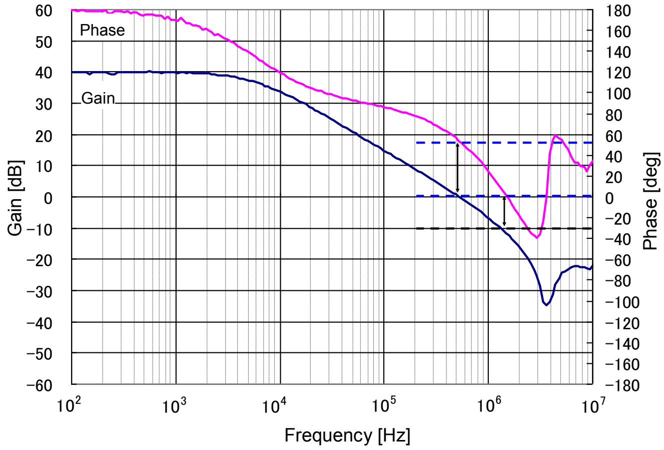


Figure 10. Frequency characteristics of BA2904 (C_L = 25 pF)

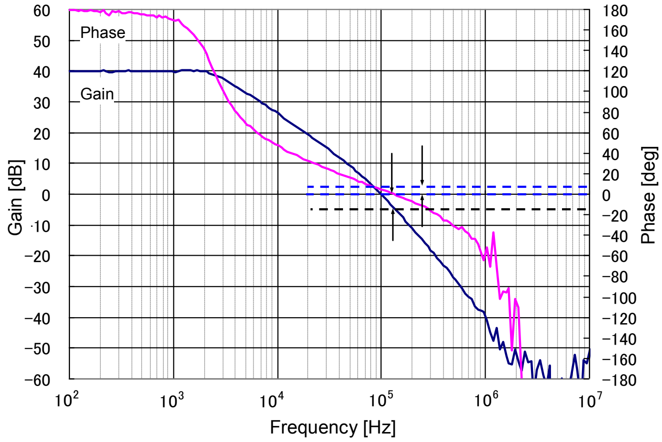


Figure 11. Frequency characteristics of BA2904 (C_L = 0.01 µF)

- When C_L = 25 pF
  Phase margin: 55deg → the phase when the gain is 0 dB
  Gain margin: -10 dB → the gain when the phase is 0deg

- When C_L = 0.01 µF
  Phase margin: 7deg → the phase when the gain is 0 dB
  Gain margin: -5 dB → the gain when the phase is 0deg
  Although the phase margin is small, no oscillation occurs.

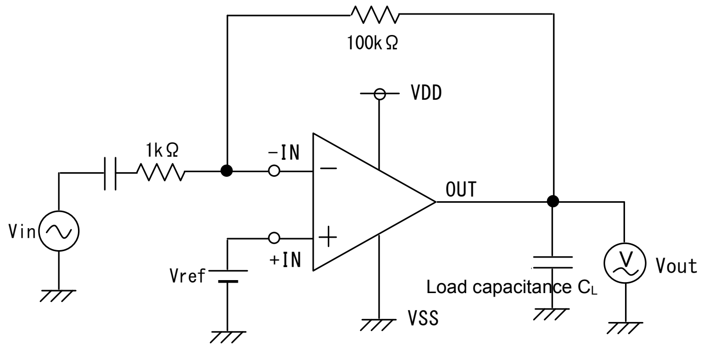


Figure 12. Inverting amplifier circuit of 40 dB (100 times)

Point

- The oscillation stability of op-amps is confirmed with the phase and gain margins.
- In an inverting amplifier circuit, the phase margin is the phase when the gain is 0 dB since the phase begins from 180deg.
- In a non-inverting amplifier circuit, the phase margin is the difference between 180deg and the phase value when the gain is 0 dB since the phase begins from 0deg.
- Considering factors such as variations or temperature change, the phase margin is designed to be 35deg or larger, and the gain margin -7 dB or smaller.

5. Stability confirmation method (unity feedback circuit/voltage follower)

We review the idea of phase margin.

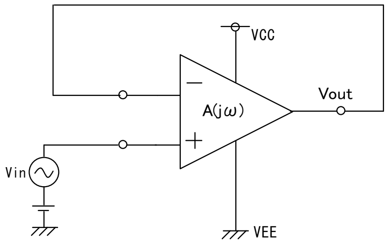


Figure 13. Overall feedback circuit

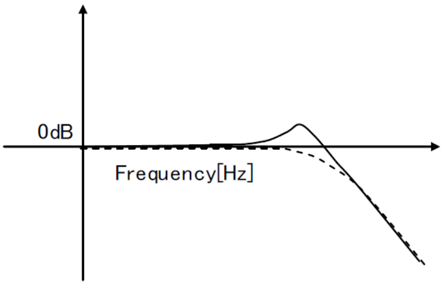


Figure 14. Measurement result

- The phase margin indicates how much margin remains from the phase delay of 180deg when the gain is unity (0 dB).
- The gain margin indicates how much the gain is attenuated from unity when the phase delay is 180deg (phase margin of 0deg).

The methods that we have explained so far cannot confirm the phase margin in an unity feedback circuit (gain of 0 dB). When the circuit becomes less stable, a peak gain appears in the frequency characteristic as shown in Figure 14. The phase margin is calculated from the size of the produced peak using the transfer function.

Transfer function of a voltage follower (unity feedback circuit)

$$\frac{V_{out}}{V_{in}}(j\omega)=\frac{A(j\omega)}{1+\beta A(j\omega)}$$

A(jω) is expressed in complex form and substituted in the transfer function.

$$A(j\omega)=\exp(j\theta)$$

$$\frac{Vout}{Vin}(j\theta)=\frac{\frac{1}{\beta}\exp(j\theta)}{\frac{1}{\beta}+\exp(j\theta)}=\frac{\frac{1}{\beta}(\cos\theta+j\sin\theta)}{\frac{1}{\beta}+\cos\theta+j\sin\theta}$$

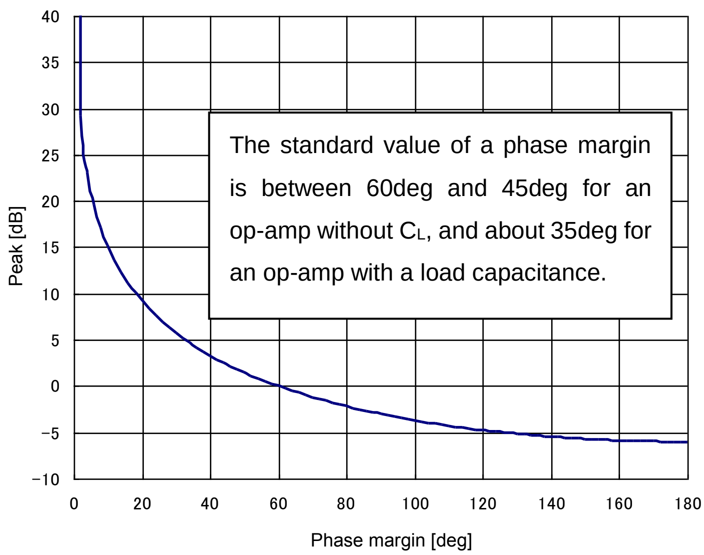


Figure 15. Result of gain peak calculation

Figure 15 shows the result of the calculation when the following values are substituted in the above equations.
θ(ω1) = -175deg (5deg), θ(ω2) = -135deg (45deg), θ(ω3) = -120deg (60deg), β=1.
As the result shows in Figure 15, the phase margin of 60deg corresponds to a peak of 0 dB, giving an ideal condition.

Phase margin	Result of calculation [times]	Peak [dB]
5deg	11.5	21
45deg	1.3	2
60deg	1	0

Point

- By measuring the frequency characteristics of a voltage follower, the phase margin can be calculated from the gain peak.
- This method is applicable to any types of general op-amps.
- When the phase margin is small, the occurrence of oscillation is actually confirmed using an oscilloscope or other instruments.

6. Summary of stability confirmation method

When an amplifier circuit is configured

• Oscillation in an amplifier circuit is confirmed by measuring the phase frequency characteristic and checking the phase and gain margins.

• In an inverting amplifier circuit, the reading of the phase margin is the phase when the gain is 0 dB since the phase begins from 180deg.

• In a non-inverting amplifier circuit, the phase margin is the difference between the phase when the gain is 0 dB and 180deg since the phase begins from 0deg.

• Considering factors such as variations or temperature change, the phase margin is designed to be 35deg or larger as a standard, and the gain margin -7 dB or smaller.
(Generally, the phase margin is designed to be between 60deg and 40deg for an op-amp alone.)

When an unity feedback circuit (voltage follower) is configured

• By measuring the frequency characteristics between the input and output and checking the gain peak, the phase margin can be estimated from Figure 15 of this document.

• Figure 15 is applicable to any types of general op-amps.

• When the phase margin is small, the occurrence of oscillation should actually be confirmed.

• Considering factors such as variations or temperature change, the phase margin is designed to be 35deg or larger as a standard.

Since the confirmation of oscillation with the calculations above is complicated, it is generally confirmed by experiment.

7. Countermeasures against oscillation by load capacitance (output isolation resistor 1)

Basically, it is possible to prevent oscillation by satisfying the conditions to avoid oscillation as described in the previous sections. In this section, however, we explain countermeasures against oscillation when a capacitor with a large capacitance is connected to the output terminal.

We calculate the transfer function in Figure 16.

$$A(s)(V_{in}-V_{o1})=V_o$$

$$V_{o1}=\frac{\frac{1}{sC_p}}{r_o+\frac{1}{sC_p}}=\frac{1}{1+r_oC_ps}V_o$$

$$\frac{V_{o1}}{V_{in}}=\frac{A(s)}{1+r_oC_ps+A(s)}=\frac{1}{1+\frac{1+C_pr_os}{A(s)}}$$

$$\frac{V_{out}}{V_{o1}}=\frac{1}{1+r_dC_Ls}$$

$$\frac{V_{o1}}{V_{in}}\frac{V_{out}}{V_{ol}}=\frac{A(s)}{1+r_oC_ps+A(s)}\frac{1}{(1+r_dC_Ls)}$$

$$\frac{V_{out}}{V_{in}}=\frac{A(s)}{(1+r_oC_ps+A(s))}\frac{1}{(1+r_dC_Ls)}$$

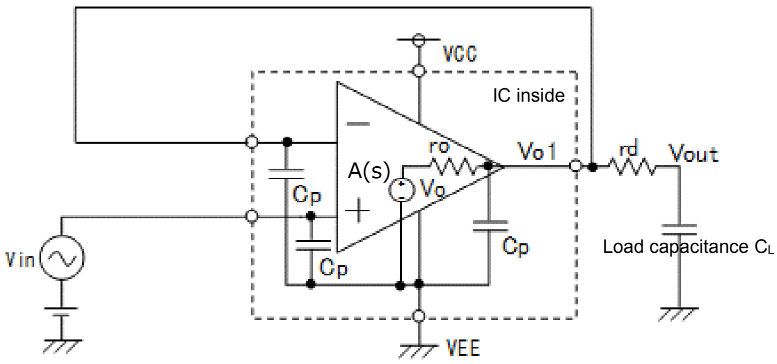


Figure 16. Example of output isolation resistor connection 1

> Point
> - The value of the isolation resistor is set to between 50Ω to several hundred ohms, according to the capacitance and the required frequency bandwidth.
> - Since a low pass filter is configured with rd and CL, the circuit bandwidth is reduced if the load capacitance is large.

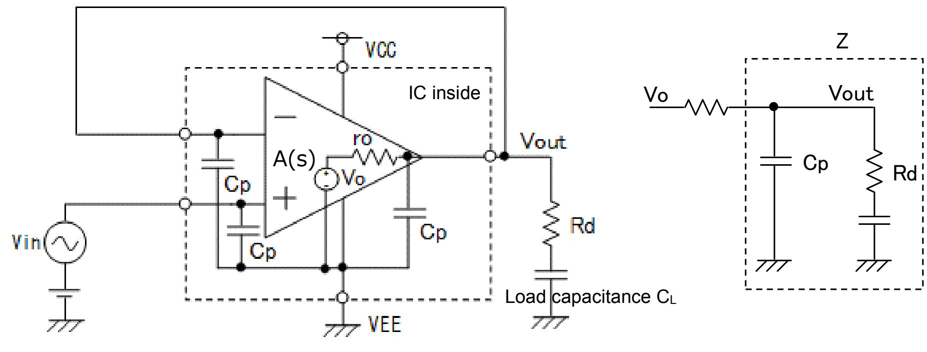
While the transfer function without the isolation resistance calculated in Figure 9 is

$$\frac{V_{o1}}{V_{in}}=\frac{A(s)}{1+r_o(C_p+C_L)s+A(s)}$$

When these two transfer functions are compared, it can be seen that the capacitance CL that is connected to the output is separated into another transfer function with the dividing resistance rd.

8. Countermeasures against oscillation by load capacitance (output isolation resistor 2)

When using the method to insert an output isolation resistor as described in the previous section, the configuration of a low pass filter may be disadvantageous in some applications. The peak gain is reduced by inserting a resistor in series to the capacitance.



$$Z = \frac{1}{sC_p + \frac{1}{R_d + \frac{1}{sC_L}}}$$

$$Z = \frac{R_d + \frac{1}{sC_L}}{1 + sC_p(R_d + \frac{1}{sC_L})}$$

Figure 17. Example of output dividing resistor connection 2

We calculate the transfer function in Figure 17.

$$A(s)(V_{in} - V_{out}) = V_o \qquad V_o = A(s)V_{in} - A(s)V_{out} \qquad V_{out} = \frac{Z}{r_o + Z}V_o$$

$$(1 + \frac{r_o}{Z})V_{out} = A(s)V_{in} - A(s)V_{out} \qquad (A(s) + 1 + \frac{r_o}{Z})V_{out} = A(s)V_{in}$$

$$\frac{V_{out}}{V_{in}} = \frac{A(s)}{A(s) + \frac{1}{Z}r_o + 1} \qquad \frac{V_{out}}{V_{in}} = \frac{1}{A(s) + \frac{1 + sC_p(R_d + \frac{1}{sC_L})}{R_d + \frac{1}{sC_L}}r_o + 1}$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{A(s) + r_o\underline{\underline{\frac{C_L + C_p(sC_L + 1)}{sC_L R_d + 1}s}} + 1} \qquad ...A$$

This part of the transfer functions is different.

While the transfer function without the isolation resistance calculated in Figure 9 is

$$\frac{V_{o1}}{V_{in}} = \frac{A(s)}{1 + r_o\underline{\underline{(C_p + C_L)s}} + A(s)}$$

> Point
> - The value of the isolation resistor is set to between 50 Ω to several hundred ohms, according to the capacitance and the required frequency bandwidth.

We analyze the frequency characteristic of the underlined part in equation A.
Suppose that S = jω = j2πf.

$$X = \frac{C_L + C_p(sC_L + 1)}{sC_L R_d + 1}$$

When f → 0: s → 0 and X → C_L + Cp
When f → ∞: s → ∞, sC_LRd >> 1, C_L << Cp (sC_L + 1),
and sC_L >> 1. Therefore, X is converged to Cp/Rd.
This result shows that the effect of the load capacitance C_L is removed.

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