Thermal Design

Heat Dissipation Effect of Thermal Via in Exposed Pad Type Package

For a device with a large power consumption in a small surface mounted type package, such as a power supply IC in the quad flat non-leaded (QFN) or quad flat package (QFP), the exposed pad type package is used in which the die pad is exposed to the outside of the package. The heat dissipation path in this package is mainly the copper foils of the printed circuit board (PCB). However, the heat dissipation performance may not be achieved as expected due to difference in the PCB layouts. This application note explains the heat dissipation effect of a thermal via for successfully dissipating the heat in the exposed pad type packages.

Heat dissipation paths in the surface mounted packages

This section explains the thermal conduction paths in the surface mounted packages from the heat source into the surrounding environment. Figure 1 shows a normal surface mounted package. The thermal conduction from the heat source in the direction of the upper surface is small because of a high thermal resistance of the mold. Since the surface area is small, it is expected that the radiation of the heat conducted to the upper surface can hardly contribute to the heat dissipation. Next, there is a thermal conduction path from the heat source through the lead inside the package to the copper foils of the PCB. However, this heat transmission is also small due to the high thermal resistance of the mold. Finally, the heat transmission in the direction of the back surface is small because of the air layer caused by the standoff between the package and the PCB. Many surface mounted packages are small and have a small surface area. Therefore, their heat dissipation is small and they are basically not suitable for applications with a large power consumption.

Figure 2 shows the thermal conduction paths in the exposed pad type in which the die pad is exposed on the back surface of the package in order to improve the heat dissipation. The thermal conduction from the heat source in the directions of the upper surface and the lead is the same as shown in Figure 1. However, the thermal resistance in the direction of the back surface can be lowered by connecting the die pad in contact with the heat source to the copper foils of the PCB. For the heat dissipation in the exposed pad type, the thermal resistance of the package is lowered by conducting the heat through the via in the PCB to the copper foils on the middle and outer (bottom) layers and radiating the heat from the PCB with a large surface area. Therefore, it is essential to secure the thermal conduction path through the via to the copper foils.

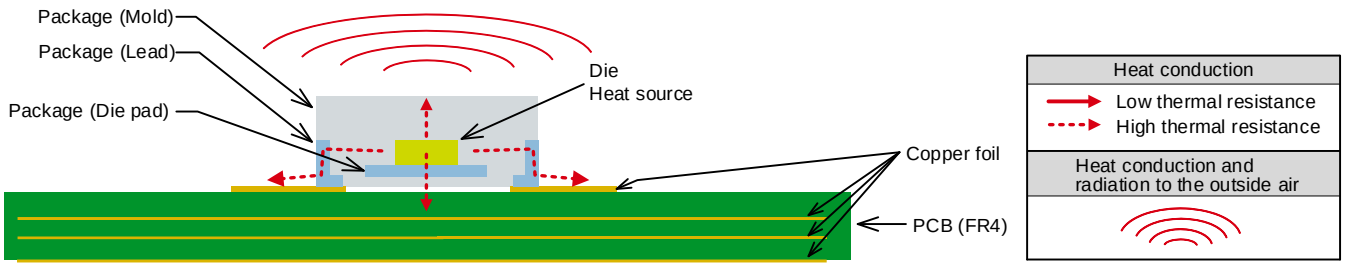

Figure 1. Thermal conduction paths in the normal surface mounted package

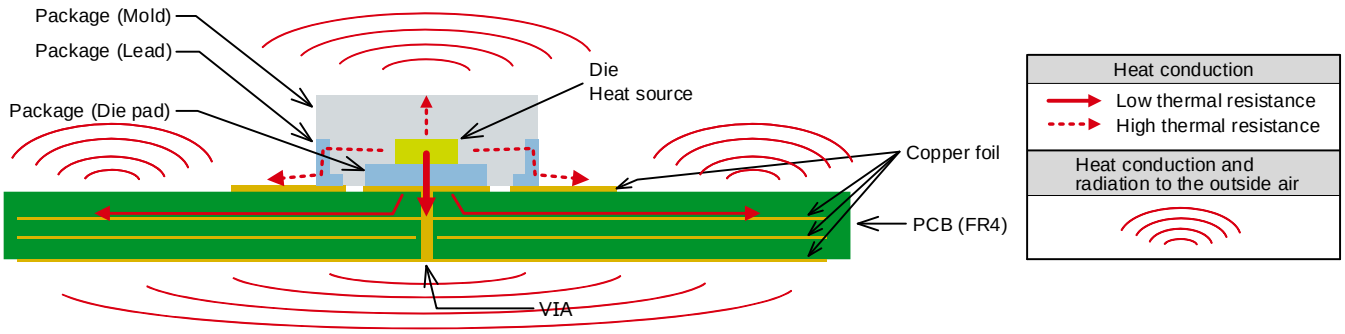

Figure 2. Thermal conduction paths in the exposed pad type

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Change in the thermal resistance due to the presence or absence of the via

This section explains how much the presence or absence of the via can change the thermal resistance.

Case 1 is the VQFN16FV3030 package, in which the center of the back surface of the package entirely serves as the exposed pad as shown in Figure 3. Since the exposed pad of this device is at the ground potential, it can be connected through the via to the ground plane where a large area can be easily secured. Figure 4 shows the change in the thermal resistance. The absence of the via results in as much as 35% higher thermal resistance.

Case 1

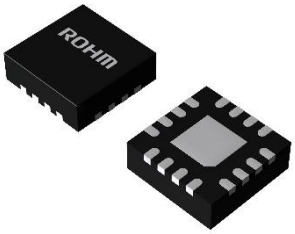
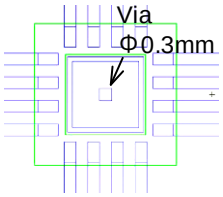
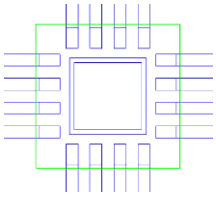


Figure 3. VQFN016V3030 package
3.00 mm × 3.00 mm × 1.00 mm

	With via	No via
PCB Layout		
Thermal resistance*1	58.4°C/W	78.8°C/W
T_J *2	108.4°C	128.8°C

*1: Simulation values for a 4-layer board in accordance with the JEDEC

*2: When P_D = 1 W, T_A = 50°C

Figure 4. Change in the thermal resistance due to the presence or absence of the via

Case 2 is the VMMP16LZ3030 package, in which functional pins (electrodes) are placed in the center of the back surface of the package as shown in Figure 5. For the device in this figure, the larger and smaller pins are assigned to function as the power supply input and the switching output, respectively.

Figure 6 shows the change in the thermal resistance. The thermal resistance can be lowered by connecting the power supply input pin (the larger pin) through the via to the copper foils on the middle layers. A difference of 16% is obtained due to the presence or absence of the via in this example, although the difference is smaller compared with case 1. This is because the copper foils on the middle layers are the power supply lines, making it impossible to secure a large copper foil area in contrast to the ground plane in case 1. However, it is essential to lower the thermal resistance by conducting the heat through the via to the copper foils on the middle layers.

Since the smaller pin functions as the switching output in this device, providing a large copper foil area for the heat dissipation in the layout may cause issues with the EMI. Therefore, the copper foil area is minimized. If such issues are prevented with the pin assignment, set the via and conduct the heat to the copper foils on the middle layers as in the case for the larger pin.

Case 2

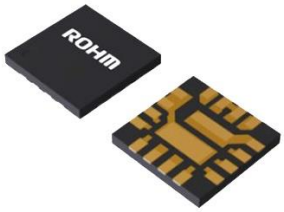
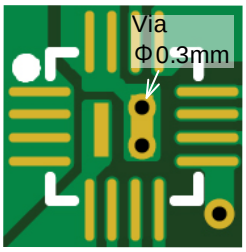
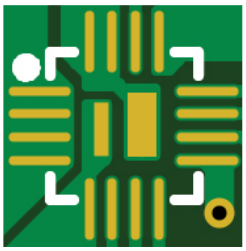


Figure 5. VMMP16LZ3030 package
3.0 mm × 3.0 mm × 0.40 mm

	With via	No via
PCB Layout		
Thermal resistance*3	49.0°C/W	54.2°C/W
T_J *4	113.7°C	120.5°C

*3: Simulation values for the BD9F500QUZ-EVK-001 board

*4: When P_D = 1.3 W, T_A = 50°C

Figure 6. Change in the thermal resistance due to the presence or absence of the via

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