LVDS Interface ICs

System Diagram and PCB Design Guide Line

BU8254KVT, BU90R104

No.11057EAY01

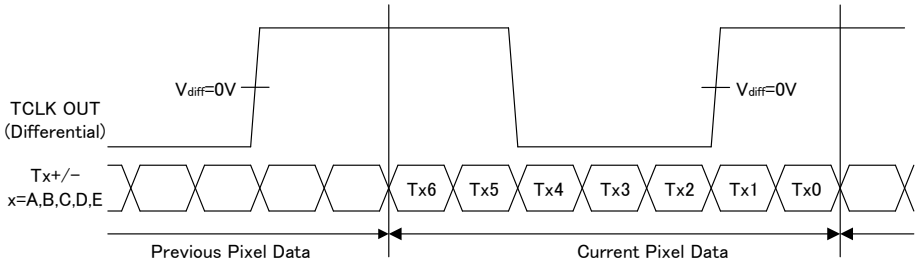
35bit LVDS Transmitter 35:5 Serializer

BU8254KVT

35bit LVDS Receiver 5:35 Deserializer

BU90R104

●LVDS Data Timing Diagram



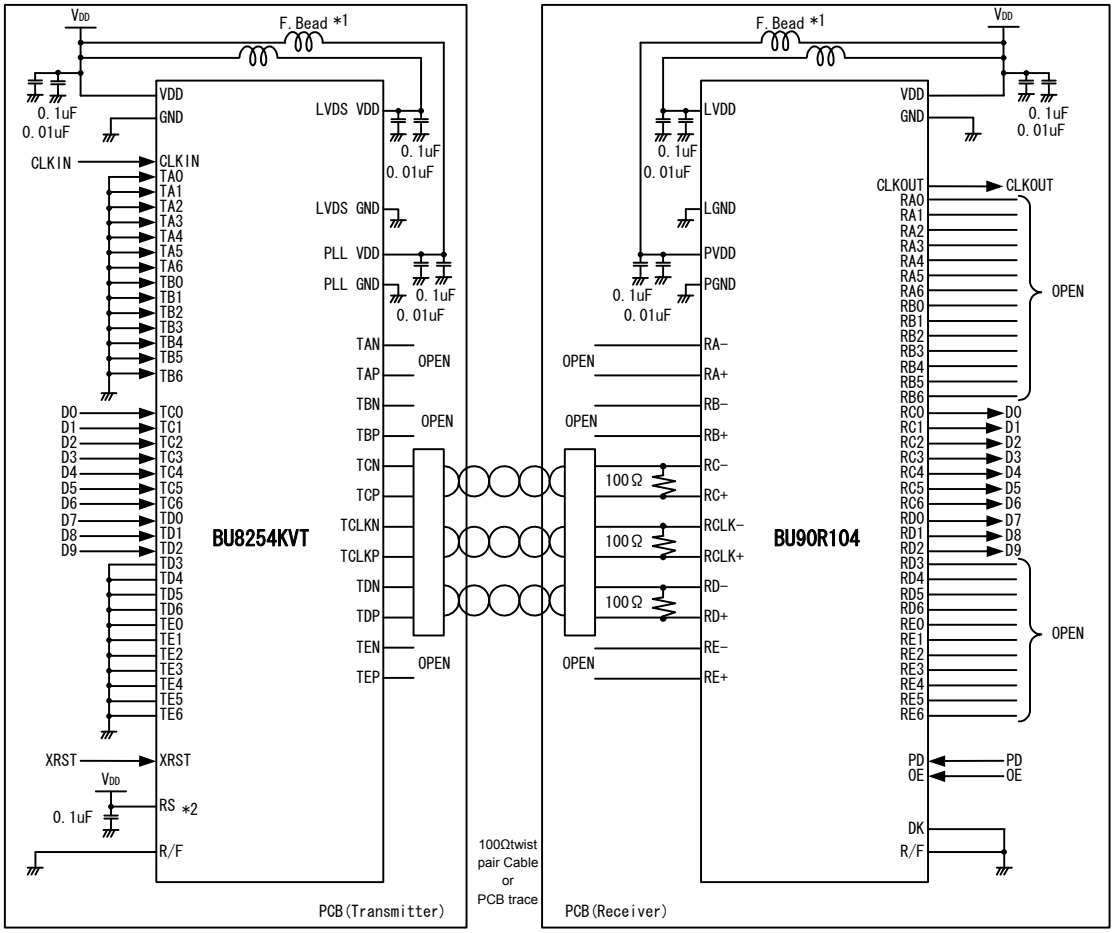
BU8254KVT/BU90R104 Pixel Data Assign (6bit, 8bit, 10bit Application)

	6bit Color	8bit Color	10bit Color
TA0	R4	R4	R4
TA1	R5	R5	R5
TA2	R6	R6	R6
TA3	R7	R7	R7
TA4	R8	R8	R8
TA5	R9	R9	R9
TA6	G4	G4	G4
TB0	G5	G5	G5
TB1	G6	G6	G6
TB2	G7	G7	G7
TB3	G8	G8	G8
TB4	G9	G9	G9
TB5	B4	B4	B4
TB6	B5	B5	B5
TC0	B6	B6	B6
TC1	B7	B7	B7
TC2	B8	B8	B8
TC3	B9	B9	B9
TC4	Hsync	Hsync	Hsync
TC5	Vsync	Vsync	Vsync
TC6	DE	DE	DE
TD0	-	R2	R2
TD1	-	R3	R3
TD2	-	G2	G2
TD3	-	G3	G3
TD4	-	B2	B2
TD5	-	B3	B3
TD6	-	N/A	N/A
TE0	-	-	R0
TE1	-	-	R1
TE2	-	-	G0
TE3	-	-	G1
TE4	-	-	B0
TE5	-	-	B1
TE6	-	-	N/A

Note : N/A=Not Assigned
Note : For 6bit application, use A _ C channel and open TD+/-,TE+/- pin.
: For 8bit application, use A _ D channel and open TE+/- pin.

●10bit Data 3.3V LVCMOS Level Input

Example:
BU8254KVT : 3.3V LVCMOS level input/Falling edge/Normal swing
BU90R104 : Falling edge



*1 : Recommended Parts:
F.Bead : BLM18A-Series (Murata Manufacturing)
*2 : If RS pin is tied to V_{DD}, LVDS swing is 350m V.
If RS pin is tied to GND, LVDS swing is 200m V.

●10bit Data Low Level Swing Input

Example:
BU8254KVT : 1.2V/1.5V/1.8V/2.5V LVCMOS level input/Falling edge/Normal swing
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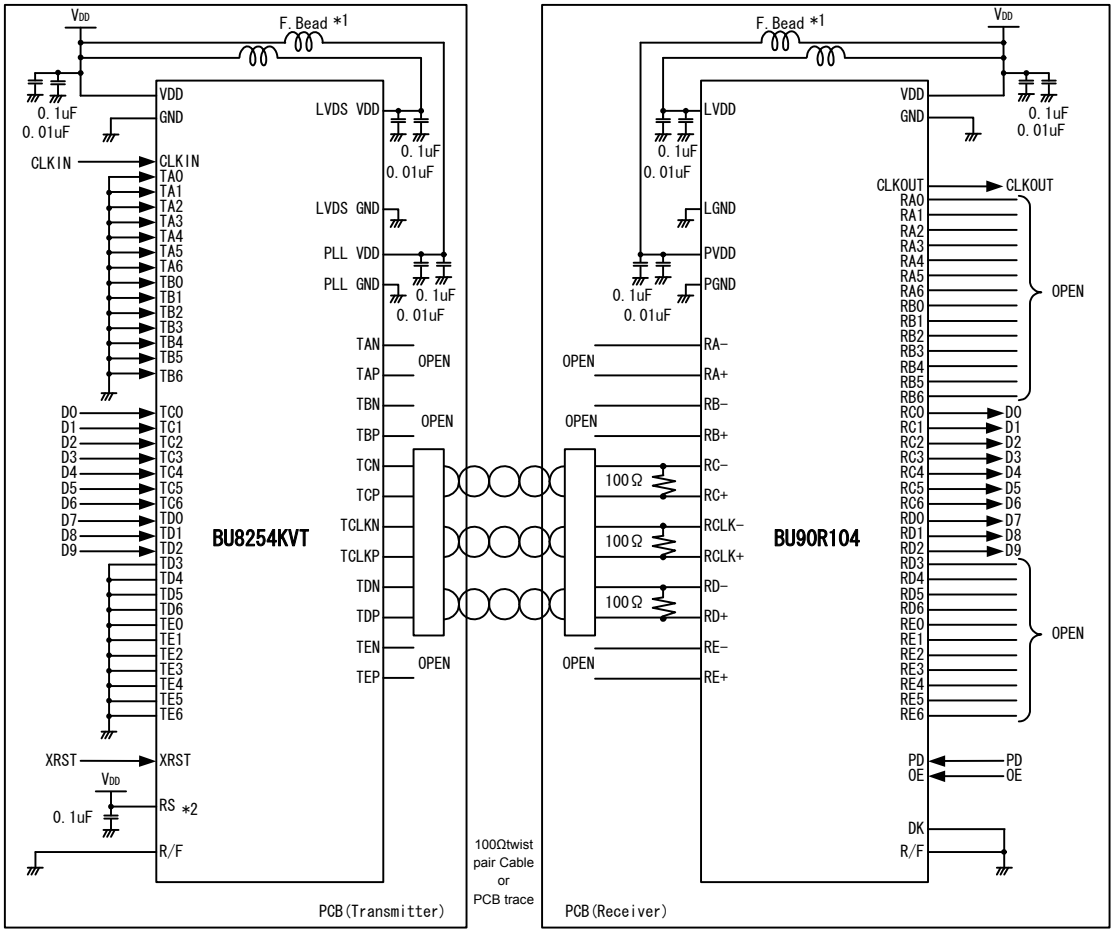
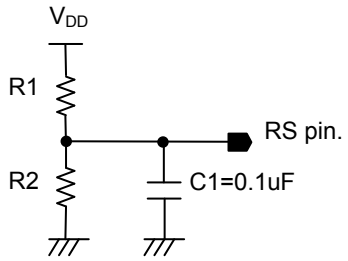


*3 : Recommended Parts:
Bead : BLM18A-Series (Murata Manufacturing)
*4 : S pin acts as VREF input pin when input voltage is set to half of high level signal input.
We recommend to locate by-pass condenser near the RS pin.



Example for LVCMOS(1.2V input):(R1,R2)=(22kΩ,5.1kΩ)
LVCMOS(1.5V input):(R1,R2)=(18kΩ,5.1kΩ)
LVCMOS(1.8V input):(R1,R2)=(15kΩ,5.6kΩ)
LVCMOS(2.5V input):(R1,R2)=(10kΩ,6.2kΩ)

●10bit Color Depth 3.3V LVCMOS Level Input (QVGA, VGA, SVGA ,XGA, WXGA, SXGA)

Example:
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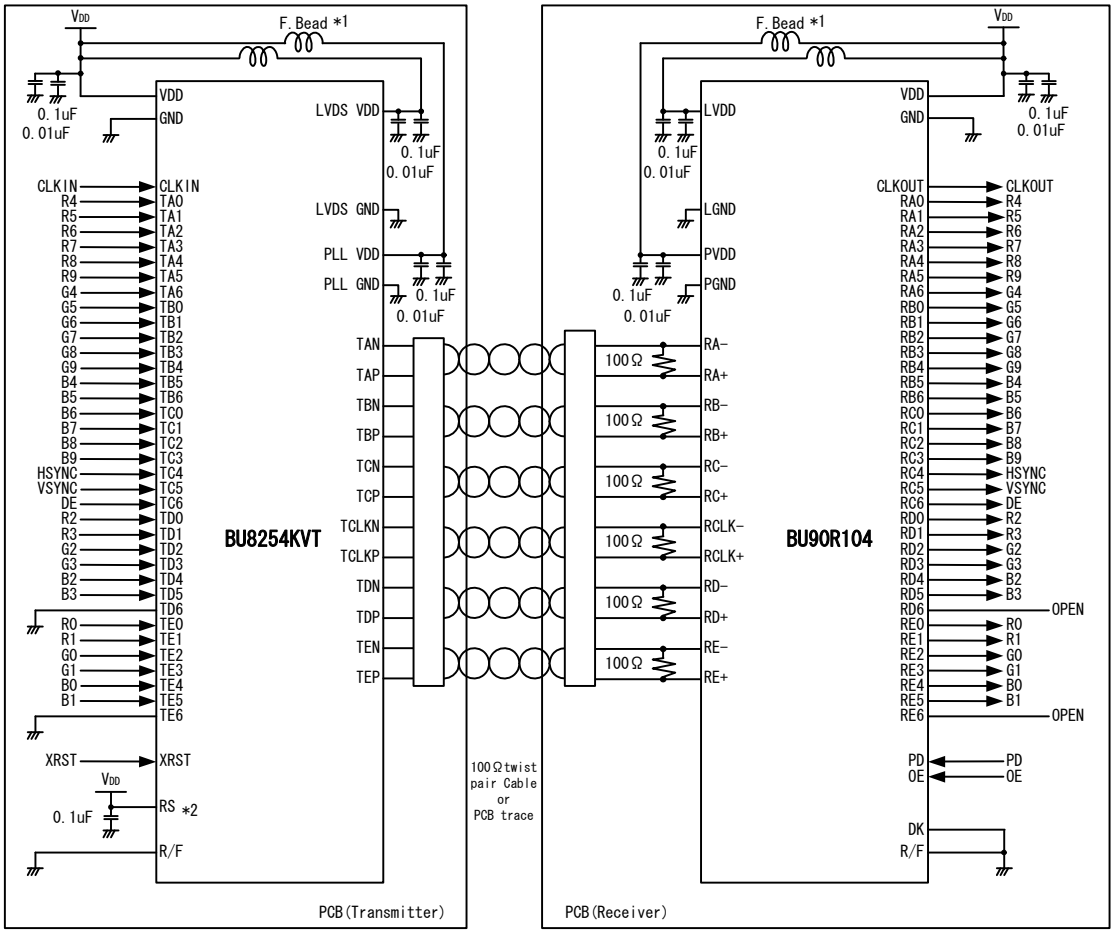

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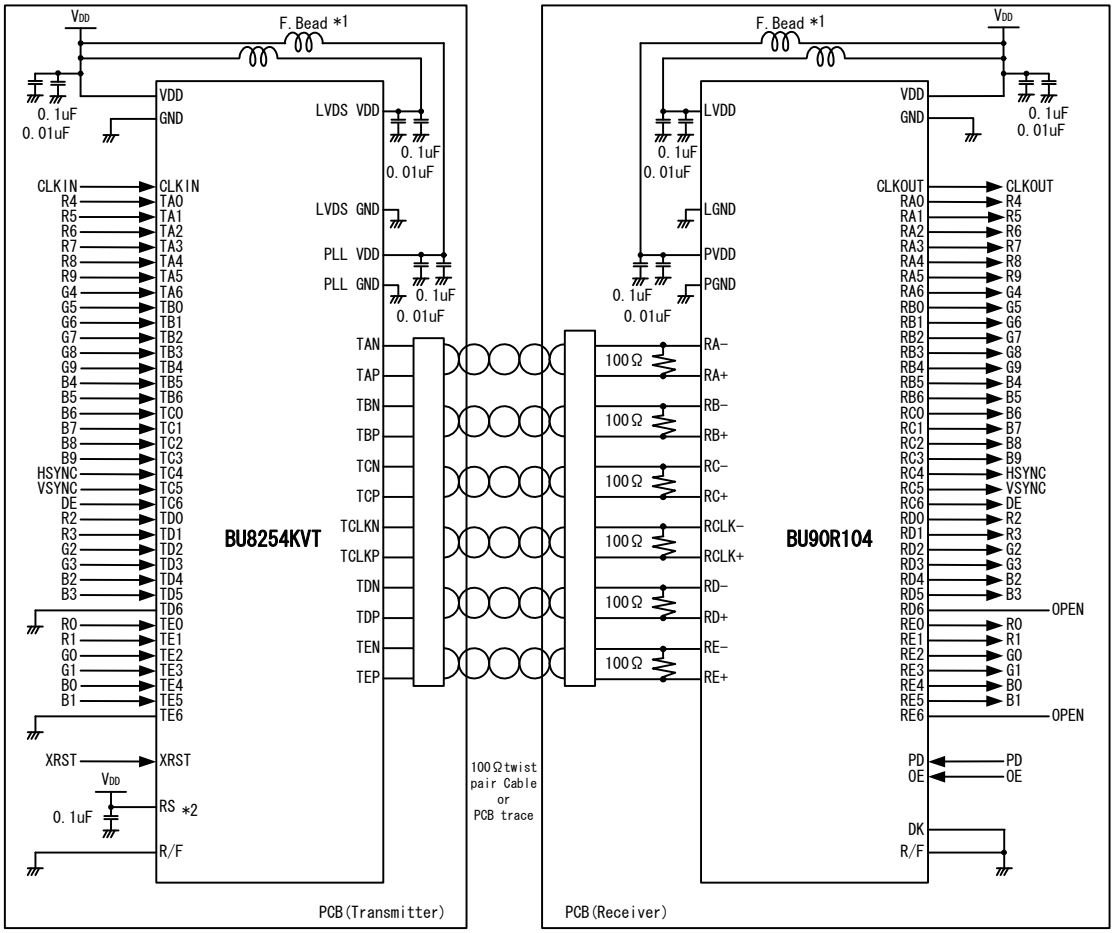

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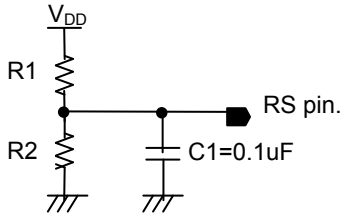

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●8bit Color Depth 3.3V LVCMOS Level Input (QVGA, VGA, SVGA ,XGA, SXGA, SXGA+)

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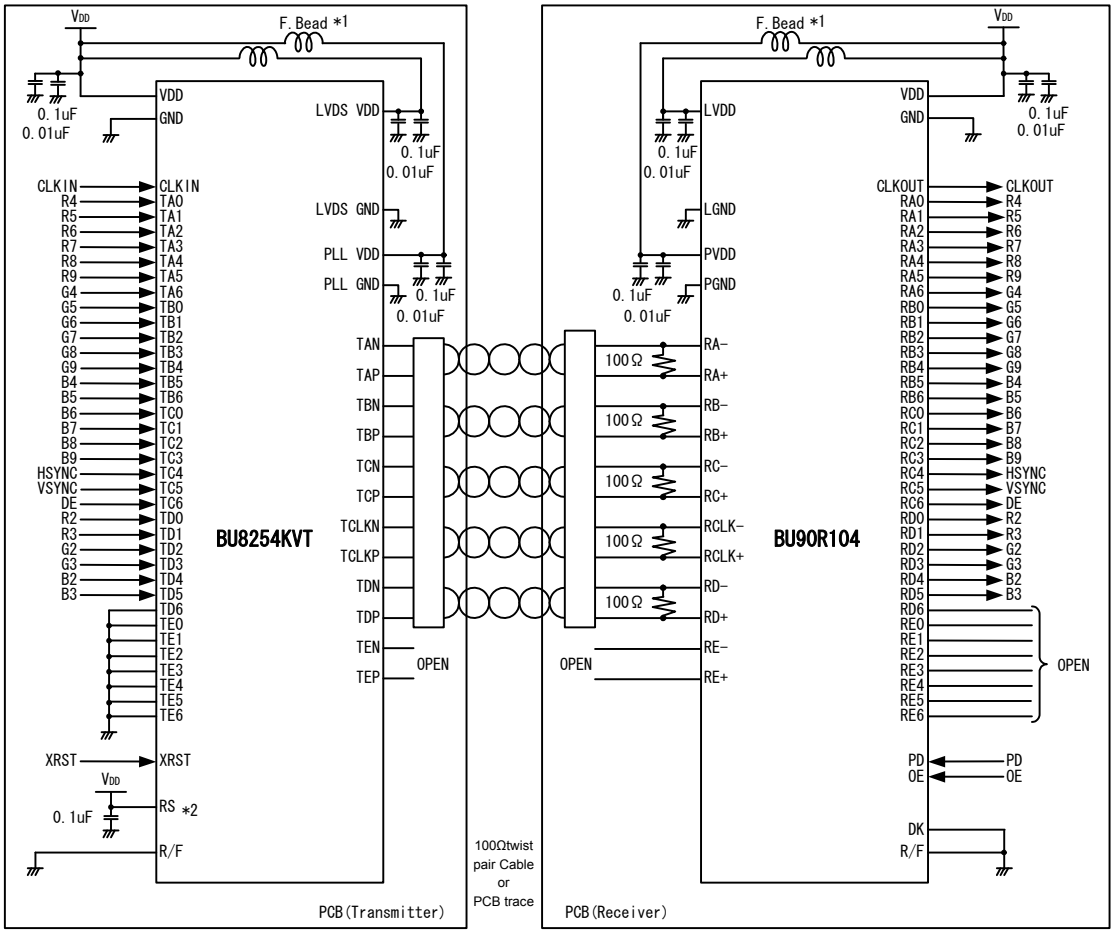

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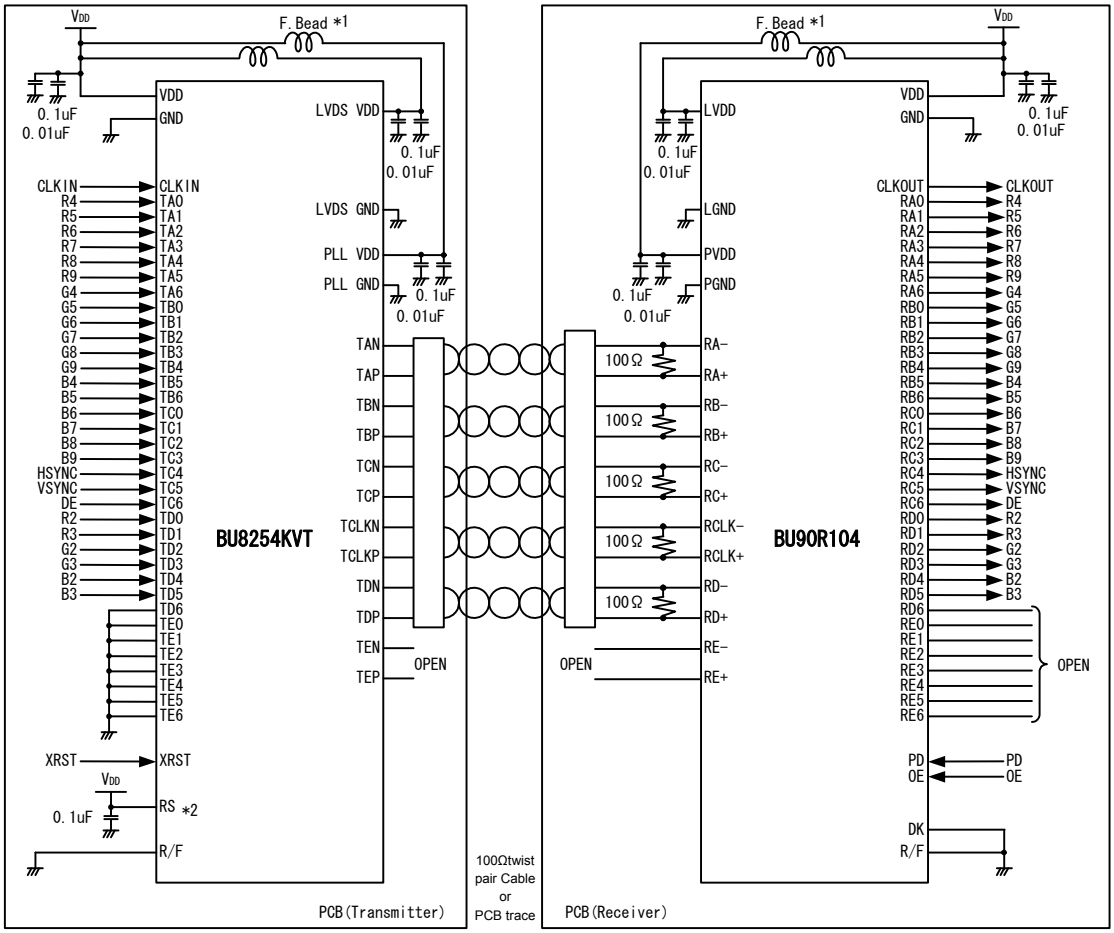

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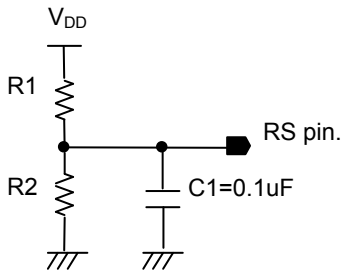

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●6bit Color Depth 3.3V LVCMOS Level Input (QVGA, VGA, SVGA ,XGA, SXGA, SXGA+)

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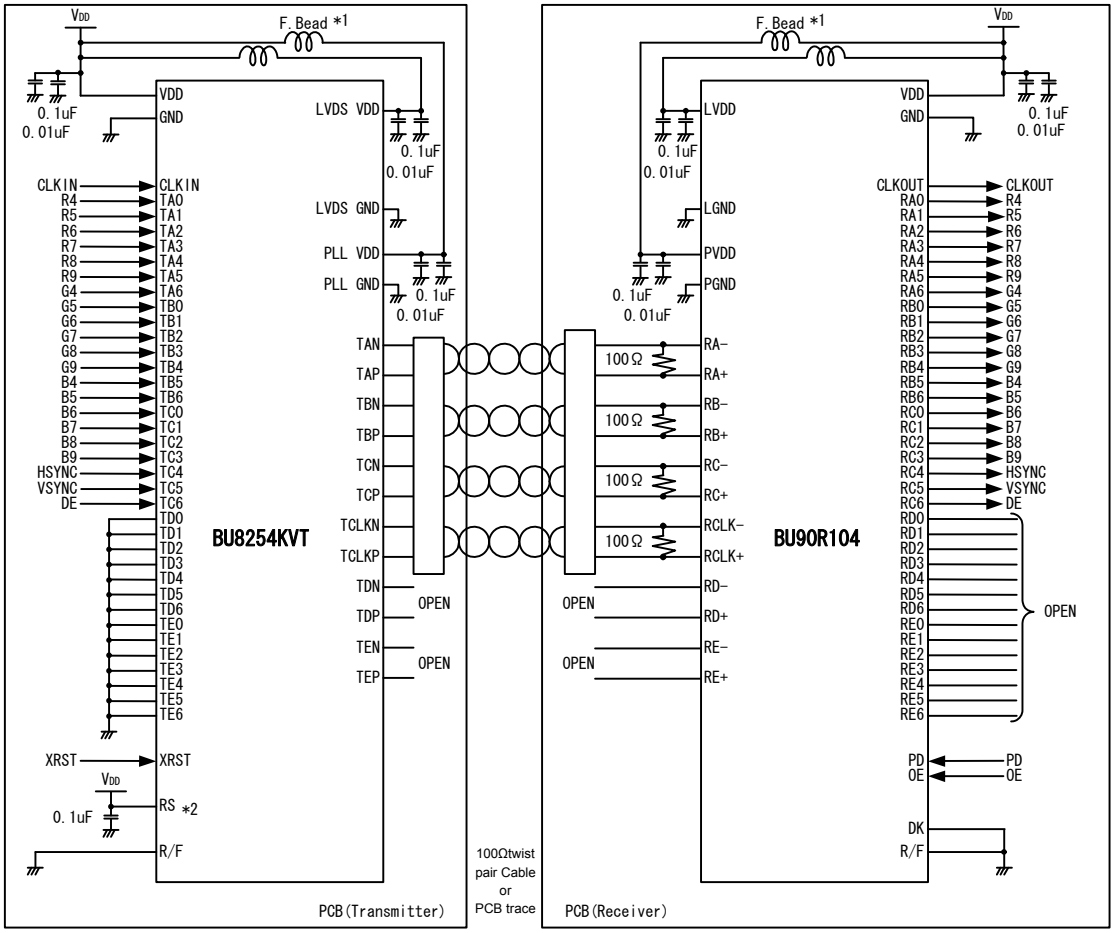
BU90R104 : Falling edge



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●6bit Color Depth Low Level Swing Input (QVGA, VGA, SVGA ,XGA, SXGA, SXGA+)

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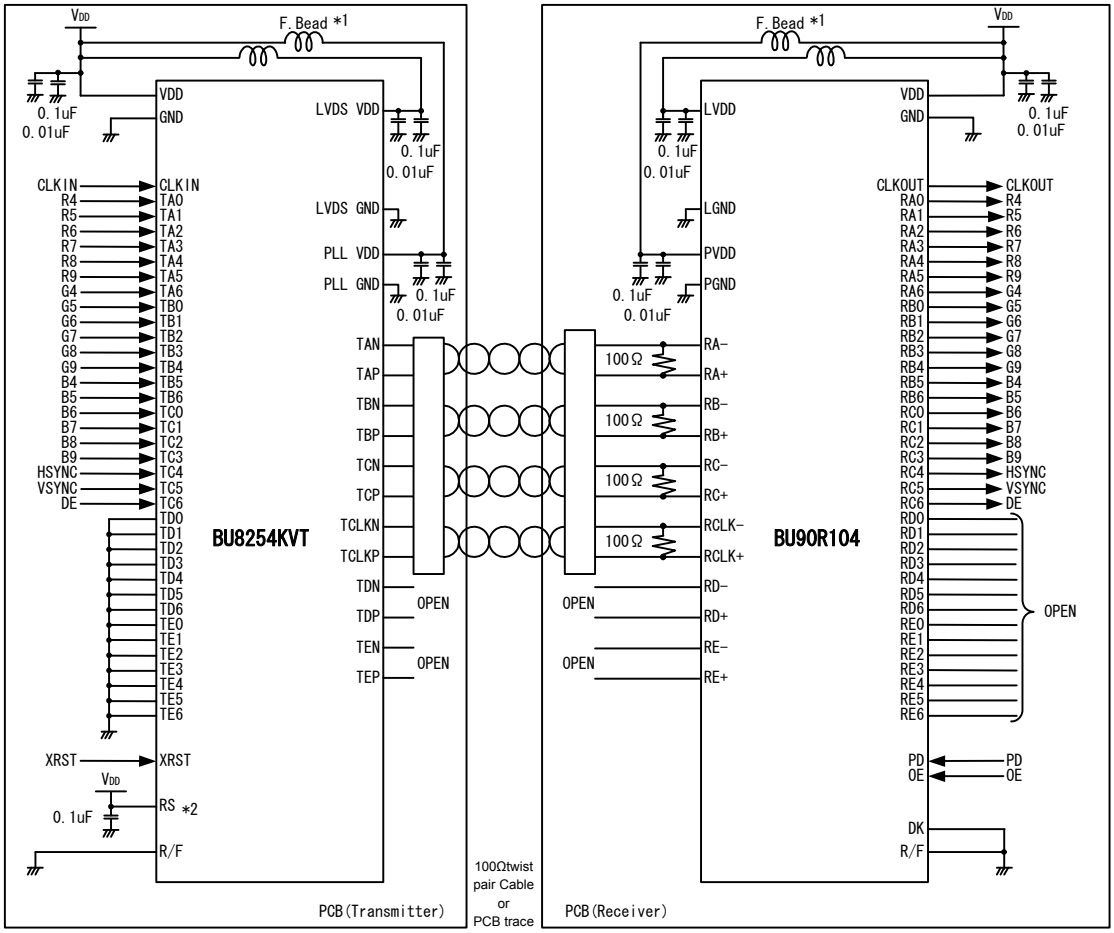

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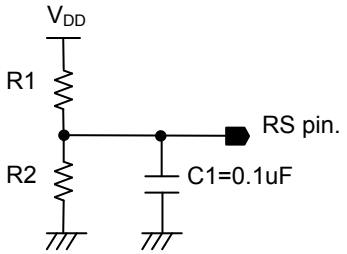

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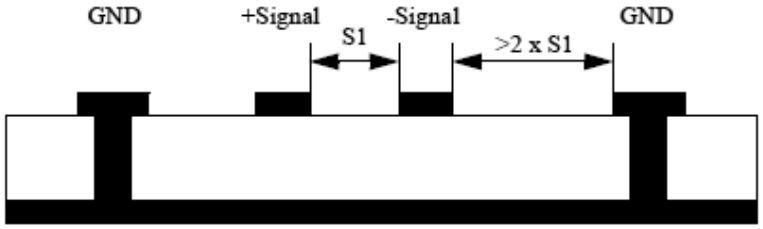
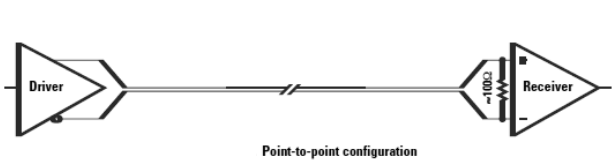
●PCB Design Guide Line for LVDS

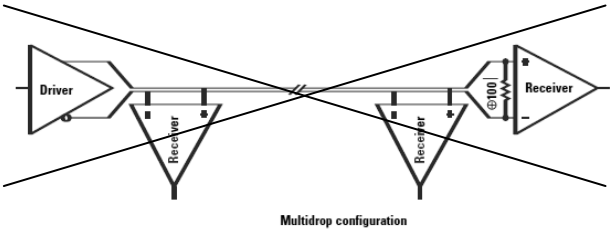
- Interconnecting media between Transmitter and Receiver (i.e. PCB trace, connector, and cable) should be well balanced.(Keep all these differential impedance and the length of media as same as possible.).
- Locate by-pass capacitors adjacent to the device pins as close as possible.
- Minimize the distance between traces of a pair (S1) to maximize common mode rejection.
  See following figure.
- Place adjacent LVDS trace pair at least twice (>2 x S1) as far away.
- Avoid 90 degree bends.
- Minimize the number of VIA on LVDS traces.
- Match impedance of PCB trace, connector, media (cable) and termination to minimize reflections (emissions) for cabled applications (typically 100. differential mode characteristic impedance).
- Use 4 layer PCB (minimum).



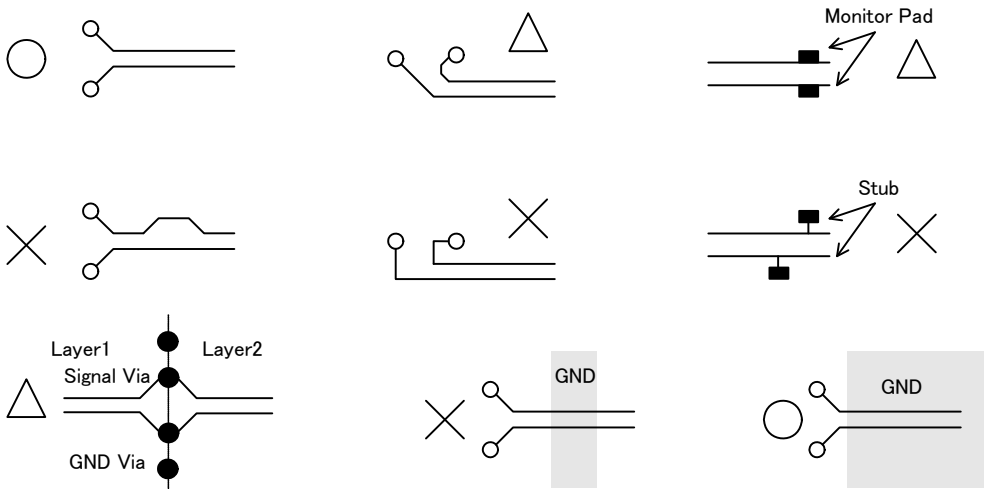
Recommend the CITS series or Si series of Polar Instruments company to the calculation of impedance



Good



No Good



●Ordering part number

B	U	8	2	5	4	K	V	T	-	E	2

Part No.

Part No.
8254

Package
KVT: TQFP64V

Packaging and forming specification
E2: Embossed tape and reel

B	U	9	0	R	1	0	4	-	E	2

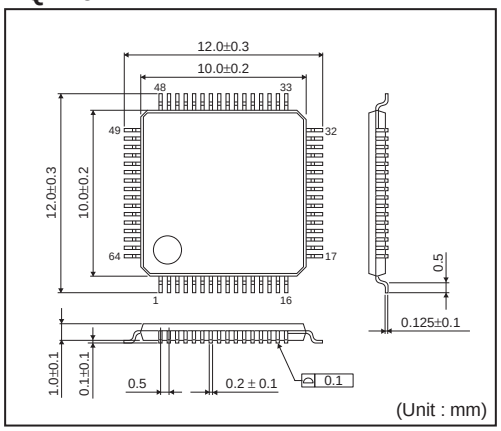
Part No.

Part No.
90R104

Package
TQFP64V

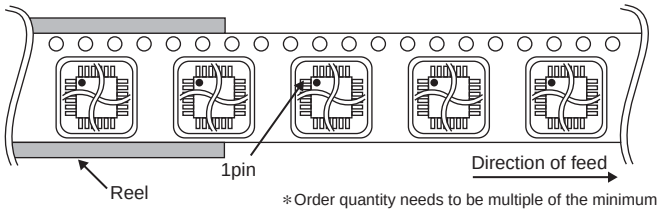
Packaging and forming specification
E2: Embossed tape and reel

TQFP64V



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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