CXPI Transceiver for Automotive BD41000AFJ-C/BD41001FJ-C/BD41003FJ-C

Frequently Asked Question (FAQ)

This application note is FAQ that CXPI transceiver (BD41000AFJ-C/BD41001FJ-C/BD41003FJ-C) is embedded in ECU. This FAQ describes general explanations. Please confirm that ECU satisfies all requirements after CXPI transceiver is embedded in ECU in refer to this application note. This FAQ mainly describes specifications required for external parts and software on microcontrollers. Thoroughly read the latest Datasheet(BD41000AFJ-C/BD41001FJ-C/BD41003FJ-C) additionally before CXPI transceiver is embedded. In this application note, CXPI transceiver is described by BD41000AFJ-C when the explanations are common in BD41000AFJ-C, BD41001FJ-C and BD41003FJ-C.

Q1. Recommended external circuit and part number of the BUS pin?

Conform to the designation about the external parts from OEM. When there is no designation, it is necessary to consider EMC performance in general. Figure 1 shows example of external circuit.

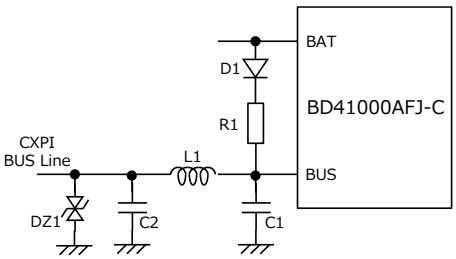

Figure 1. External circuit example of the BUS pin

D1 and R1 are necessary for master only. Both C1 and C2 are not necessary If ECU can satisfy EMC performance, it is allowed to use either C1 or C2.
Table 1 shows the purpose of each part, each part's minimum characteristic value according to CXPI standard and BD41000AFJ-C characteristic, and part number (reference).

Table 1. Purpose of Each Part, Minimum Characteristic Value, Part Number (reference)

Parts	Purpose	Minimum characteristic value	Part Number (reference)
D1	Prevention of reverse current	V_Z=0.4V to 1.0V	RR268MM-600TF(ROHM)
R1	Pullup resistance	0.9kΩ to 1.1kΩ	-
C1, C2	EMI measures EMS measures	to 250pF (Total) (Limitation for slave only)	-
L1	EMI measures	-	BLM21AG601S(Murata)
DZ1	ESD measures	V_Z=±18V to ±24V	UDZVFH18B(ROHM)

Pay attention that the EMS performance may worsen if the voltage of the DZ1 value is too low. For C1 and C2, decide the value after confirmation for OEM requirements because there is the capacity constraint as the whole CXPI system.

Q2. The limitation of the external resistance value of the MS pin?

The MS pin has to set "H" (for master) and "L" (for slave) as follows Figure 2. The MS pin threshold voltage is described in the Datasheet.

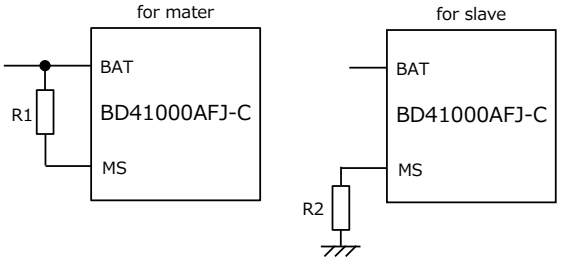

Figure 2. External circuit example of the MS pin

The purposes to insert R1 and R2 in the MS pin are follows;

1. Countermeasure of adjacent pin (BAT and MS) short
   (The risk is higher for slave than master)
2. Countermeasure of EMS

The resistances of R1 and R2 have no constraint if it has no problem for above 1 and 2. Decide the value that it does not have any problem for ECU evaluation.
Power off mode circuit current (dark current) affected

the battery life is 3μA(typ.) described in Datasheet when using any value on R1 and R2 even if for slave.

Q3. The limitation of the external resistance value of the RXD pin?

Because the RXD pin is an open drain output, it has to pullup for MCU interface supply as follows Figure 3.

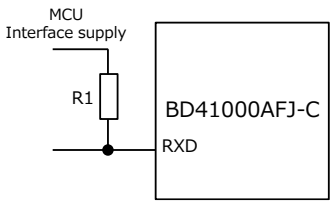

Figure 3. External circuit example of the RXD pin

For R1, decide to the resistance value in consideration of following 1 and 2.

1. Set to the resistance value or over by following expression for it does not exceed EM (electro migration) allowable current.
   R1 resistance(Ω) > MCU interface supply(V) / 4(mA)
2. Set to the resistance value or less that is has enough margin of slew rate against baud rate in consideration of the board capacity and pin capacity.

Q4. The limitation of the external capacitance value of the BAT pin?

If EMC performance does not have any problem, there is no constraint. 100nF or over is strongly recommended.

Q5. The processing required on the microcomputer side for arbitration function?

Arbitration function is realized by the following function allotment on the microcomputer side and the transceiver side.

Microcomputer side : Arbitration of the byte unit between the UART frame

Transceiver side : Arbitration of the bit unit in the UART frame

Transmit delay occurs with transceiver as described in BD41000AFJ-C Datasheet. Implement the following two functions on microcomputer side to operate arbitration function correctly.

1. Before transmitting check if UART receiving
2. After transmitting check if the received data is as same as transmitted data.

Figure 4 shows basic flowchart example on microcomputer side when frame transmitting.

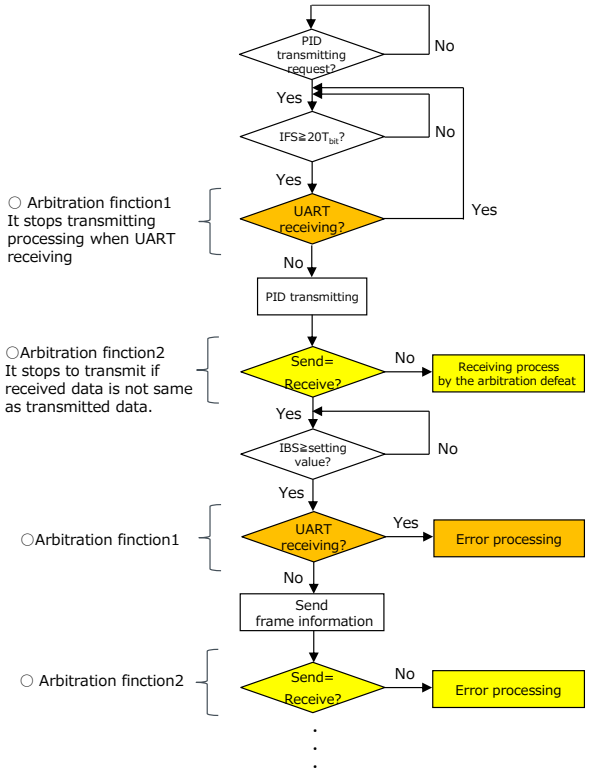

Figure 4. Flowchart example on microcomputer side when frame transmitting

There are 2 methods to check whether UART receiving

1. Using the UART peripheral status function of the microcomputer
2. Using the general-purpose IO interrupt function of the microcomputer

Please choose methods in consideration of the using microcomputer specification. When use method 2, confirm that the ECU satisfies all requirements in consideration of noise.

Q6. The processing required on the microcomputer side for wakeup detection function?

Wakeup detection function is realized by the following function allotment on the microcomputer side and the transceiver side.

○ For master
Microcomputer side : no function

Transceiver side : Judge that wakeup pulse detection

○ For slave

Microcomputer side : Judge that second dominant.
Judge that first dominant is invalid.

Transceiver side : Judge that first dominant.
Notify that dominant since the second.

As described in BD41000AFJ-C Datasheet, transceiver toggles RXD output signal when detecting the rising edge from dominant to recessive after valid dominant width.

Figure 5 shows the basic flowchart example for operates wakeup detection function correctly for slave. Figure 6 and Figure 7 show the state transition examples for BUS wave and RXD output signal on microcomputer side.

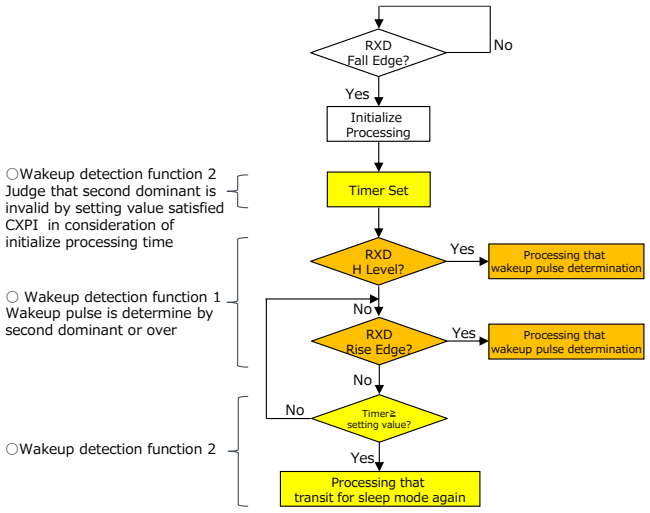

Figure 5. Basic flowchart example of wakeup detection on microcomputer side for slave

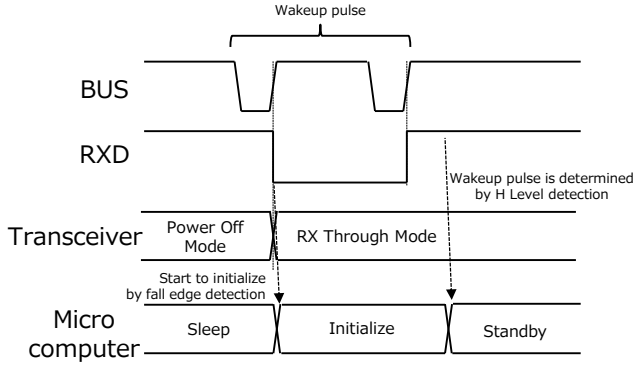

Figure 6. State transition examples in case that initialization is completed after second dominant

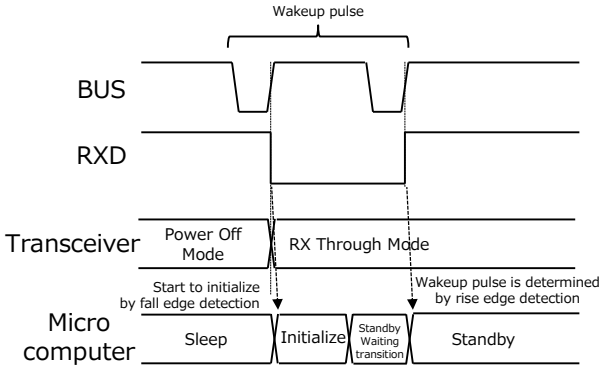

Figure 7. State transition example in case that initialization is completed before second dominant

In case that microcomputer wakeup by BUS clock from master, microcomputer wakeup after third dominant detection over than wakeup determination timing depends on the initialization time for microcomputer. Microcomputer can not judge that wakeup because RXD is “L” when initialization is completed just after receiving odd dominant. However microcomputer can judge that wakeup by detecting RXD rise edge from next even dominant.

Figure 8 shows state transition example on microcomputer side for invalidating first dominant detection when first dominant occurs only. Please refer to Q7 for the time to control the NSLP pin.

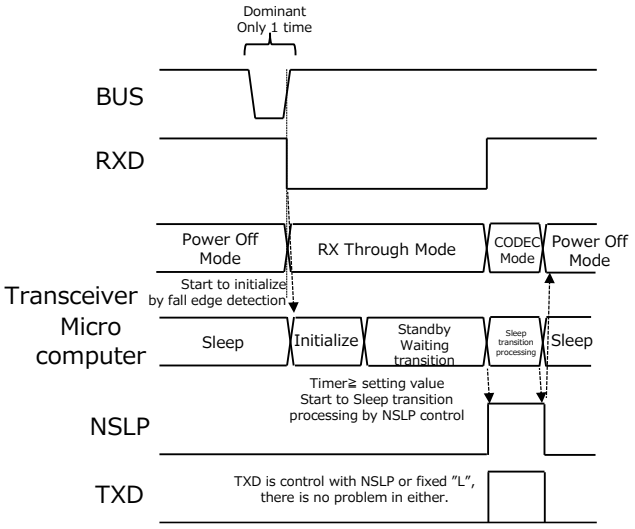

Figure 8. State transition example in case that

first dominant occurs only

CXPI standard prescribe that the time to determine the first invalid dominant is Max 60msec from BUS fall edge. Set the appropriate timer value to satisfy within 60msec in consideration of the maximum dominant width 2.5msec that is prescribed CXPI standard and the processing time shown in Figure5 including the initialization. Be careful that ECU can not satisfy the wakeup specification of CXPI standard if using microcomputer that can not complete initialization within 60msec.
It shows a timer setting example with the microcomputer initialization time as follows.
(Example 1) Initialize time: 40 to 50msec :

Timer setting value < 7.5msec

(Example 2) Initialize time: 5 to 10msec :

10msec < Timer setting value < 47.5msec

Q7. The necessary state transition waiting time when controlling NSLP terminal ?

NSLP pin has the low pass filter function (time constant 5μsec (Max)) for the purpose of the noise reduction. In addition, 15μsec (Max) is necessary for waiting stable state transition of the internal circuit.

Thus, fix to input level into NSLP pin at time more than at least 20μsec to change the state surely.

Q8. What happen if he TXD pin is changed “H” after the NSLP pin changed “H”

In the CODEC Mode, transceiver transmits data to BUS after detecting the fall edge of the TXD pin.
Thus, transmitter does not transmit abnormal data to BUS if the TXD pin is changed “H” after the NSLP pin changed “H” because fall edge does not occur.
But be careful that there is possibility to change to a Through Mode without expecting if TXD pin is changed “H” more than 30μsec before NSLP pin is changed “H”.

Q9. How to use clock output from the CLK pin on microcomputer side for slave?

It is not necessary to use the clock output on the microcomputer side and can realize CSMA/CR of the CXPI standard by using the timer of the microcomputer. For example, use the clock when you want to constitute the following system.

1. There is the application operated correctly by master baud rate cycle
2. Baud rate clock from the CLK pin can be used in place of the oscillation of the microcomputer

When it does not use the CLK pin, there is no problem that the pin is opened as described in BD41000AFJ-C Datasheet.

Q10. The processing for slave to receive wakeup pulse by the another slave node trigger?

Figure9 and Figure10 show the processing for slave to wakeup by the another slave node.

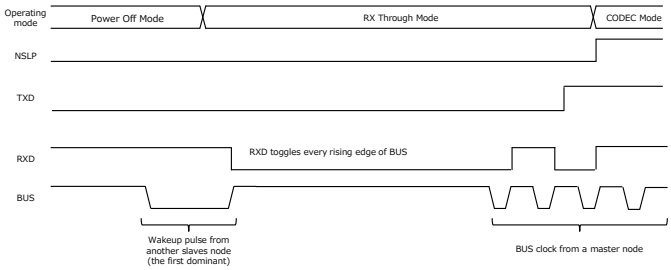

Figure 9. Transition example when BUS clock was output by a master node after the first dominant output from another slave node

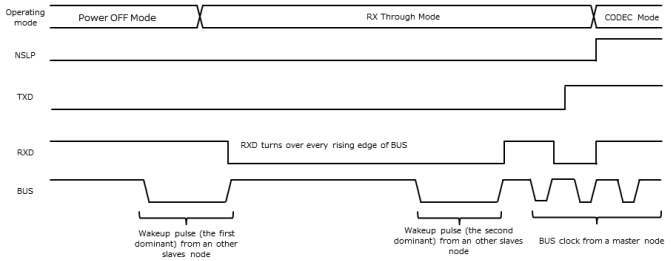

Figure 10. Transition example when another slave output the second dominant

As for the slave node to receive Wakeup pulse from another slave node, change the state on the microcomputer side described in Q6.

Q11. The processing that is required for software on the microcomputer side as failsafe processing?

Reset CXPI transceiver as far as microcomputer do not violate OEM requirements if microcomputer detect the following abnormal conditions.

Obey the designation about the fail-safe processing from OEM.

○ Abnormal detective example on the microcomputer side.

1. Physical bus error
   (more than prescribed time, no PTYPE, PID reception)
2. Transmission error 1
   (error counter becomes than the prescribed value)
3. Transmission error 2
   (more than prescribed time, no transmit)
4. Time-out error
   (more than prescribed time, no receive specific PID)

When resetting CXPI transceiver, fix NSLP pin to "L" at time more than at least 20µsec shown in Q7.

Q12. The POR release time after the power supply (BAT) injection?

The release time of POR is 15µsec(Max) from the timing when the wakeup condition (NSLP=H or BUS terminal Wakeup pulse detective or TXD terminal Wakeup detection) occur.

POR circuit does not work during Power Off Mode because internal power is off. Thus, POR circuit does not work starting from power supply (BAT) injection.

Q13. Why the RXD sometimes output fixed “L” when the power supply (BAT) stands up quickly?

When BUS load (time constant) is large, BUS rising voltage rate is late against the rising voltage rate of power supply (BAT).
Because Wakeup pulse detection LO time for slave is short with 0.5μs to 5μs, a delay time with the BUS rising voltage rate is recognized to be Wakeup pulse, and it may change in RX Through Mode at power supply (BAT) injection.
Show the state transition example in Figure11.

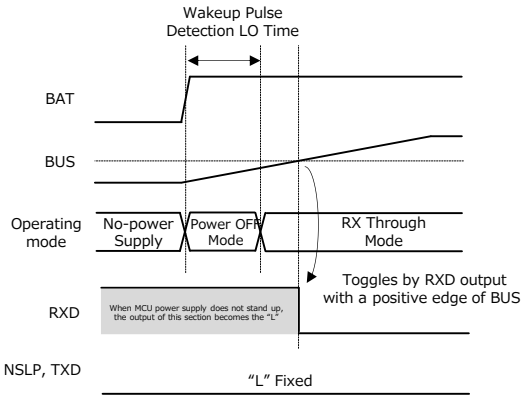

Figure 11. State transition example when power supply (BAT) stands up quickly and BUS load (time constant) is large

Control the NSLP pin and change to the appropriate mode if the RXD pin output is “L” after power supply (BAT) injection because there is the possibility to change in RX Through Mode. Refer to Q7 for the time to control the NSLP pin.

Q14. What is the warning point of the interval of TXD transmit after arbitration defeat?

In Datasheet, it is described that it is necessary to have the interval 1Tbit(BUS baud rate period) or more to transmit again after arbitration defeat.

There is no specific warning point when own node transmit response data for transmitted own node PID because CXPI transceiver have a delay and microcomputer operate arbitration function as Figure12.

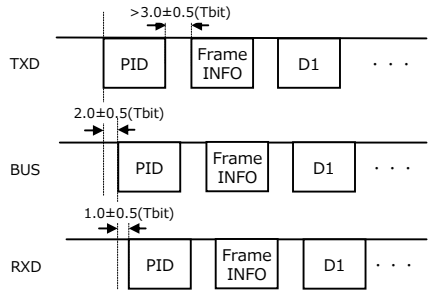

Figure 12. When own node transmits PID and response

On the other hand, it is necessary to set TXD transmit interval carefully enough in consideration of arbitration defeat occurring when own node transmits response data to transmitted another node’s PID for own node as Figure13.

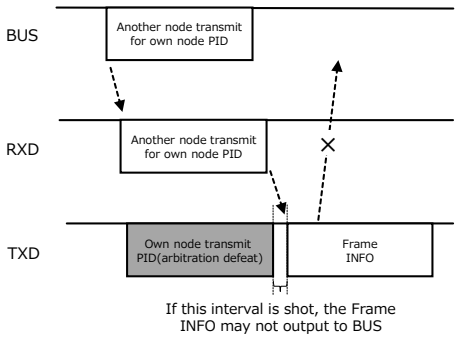

Figure 13. When own node transmit response data for transmitted another node’s PID

As Figure13, arbitration defeat occur when microcomputer transmit PID just before receiving own node PID.
After that, transceiver may not output the frame information to BUS because the TXD interval is too short when own node transmits response data for transmitted another node’s PID.

To avoid error described in Figure13, software should set the wait time of TXD transmit interval in consideration of the most late time that microcomputer start to transmit arbitration defeat PID(including the hardware delay, software delay etc.), the baud rate frequency deviation in microcomputer, the baud rate frequency deviation on BUS, jitter, the deviation(0.005Tbit) when transceiver take the signal to internal.
Large wait time may be necessary as following two considerations.

○The most late timing that microcomputer start to transmit arbitration defeat PID

As Figure14, some microcomputer may not transmit data to TXD pin just after software operate UART transmit order. Software need to set wait time in consideration of the following delay time when software judge if microcomputer can transmit or not by checking UART receiving.

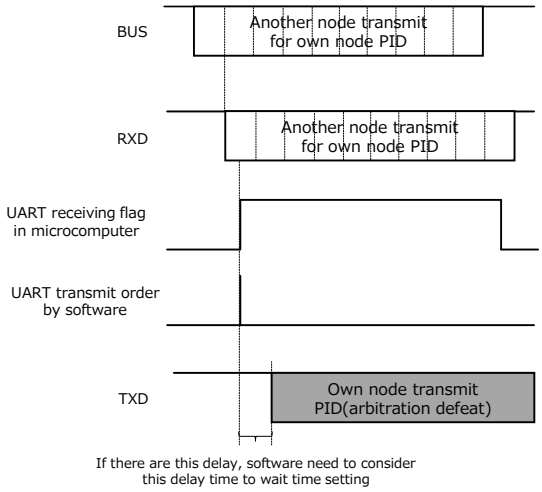

Figure 14. Delay time example from UART transmission order to the TXD pin output

○Deviation of the baud rate in microcomputer side and BUS side

Calculation example of the wait time is shown in Figure15,16 in consideration of baud rate frequency deviation.
In addition, Figure15 shows an example when calculate wait time by RXD Stopbit base and Figure16 shows by TXD Stopbit base.
In Figure15, 16, TXD is shown as the same timing with RXD, BUS, but if the most late timing described above is not same as Figure15, 16, calculate the wait time after considering the TXD timing.

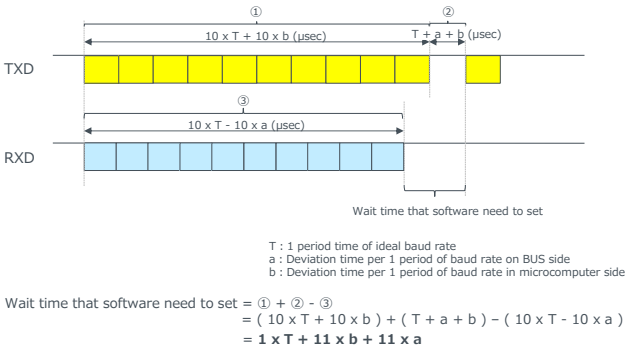

Figure 15. Calculation example of the WAIT time in consideration of a baud rate deviation (wait by RXD Stopbit base)

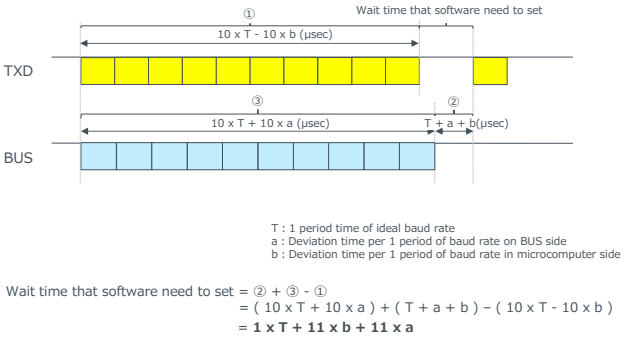

Figure 16. Calculation example of the WAIT time in consideration of a baud rate deviation (wait by TXD Stopbit base)

Set the wait time with margin in consideration of jitter and hardware delay time in addition to described Figure14,15,16 and check if error does not occur at BUS high communication rate test (arbitration happens frequently).

In addition, check if CXPI Standard of IBS≦9Tibt can be satisfied when long application soft operating time is need between PID receiving and response transmitting.

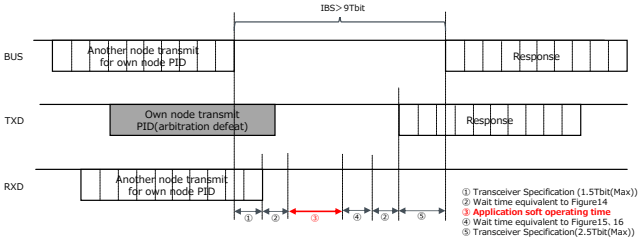

Figure 17. The example which cannot satisfy CXPI standard of IBS <= 9Tbit

Q15. What is the difference between BD41001FJ-C and BD41003FJ-C?

The behavior of the wakeup sequence from sleep mode by BUS terminal or TXD terminalis is partially different between BD41001FJ-C and BD41003FJ-C.
(About the behavior described in Q15, BD41000AFJ-C has same behavior as BD4100AFJ-C.)

Figure18,19 show the difference of the behavior when normal Wakeup pulse is applied to BUS terminal.

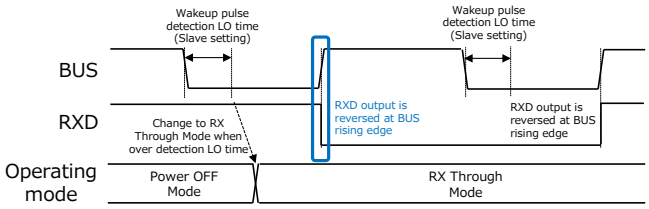

Figure 18. The behavior when the normal Wakeup pulse is applied (BD41001FJ-C)

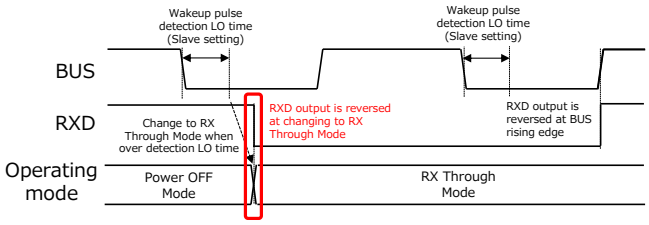

Figure 19. The behavior when the normal Wakeup pulse is applied (BD41003FJ-C)

Next, Figure20,21 show the difference of the behavior when the specific signal like noise(short Dominant signal(1.2μs～3.5μs(typ))) is applied to BUS terminal.
When the specific signal is applied, BD41001FJ-C may change to RX through mode without reversal of RXD output. Therefore microcomputer fail-safe software processing with controlling NSLP terminal is necessary.
BD41003FJ-C should output reversal signal from RXD terminal when BD41003FJ-C change to RX through mode. Therefore microcomputer fail-safe software processing can implement by RXD signal for noise measure.

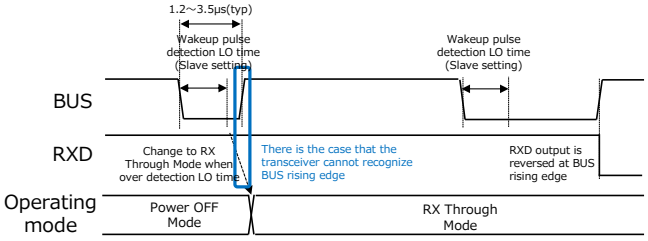

Figure 20. The behavior when the special signal like noise is applied (BD41001FJ-C)

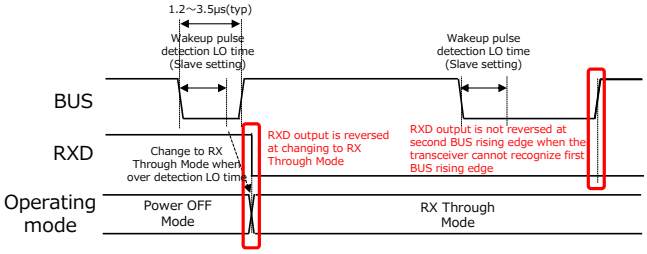

Figure 21. The behavior when the special signal like noise is applied (BD41003FJ-C)

In addition, it is supposed that following noise cannot occur usually but Figure22,23 show the difference of the behavior when the specific signal(90μs～90.2μs(typ)) is applied to TXD terminal.

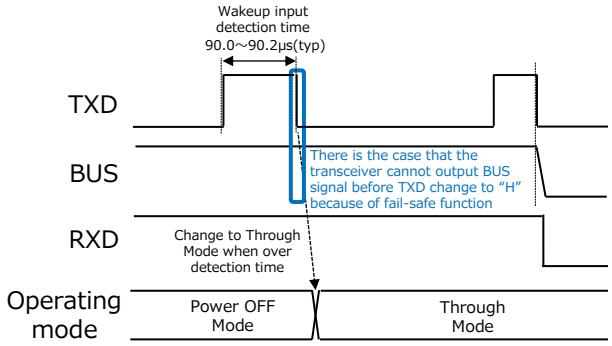

Figure 22. The behavior when the special signal like noise is applied (BD41001FJ-C)

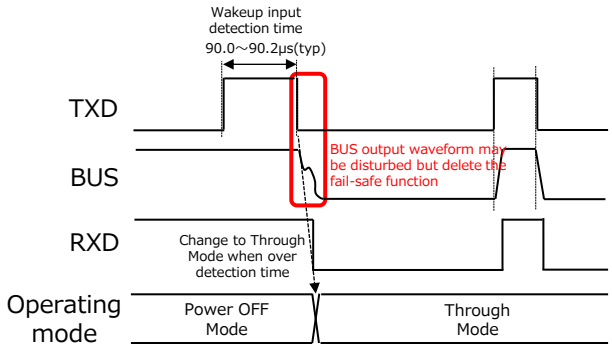

Figure 23. The behavior when the special signal like noise is applied (BD41003FJ-C)

List of reference of Datasheet for each QA

QA No	Datasheet chapter title
1	Block Diagram, Application Example
2	Block Diagram, Application Example
3	Block Diagram, Application Example
4	Block Diagram, Application Example
5	Arbitration Function
6	Sequence Diagram
7	Sequence Diagram
8	Sequence Diagram
9	Sequence Diagram
10	Sequence Diagram
11	Sequence Diagram
12	Fail-safe Mode
13	Sequence Diagram
14	Arbitration Function
15	State Transition Diagram

Revision history

Date	Rev.	Changes
Mar.2019	005	New Release
Seq.2021	006	Added BD41003FJ-C Added Q15

Notes

1) The information contained herein is subject to change without notice.

2) Before you use our Products, please contact our sales representative and verify the latest specifications :

3) Although ROHM is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors.
Therefore, in order to prevent personal injury or fire arising from failure, please take safety measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. ROHM shall have no responsibility for any damages arising out of the use of our Poducts beyond the rating specified by ROHM.

4) Examples of application circuits, circuit constants and any other information contained herein are provided only to illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

5) The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM or any other parties. ROHM shall have no responsibility whatsoever for any dispute arising out of the use of such technical information.

6) The Products specified in this document are not designed to be radiation tolerant.

7) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a ROHM representative : transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.

8) Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters.

9) ROHM shall have no responsibility for any damages or injury arising from non-compliance with the recommended usage conditions and specifications contained herein.

10) ROHM has used reasonable care to ensure the accuracy of the information contained in this document. However, ROHM does not warrants that such information is error-free, and ROHM shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.

11) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. For more details, including RoHS compatibility, please contact a ROHM sales office. ROHM shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

12) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.

13) This document, in part or in whole, may not be reprinted or reproduced without prior consent of ROHM.

ROHM SEMICONDUCTOR

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/