ROHM Automotive Solutions

2 Channel Half-Bridge Gate Driver Setup Guide

BD16951EFV-M

●Description

The BD16951EFV-M is an AEC-Q100 automotive qualified 2-channel Half-Bridge Gate-Driver, which can be controlled by an external MCU through a 16-bit Serial Peripheral Interface (SPI). Independent control of low- and high-side N-Ch. MOSFETS allows for several MCU controlled modes. A programmable drive current is available to adjust slew-rates, in order to meet EMI and power dissipation requirements. Diagnostics can be read and reset by an external MCU.

●Features

1) AEC-Q100 Qualified (Note1)
2) 2ch Half-Bridge Gate Drivers
3) 4 external MOSFETs are Controlled Independently
4) Half-Bridge Control Modes are selected by SPI
5) Slew Rates are controlled with Constant Source/Sink Current
6) 500 kHz Oscillation for Charge Pump
7) 16bit SPI

(Note1) Grade1

●Applications

Power Window Lifter, Sun Roof Module,
Wiper, Seat Belt Tensioner, Seat Positioning.

Symbol	Part
TGH1, TGH2, TGL1, TGL2	N-Channel MOSFET
C_{VS}	1.0µF, ±10%
C_{VCC}	0.1µF, ±10%
C_{CP1}	0.1µF, ±10%
C_{CP2}	0.1µF, ±10%

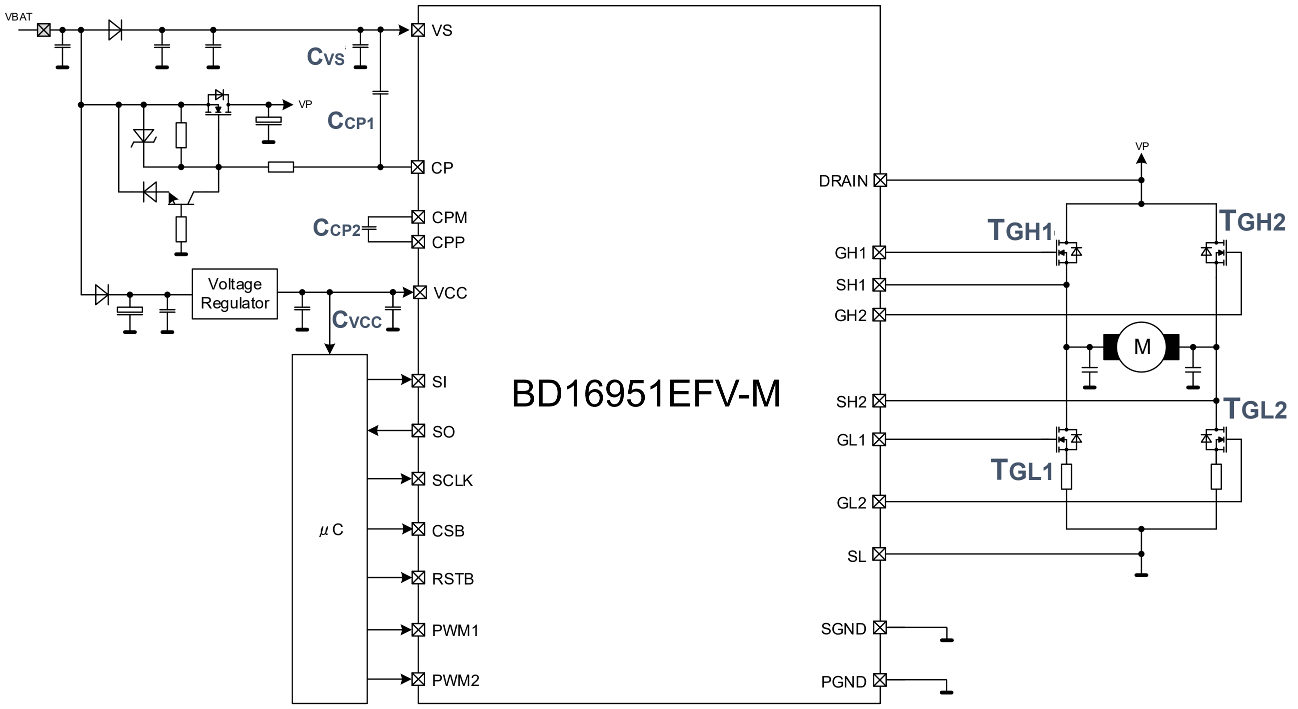


Fig.1 Typical Application Circuit

●Hardware Peripherals

Input Capacitor CVS

The input capacitor (CVS) lowers the power supply impedance and averages the input current. The CVS value is selected according to the impedance of the power supply that is used. A ceramic capacitor with a small equivalent series resistance (ESR) should be used. Although the capacitance requirement varies according to the impedance of the power supply that is used, as well as the load current value, it is generally in the range of 1.0μF.

This document relates to frequently used high speed MOSFET gate driver applications in a clamped inductive switching environment.

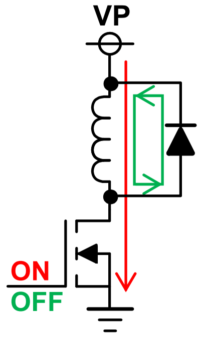


Fig.2 Simplified Circuit

Input Capacitor CVCC

The input capacitor (CVCC) lowers the power supply impedance and averages the input current. The CVCC value is selected according to the impedance of the power supply that is used. A ceramic capacitor with a small equivalent series resistance (ESR) should be used. A capacitor value of 0.1μF is recommended.

Charge Pump Capacitor CCP1

The Charge pump capacitor CCP1 is required for smoothing the ripple voltage. A capacitor value of 0.1μF is recommended. Using a capacitor with a capacitance lower than 0.1μF, results in a larger ripple voltage. Conversely, using a capacitor with a capacitance greater than 0.1μF results in a larger rush current during start-up, but ripple voltage becomes lower.

Charge Pump Capacitor CCP2

The charge pump capacitor CCP2 is required for charging up the voltage. A capacitor value of 0.1μF is recommended. Using a capacitor with a capacitance lower than 0.1μF, results in a larger ripple voltage. Conversely, using a capacitor with a capacitance greater than 0.1μF results in a larger rush current during start-up, but ripple voltage becomes lower.

External N-ch MOSFET

The BD16951EFV-M is the gate driver for high side and low side N-channel MOSFETs. Select MOSFETs with the required current capability to drive the motor and a Gate-Source breakdown voltage ≥ 12V.

●External MOSFET Parameter

The BD16951EFV-M is a gate driver for high side and low side N-Channel MOSFETs. Select the FET with the required current capacity (IDS, plus some headroom) to drive the motor and with a Gate-Source pressure voltage of more than VBAT. The relevant parameters for setting up the gate-driver are shown below:

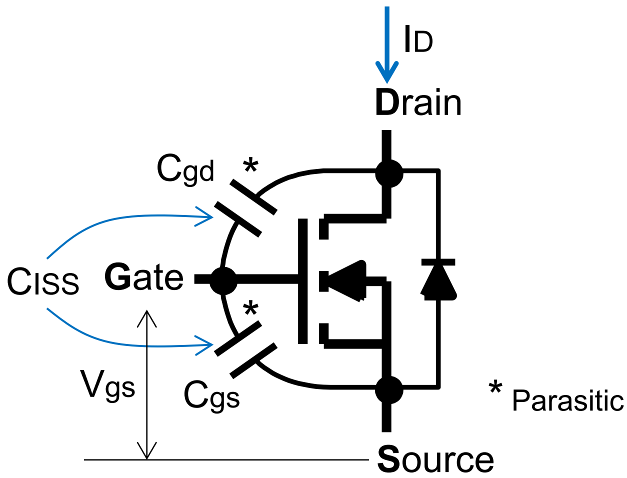


Fig.3: N-Channel MOSFET

CISS: the transistor input capacitance is a combination of the parasitc gate-to-source (Cgs) and gate-to-drain (Cgd) capacitance.
Qgd: Gate-drain charge.
gfs: Forward transconductance.
Vgs: Gate-source voltage ≥ 12V.
Vgs(th): Gate-source threshold voltage.
Vgp or Vgs(Miller): Miller plateau voltage
IDS: Continuous drain-to-source current.

●Register Map

Description	MSB	Address	Data bit							LSB	Default Value
	15	14-8	7	6	5	4	3	2	1	0	7-0
Software POR	W	Addr. 0 (000_0000)	1	1	0	1	0	1	1	1	NA
Enable Register	R/W	Addr. 1 (000_0001)	x	x	x	x	x	EN	CPEN	DRVEN	0000_0000
Mode Setting Ch2. Ch1	R/W	Addr. 2 (000_0010)	CH2_ MODE [3]	CH2_ MODE [2]	CH2_ MODE [1]	CH2_ MODE [0]	CH1_ MODE [3]	CH1_ MODE [2]	CH1_ MODE [1]	CH1_ MODE [0]	0000_0000
Protection Mode Setting	R/W	Addr. 3 (000_0011)	OCPLA_ H2	OCPLA_ L2	OCPLA_H1	OCPLA_L1	UVLOLA	OVPLA	UVLOM	OVPM	1111_1100
Half-Bridge Motor Op. Setting1	R/W	Addr. 4 (000_0100)	x	x	x	CUR_ SOURCE[4]	CUR_ SOURCE[3]	CUR_ SOURCE[2]	CUR_ SOURCE[1]	CUR_ SOURCE[0]	0001_1111
Half-Bridge Motor Op. Setting2	R/W	Addr. 5 (000_0101)	x	x	x	CUR_ SINK[4]	CUR_ SINK[3]	CUR_ SINK[2]	CUR_ SINK[1]	CUR_ SINK[0]	0001_1111
Half-Bridge Motor Op. Setting3	R/W	Addr. 6 (000_0110)	x	x	CCPT[5]	CCPT[4]	CCPT[3]	CCPT[2]	CCPT[1]	CCPT[0]	0011_1111
OCP Setting	R/W	Addr. 7 (000_0111)	x	x	OCPHD[2]	OCPHD[1]	OCPHD[0]	OCPLD[2]	OCPLD[1]	OCPLD[0]	0000_0000
OCP Filter Time Setting	R/W	Addr. 8 (000_1000)	x	x	OCP_ FILTER[5]	OCP_ FILTER[4]	OCP_ FILTER[3]	OCP_ FILTER[2]	OCP_ FILTER[1]	OCP_ FILTER[0]	0000_0000
Status Read/Clear Status	R/W	Addr. 9 (000_1001)	OCP_ HS1	OCP_ HS2	OCP_ LS1	OCP_ LS2	x	x	x	x	0000_0000

Bit #	[MSB] 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 [LSB]
	R/W	Address							Data Byte							

●Register Setting Overview

Address 0: software Power-On-Reset (POR): the only effective command here to be send is d7h which will set back all register (settings, error-bits and counter) to their default values [command string: 80h – d7h].

Address 1: separate chip-, charge pump- and gate driver-enable.

Address 2: separate working mode select for channel 1 and 2.

Address 3: protection mode select for gate (OCP/UVP) and VS voltage monitor.

Address 4/5: separate source and sink current settings.

Address 6: Cross current protection (CCPT).

Address 7: OCP threshold voltage setting.

Address 8: OCP filter time setting.

Address 9: Status Register for OCP. Read out and clear by writing 00h

●Gate Source- and Sink-Current

The controlled constant source- and sink-current values of the gate driver (GHx/GLx) can be set individually by setting up the relating SPI register. Setting ranges are: Drivers OFF' and 1mA - 31mA in steps of 1mA.

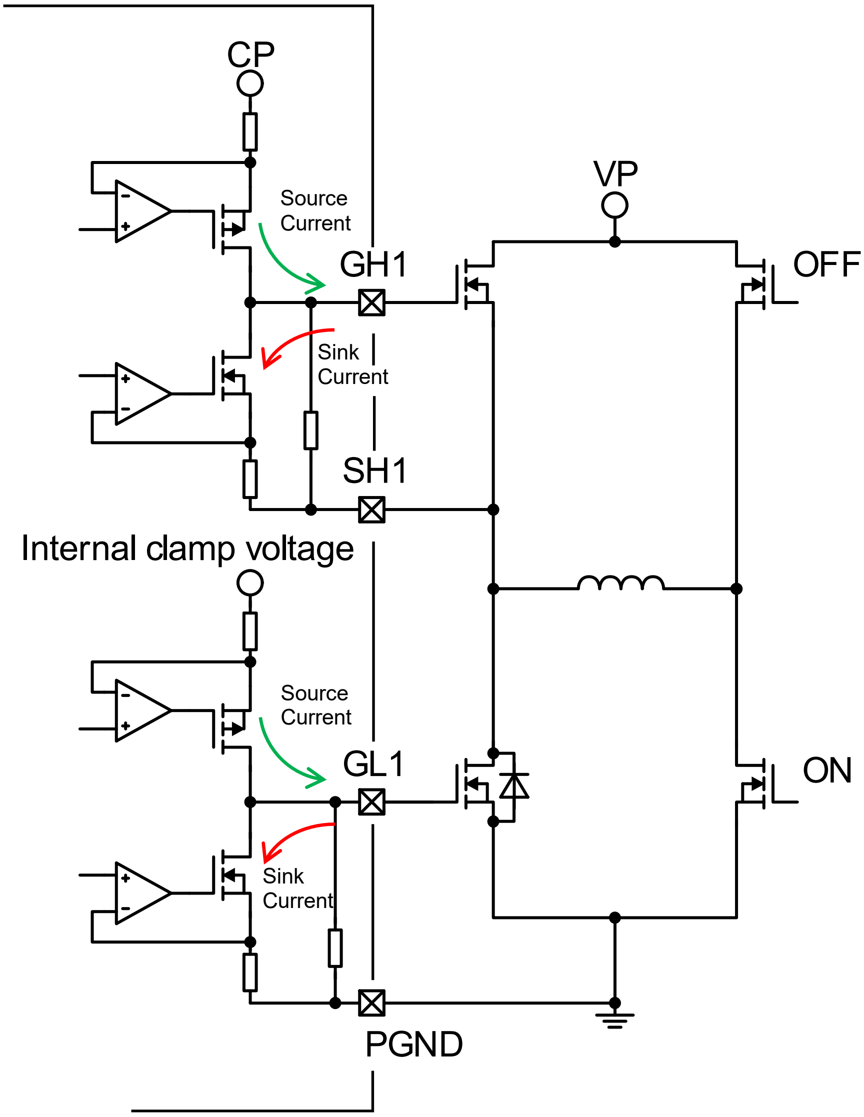


Fig.4: Gate Current in Mode 9

Cross Current Protection Time (CCPT)

It is essential that both drivers of one half-bridge aren't conductive at the same time. This will result in a high short-circuit current, also known as cross-current. Therefor the both half-bridges can be protected against cross-current with the help of an internal adjustable delay counter. Please be aware that wrong settings might make the protection ineffective and damage the hardware! The cross-current protection delay only is effective in mode 9 (Half-Bridge control mode).

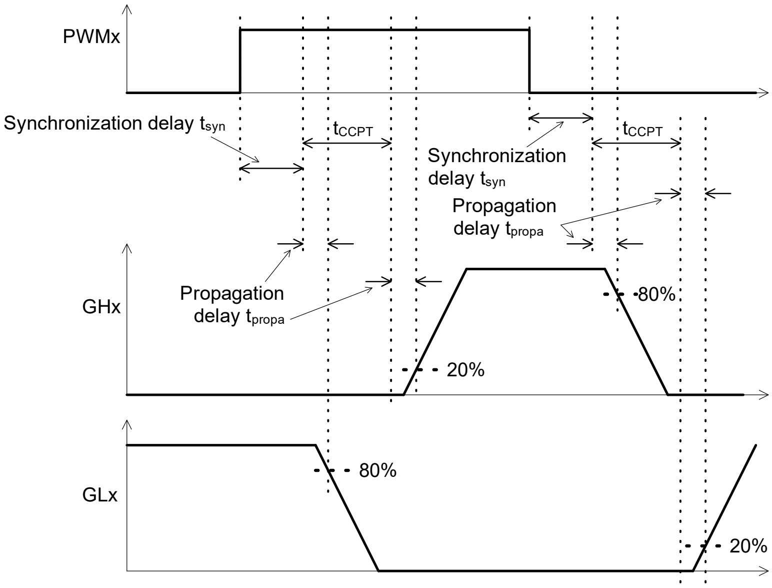


Fig.5: Half-Bridge Control Mode 9 - Active Free Wheeling

In mode 9 an external supplied PWM signal is controlling the GHx and GLx outputs. The control signal always will be delayed a bit caused by a fixed internal propagation time (tpropa) and a slightly fluctuating synchronization time (tsyn). The charge-pump circuit is clocked by the internal timer resulting in PWM- and charge pump-clock aren't synchronized. It will take 3 clocks to synchronize plus/minus some synchronization jitter. To prevent cross current in the half-bridge it is necessary to add an additional delay time (tCCPT). Cross-current protection is defined in the source current start of GH1/GH2 from the sink current start of GL1/GL2. This cross current protection time setting value can be set by the SPI register.

Find out the Cross-Current Protection Time Setting (CCPT)

$$t_{CCPT(min.)} \geq \frac{V_{DS} * C_{ISS}}{I_{SINK} * 0.75}$$

Example:
VDS:---------------------------------12V
CISS:--------------------------------950pF*(max value)
I_{sink}:---------------------------------- 30mA

*taken from MOSFET datasheet

$$t_{CCPT(min.)} \geq \frac{12V * 950pF}{30mA * 0.75}$$

$$t_{CCPT(min.)} \geq 0.51\mu s$$

tCCPT(min) ≥ Min value from the list below. Set the associating typ. value.

tCCPT(min) = 0.51µs => Min. value from list is 0.56µs =>

Setting value is ≥ **0.75 µs**.

Min	Typ	Max	unit	Tolerance
0.19	0.25	0.31	µs	±25%
0.38	0.50	0.63	µs	±25%
0.56	0.75	0.94	µs	±25%
0.75	1.00	1.25	µs	±25%
0.94	1.25	1.56	µs	±25%
1.13	1.50	1.88	µs	±25%
1.31	1.75	2.19	µs	±25%
1.50	2.00	2.50	µs	±25%
1.69	2.25	2.81	µs	±25%
1.88	2.50	3.13	µs	±25%
2.06	2.75	3.44	µs	±25%
2.25	3.00	3.75	µs	±25%
2.44	3.25	4.06	µs	±25%
2.63	3.50	4.38	µs	±25%
2.81	3.75	4.69	µs	±25%
3.00	4.00	5.00	µs	±25%
3.75	5.00	6.25	µs	±25%
4.50	6.00	7.50	µs	±25%
5.25	7.00	8.75	µs	±25%
6.00	8.00	10.00	µs	±25%
6.75	9.00	11.25	µs	±25%
7.50	10.00	12.50	µs	±25%
8.25	11.00	13.75	µs	±25%
9.00	12.00	15.00	µs	±25%
10.50	14.00	17.50	µs	±25%
12.00	16.00	20.00	µs	±25%
13.50	18.00	22.50	µs	±25%
15.00	20.00	25.00	µs	±25%
16.50	22.00	27.50	µs	±25%
18.00	24.00	30.00	µs	±25%
19.50	26.00	32.50	µs	±25%
21.00	28.00	35.00	µs	±25%

Min	Typ	Max	unit	Tolerance
22.50	30.00	37.50	µs	±25%
24.00	32.00	40.00	µs	±25%
25.50	34.00	42.50	µs	±25%
27.00	36.00	45.00	µs	±25%
28.50	38.00	47.50	µs	±25%
30.00	40.00	50.00	µs	±25%
31.50	42.00	52.50	µs	±25%
33.00	44.00	55.00	µs	±25%
34.50	46.00	57.50	µs	±25%
36.00	48.00	60.00	µs	±25%
37.50	50.00	62.50	µs	±25%
39.00	52.00	65.00	µs	±25%
40.50	54.00	67.50	µs	±25%
42.00	56.00	70.00	µs	±25%
43.50	58.00	72.50	µs	±25%
45.00	60.00	75.00	µs	±25%
46.50	62.00	77.50	µs	±25%
48.00	64.00	80.00	µs	±25%
49.50	66.00	82.50	µs	±25%
51.00	68.00	85.00	µs	±25%
52.50	70.00	87.50	µs	±25%
54.00	72.00	90.00	µs	±25%
55.50	74.00	92.50	µs	±25%
57.00	76.00	95.00	µs	±25%
58.50	78.00	97.50	µs	±25%
60.00	80.00	100.00	µs	±25%
61.50	82.00	102.50	µs	±25%
63.00	84.00	105.00	µs	±25%
64.50	86.00	107.50	µs	±25%
66.00	88.00	110.00	µs	±25%
67.50	90.00	112.50	µs	±25%
69.00	92.00	115.00	µs	±25%

Table 1: CCPT Time Settings

Over Current Protection (OCP)

To protect the external MOSFETS from overcurrent the BD16951EFV-M measures each drain-source voltage. The relevant transistor will be switched off as soon the drain-source voltage exceeds the OCP detection threshold setting value. The OCP detection threshold setting value can be set by editing the corresponding SPI register. Setting ranges are 200mV, 300mV, 400mV, 500mV, 750mV, 1000mV, 1250mV and 1500mV.

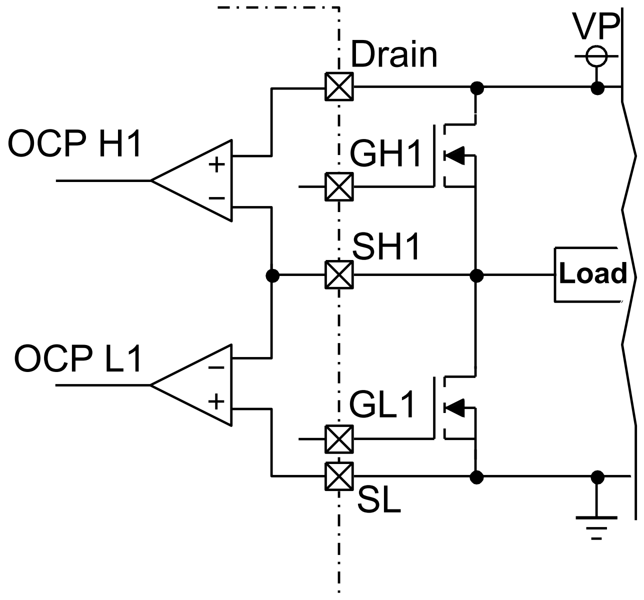


Fig.6: OCP on the Half-Bridge 1

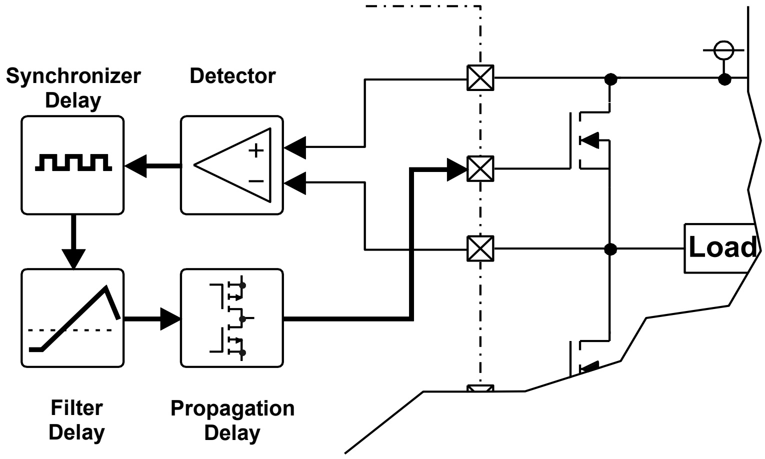


Fig.7: OCP on the Half-Bridge 1 - Delay Chain from Detection to Gate Driver Output

Total detection time = Synchronizer + Propagation + Filter Delay

Total detection time$_{(max)}$ = 1.25µs + 0.4µs + Filter Delay [1-64µs]

Total detection time$_{(max)}$ = 1.65µs + Filter Delay [1-64µs]

In order to prevent false OCP detection due to glitches or noise on the drain-source voltage of the external FET an OCP Filter is integrated. As soon the set OCP detection voltage is exceeded an adjustable filter time is awaited before the relevant transistor will be switched off. The filter time can be set in a range of 1μs to 64μs.
Note: each PWM high-to-low and low-to-high transition reset the OCP filter time counter.

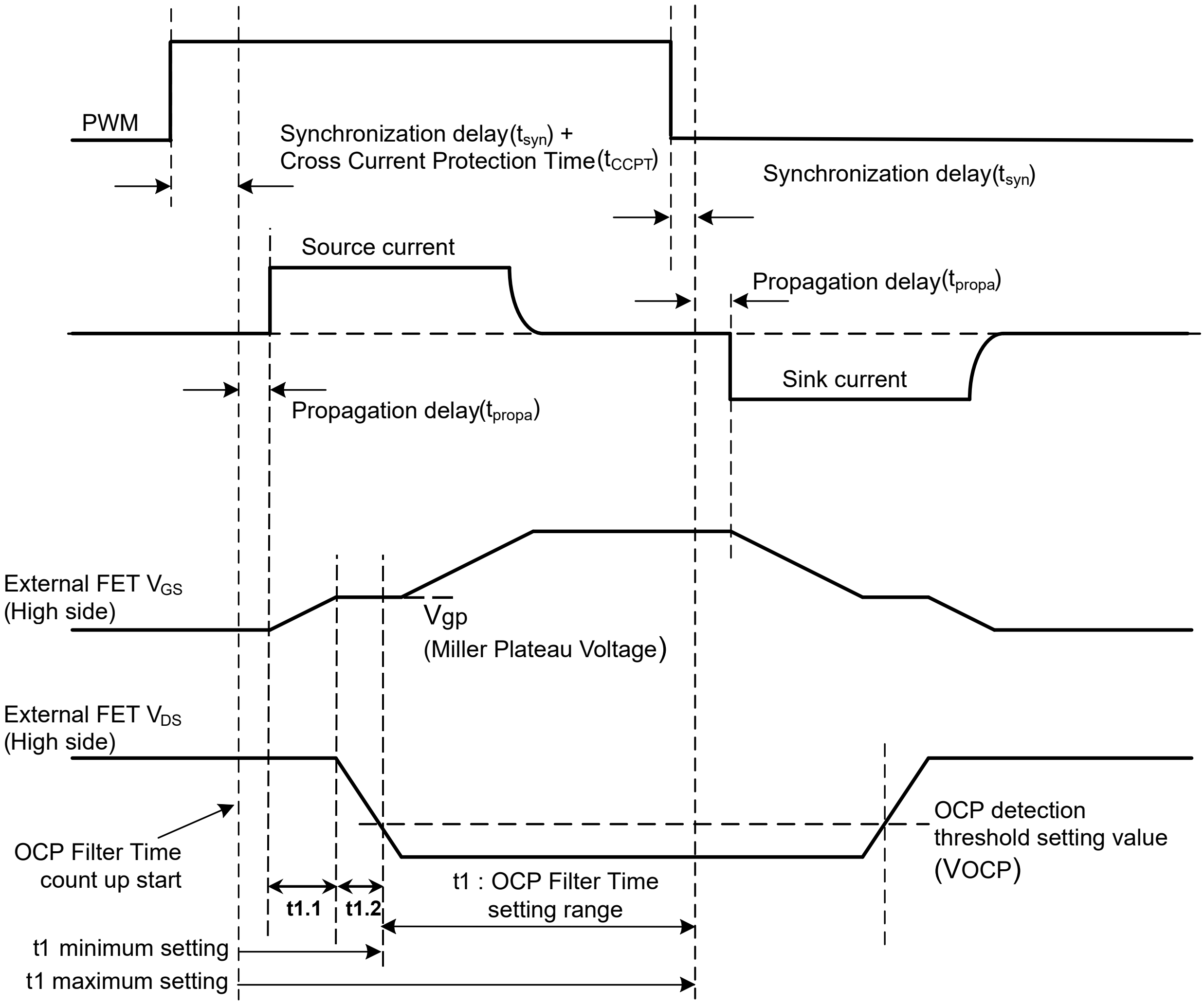


Fig.8: OCP Timing

OCP Filter Time min. setting

OCP Filter Time min. setting is set to prevent false OCP detection as following formula.
OCP Filter Time min. setting = t_{PROPA} + t1.1+ t1.2

OCP Filter Time max. setting

If OCP should be detected in minimum PWM duty cycle, the formula of OCP Filter Time max. setting is as below.
OCP Filter Time max. setting = “PWM Pulse Width(min.) – tccpt(max.)”

If OCP filter time is set higher than “PWM Pulse Width(min.) – tccpt(max.)”, OCP can’t be detected within this time. Then, external FET’s power dissipation should be checked with OCP condition and PWM Pulse Width.

Find out the OCP Filter Time Setting

OCP Filter Time min. setting = t_{propa}(max.) + t1.1(max.) + t1.2(max.)

$$t1.1(max.) = \left(V_{th} + \frac{I_{DS}}{g_{fs}}\right) * \frac{C_{ISS}}{I_{SOURCE} * 0.75}$$

$$t1.2(max.) = \frac{Q_{gd}}{V_{DS} - V_{th} + \frac{I_{DS}}{g_{fs}}} * \frac{V_{DS} - V_{th} + \frac{I_{DS}}{g_{fs}} - V_{OCP}}{I_{SOURCE} * 0.75}$$

OCP Filter Time max. setting = Pulse Width(min) – t_{CCPT}(max)

$$Pulse\ Width = \frac{Duty - Cycle}{PWM\ freq.}$$

Example:

- V_{th}:----------------------------------2.0V*(max value)
- C_{ISS}:--------------------------------- 950pF*(max value)
- t_{propa}:---------------------------------400ns (max value)
- t_{CCPT}:--------------------------------0.94µs (max value)
- PWM freq:------------------------- 20kHz
- Duty-Cycle:------------------------15% (min value)
- I_{DS} = VBAT/1Ω * 0.15:---------- 1.8A (on-duty)
- Q_{gd}:-------------------------4nC (max value)
- g_{fs}:-------------------------- 10S (min value)
- I_{source}:---------------------- 10mA
- V_{DS}:------------------------ 12V
- V_{OCP}:-----------------------200mV
- Load:-----------------------1Ω, 270µH

*taken from MOSFET datasheet

$$t1.1(max.) = \left(2V + \frac{1.8A}{10S}\right) * \frac{950pF}{10mA * 0.75}$$

$$t1.1 = 276.1ns$$

$$t1.2 = \frac{4nC}{12V - 2V + \frac{1.8A}{10S}} * \frac{12V - 2V + \frac{1.8A}{10S} - 0.2V}{10mA * 0.75}$$

$$t1.2 = 522.9ns$$

$$OCP\ Filter\ Time\ min. setting = t_{propa}(max.)\ +\ t1.1\ +\ t1.2$$
$$OCP\ Filter\ Time\ min. setting = 400ns\ +\ 276.1ns\ +\ 522.9ns$$
$$OCP\ Filter\ Time\ min. setting = 1.20\mu s$$

$$OCP\ Filter\ Time\ max. setting = Pulse\ Width(min.)\ -\ t_{CCPT(max.)}$$
$$OCP\ Filter\ Time\ max. setting = \frac{0.15}{20kHz}\ -\ 0.94\mu s$$

$$OCP\ Filter\ Time\ max. setting =\ 6.56\mu s$$

Example Conclusion

To program the typ. OCP filter time the tolerance range must be taken into consideration. In this example:
The min value must be ≥ 1.20µs, the max value must be ≤ 6.56µs. Therefor the possible filter time setting range which can be programmed is 2µs-5µs (typ).
If there will be an overlapping, e.g. the calculated max value is too low, the conditions must be changed. That might be done by decreasing the max. PWM frequency.

First min. entry higher than the calculated filter time min. value.

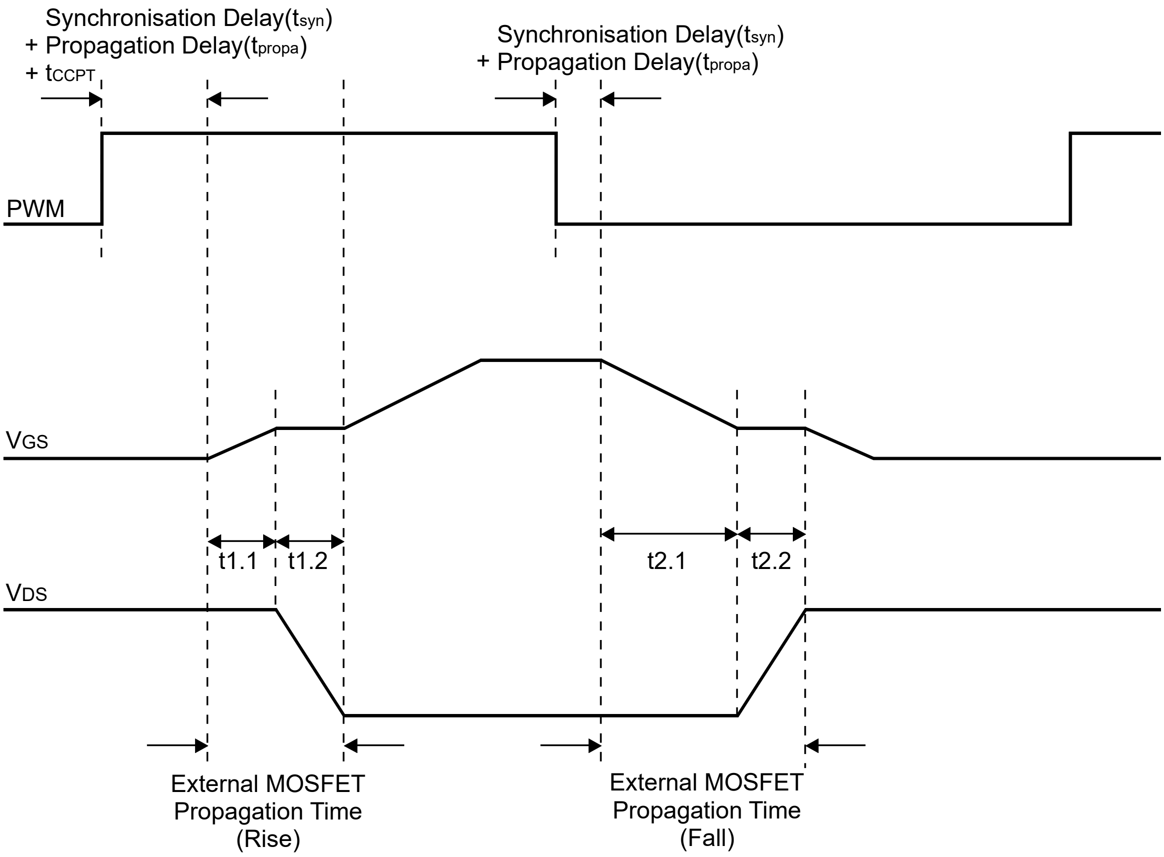
Corresponding max. value. Must be lower than the calculated filter time max. value.

Min	Typ	Max	unit	Tolerance
0.75	1.00	1.25	µs	±25%
1.50	2.00	2.50	µs	±25%
2.25	3.00	3.75	µs	±25%
3.00	4.00	5.00	µs	±25%
3.75	5.00	6.25	µs	±25%
4.50	6.00	7.50	µs	±25%
5.25	7.00	8.75	µs	±25%
6.00	8.00	10.00	µs	±25%
6.75	9.00	11.25	µs	±25%
7.50	10.00	12.50	µs	±25%
8.25	11.00	13.75	µs	±25%
9.00	12.00	15.00	µs	±25%
9.75	13.00	16.25	µs	±25%
10.50	14.00	17.50	µs	±25%
11.25	15.00	18.75	µs	±25%
12.00	16.00	20.00	µs	±25%
12.75	17.00	21.25	µs	±25%
13.50	18.00	22.50	µs	±25%
14.25	19.00	23.75	µs	±25%
15.00	20.00	25.00	µs	±25%
15.75	21.00	26.25	µs	±25%
16.50	22.00	27.50	µs	±25%
17.25	23.00	28.75	µs	±25%
18.00	24.00	30.00	µs	±25%
18.75	25.00	31.25	µs	±25%
19.50	26.00	32.50	µs	±25%
20.25	27.00	33.75	µs	±25%
21.00	28.00	35.00	µs	±25%
21.75	29.00	36.25	µs	±25%
22.50	30.00	37.50	µs	±25%
23.25	31.00	38.75	µs	±25%
24.00	32.00	40.00	µs	±25%

Min	Typ	Max	unit	Tolerance
24.75	33.00	41.25	µs	±25%
25.50	34.00	42.50	µs	±25%
26.25	35.00	43.75	µs	±25%
27.00	36.00	45.00	µs	±25%
27.75	37.00	46.25	µs	±25%
28.50	38.00	47.50	µs	±25%
29.25	39.00	48.75	µs	±25%
30.00	40.00	50.00	µs	±25%
30.75	41.00	51.25	µs	±25%
31.50	42.00	52.50	µs	±25%
32.25	43.00	53.75	µs	±25%
33.00	44.00	55.00	µs	±25%
33.75	45.00	56.25	µs	±25%
34.50	46.00	57.50	µs	±25%
35.25	47.00	58.75	µs	±25%
36.00	48.00	60.00	µs	±25%
36.75	49.00	61.25	µs	±25%
37.50	50.00	62.50	µs	±25%
38.25	51.00	63.75	µs	±25%
39.00	52.00	65.00	µs	±25%
39.75	53.00	66.25	µs	±25%
40.50	54.00	67.50	µs	±25%
41.25	55.00	68.75	µs	±25%
42.00	56.00	70.00	µs	±25%
42.75	57.00	71.25	µs	±25%
43.50	58.00	72.50	µs	±25%
44.25	59.00	73.75	µs	±25%
45.00	60.00	75.00	µs	±25%
45.75	61.00	76.25	µs	±25%
46.50	62.00	77.50	µs	±25%
47.25	63.00	78.75	µs	±25%
48.00	64.00	80.00	µs	±25%

Table 2: OCP Filter Time Settings

Find out the min. PWM ON-/OFF-Time



$$\boldsymbol{Min.ON\ Time > t_{syn} + t_{propa} + t_{CCPT}(max.) + t1.1(max.) + t1.2(max.)}$$

$$\boldsymbol{Min.OFF\ Time > t_{syn} + t_{propa} + t2.1(max.) + t2.2(max.)}$$

$$\boldsymbol{t1.1(max.) = \left(V_{th} + \frac{I_{DS}}{g_{fs}}\right) * \frac{C_{ISS}}{I_{SOURCE} * 0.75}}$$

$$\boldsymbol{t1.2(max.) = \frac{Q_{gd}}{V_{DS} - V_{th} + \frac{I_{DS}}{g_{fs}}} * \frac{V_{DS} - V_{th} + \frac{I_{DS}}{g_{fs}} - V_{OCP}}{I_{SOURCE} * 0.75}}$$

$$\boldsymbol{t2.1(max.) = \left(V_{DS} - V_{th} + \frac{I_{DS}}{g_{fs}}\right) * \frac{C_{ISS}}{I_{SINK} * 0.75}}$$

$$\boldsymbol{t2.2(max.) = \frac{Q_{gd}}{I_{SINK} * 0.75}}$$

Example:

- V_{th}:----------------------------------2.0V*(max value)
- C_{ISS}:--------------------------------- 950pF*(max value)
- t_{syn}:-----------------------------------1.25µs (max value)
- t_{propa}:---------------------------------400ns (max value)
- t_{CCPT}:-------------------------------- 0.94µs (max value)
- PWM freq:------------------------ 20kHz
- Duty-Cycle:------------------------15% (min value)
- I_{DS} = VBAT/1Ω * 1:---------------12A (max. on-duty)

- Q_{gd}:-------------------------4nC (max value)
- g_{fs}:-------------------------- 10S (min value)
- I_{source}:---------------------- 10mA
- I_{sink}:---------------------- 30mA
- V_{DS}:------------------------ 12V
- V_{OCP}:-----------------------200mV
- Load:-----------------------1Ω, 270µH

*taken from MOSFET datasheet

$$Min.ON\ Time > t_{syn} + t_{propa} + t_{CCPT}(max.) + t1.1(max.) + t1.2(max.)$$

$$Min.OFF\ Time > t_{syn} + t_{propa} + t2.1(max.) + t2.2(max.)$$

$$t1.1(max.) = \left(V_{th} + \frac{I_{DS}}{g_{fs}}\right) * \frac{C_{ISS}}{I_{SOURCE} * 0.75} \qquad t1.2(max.) = \frac{Q_{gd}}{V_{DS} - V_{th} + \frac{I_{DS}}{g_{fs}}} * \frac{V_{DS} - V_{th} + \frac{I_{DS}}{g_{fs}} - V_{OCP}}{I_{SOURCE} * 0.75}$$

$$t1.1(max.) = \left(2V + \frac{12A}{10S}\right) * \frac{950pF}{10mA * 0.75} \qquad t1.2(max.) = \frac{4nC}{12V - 2V + \frac{12A}{10S}} * \frac{12V - 2V + \frac{12A}{10S} - 0.2V}{10mA * 0.75}$$

$$t1.1(max.) = 405.3ns \qquad t1.2(max.) = 523.8ns$$

$$t2.1(max.) = \left(V_{DS} - V_{th} + \frac{I_{DS}}{g_{fs}}\right) * \frac{C_{ISS}}{I_{SINK} * 0.75} \qquad t2.2(max.) = \frac{Q_{gd}}{I_{SINK} * 0.75}$$

$$t2.1(max.) = \left(12V - 2V + \frac{12A}{10S}\right) * \frac{950pF}{30mA * 0.75} \qquad t2.2(max.) = \frac{4nC}{30mA * 0.75}$$

$$t2.1(max.) = 472.9ns \qquad t2.2(max.) = 178ns$$

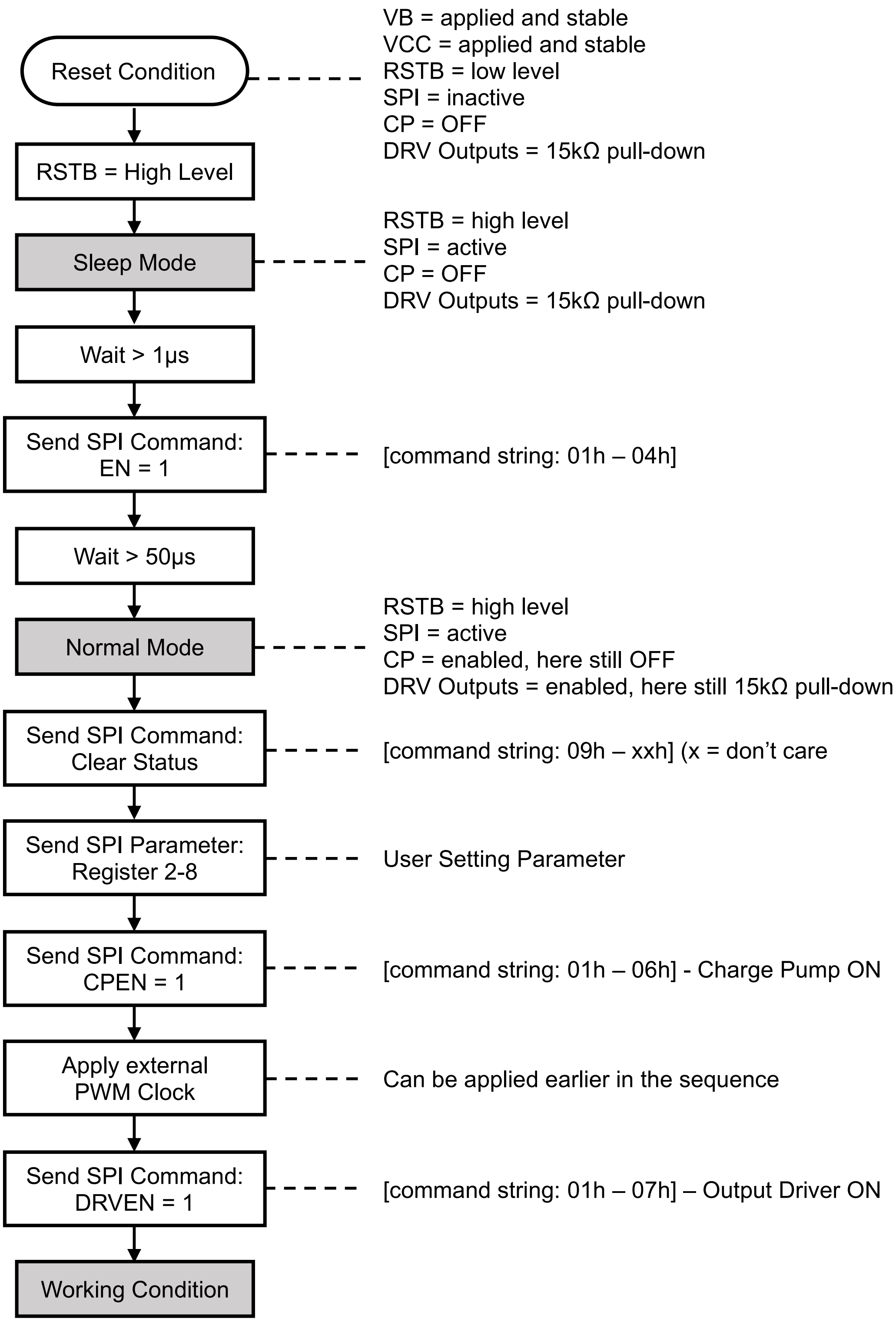
$$Min.ON\ Time > t_{syn} + t_{propa} + t_{CCPT}(max.) + t1.1(max.) + t1.2(max.)$$
$$Min.ON\ Time > 1.25\mu s + 400ns + 0.94\mu s + 405.3ns + 523.8ns$$
$$Min.ON\ Time > 3.52\mu s$$

$$Min.OFF\ Time > t_{syn} + t_{propa} + t2.1(max.) + t2.2(max.)$$
$$Min.OFF\ Time > 1.25\mu s + 400ns + 472.9ns + 178ns$$
$$Min.OFF\ Time > 2.30\mu s$$

$$PWM\ min.ON\ Time > (ON\ Time) - (OFF\ Time)$$
$$PWM\ min.ON\ Time > 3.52\mu s - 2.30\mu s$$
$$PWM\ min.ON\ Time > 1.22\mu s$$

$$PWM\ min.ON\ Duty = 1.22\mu s * 20kHz * 100 = 2.44\%$$
$$PWM\ max.ON\ Duty = (50\mu s - 1.22\mu s) * 20kHz * 100 = 97.56\%$$

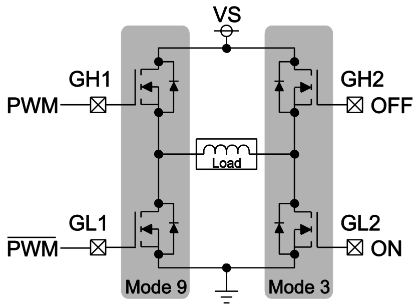
Standard Startup Sequence (for PWM Controlled Brushed Motor)



Default Startup Sequence for Full-Bridge Motor Control

Example:

- Load: Brushed Motor, Full-Bridge control
- Mode: Half-Bridge 1 → Mode 9, Half-Bridge 2 → Mode 3 (swap Mode for motor rotation direction)
- Protection Mode Setting: all latched, Under- and Overvoltage Protection enabled
- Source Current: 10mA
- Sink Current: 30mA
- Cross-Current Protection Time: 5µs
- OCP Threshold Voltage: 400mV
- OCP Filter Time: 10µs



Full-Bridge Control

1	Check Reset Condition	VB applied and stable VCC applied and stable RSTB = low level
2	Disable Reset	RSTB = high level
3	Entering Sleep Mode	Wait > 1µs before proceeding the sequence
4	Chip-Enable	SPI command string: 01h – 04h
5	Entering Normal Mode	Wait > 50µs before proceeding the sequence
6	Clear Status Register	SPI command string: 09h – 00h
7	Mode	SPI command string: 02h – 18h
8	Protection Mode	SPI command string: 03h – FCh
9	Source Current	SPI command string: 04h – 0Ah
10	Sink Current	SPI command string: 05h – 1Eh
11	Cross Current Protection Time	SPI command string: 06h – 10h
12	OCP Threshold Voltage	SPI command string: 07h – 02h
13	OCP Filter Time	SPI command string: 08h – 09h
14	Charge Pump Enable	SPI command string: 01h – 06h
15	PWM Clock	Apply external (or earlier in the sequence)
16	Output Driver Active	SPI command string: 01h – 07h
17	**Working Condition**	

Example Startup Sequence Table

Revision History

Date	Revision Number	Description
2023.11	001	New Release

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