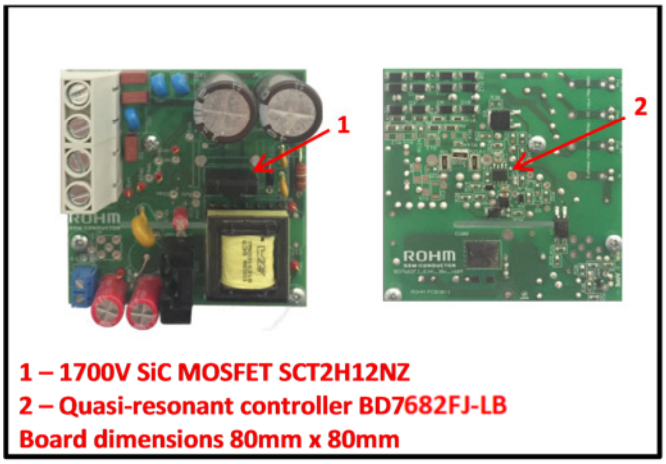
Controller BD7682FJ-LB

Quasi-resonant Auxiliary Power Supply with 1700V SiC MOSFET

Power converters used in industrial systems, as for instance photovoltaic (PV) inverters, uninterruptable power supplies (UPS) and industrial motor drives, need an auxiliary supply unit (AUX). Such unit provides the required power for system peripherals – i.e. Microprocessor, LCD display, sensors, fans, - as well as for gate drivers inside the main power circuit.

The toplogy typically used is flyback and the input voltage levels in 3-phase systems can go up to 480Vac or 900Vdc. Considering the reflected voltage in the primary side, which is added during switch blocking state, a device with breakdown voltage above 1500V is normally required. By using standard silicon devices, the possible implementations become either too complex, i.e. using the series connection of lower voltage devices, or very inefficient, i.e. using 1500V rated Silicon MOSFETs that show high losses and require bulky and expensive heat-sinks. In order to overcome these issues, a 1700V rated SiC MOSFET is used as single, high performance device for AUX applications.

This application note presents the AUX board developed by ROHM Semiconductor, shown in Figure 1. It is based on Flyback topology, and contains the device **SCT2H12NZ** [1] as main switch, in combination with **BD7682FJ-LB** [2][3], a quasi-resonant controller. The technique of quasi-resonance reduces the dynamic losses on the SiC MOSFET and consequently lowers its operating temperature.



Param.	Description	Value
V_{IN}	Input voltage	210...480 V_{AC} 300...to 900 V_{DC}
V_{OUT}	Output voltage	12 V_{DC} ± 3%
P_{OUT}	Output power	30 W @ $V_{IN.MIN}$ 40 W @ $V_{IN.MAX}$
f_{sw}	Switching frequency	90..120 kHz

Figure 1 – Top and Bottom views of the AUX Board, and its main electrical parameters.

The AUX board is able to operate with both AC and DC input voltages. It is therefore possible to derive the power directly from the grid or from the system DC link, e.g. after the PFC stage. In case of AC input, the accepted input voltage range goes from 210 V_{AC} to 480 V_{AC}. This option can be interesting for applications like UPS and industrial drives, where the power for the AUX board comes from the AC grid. In case of DC input, the input range goes from 300 V_{DC} to 900 V_{DC}. This can be useful for solar PV inverters, enabling the power to be extracted directly from the PV panels. Further electrical parameters of the AUX board can be found in the table of Figure 1.

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The simplified schematic of the AUX board is shown in Figure 2.

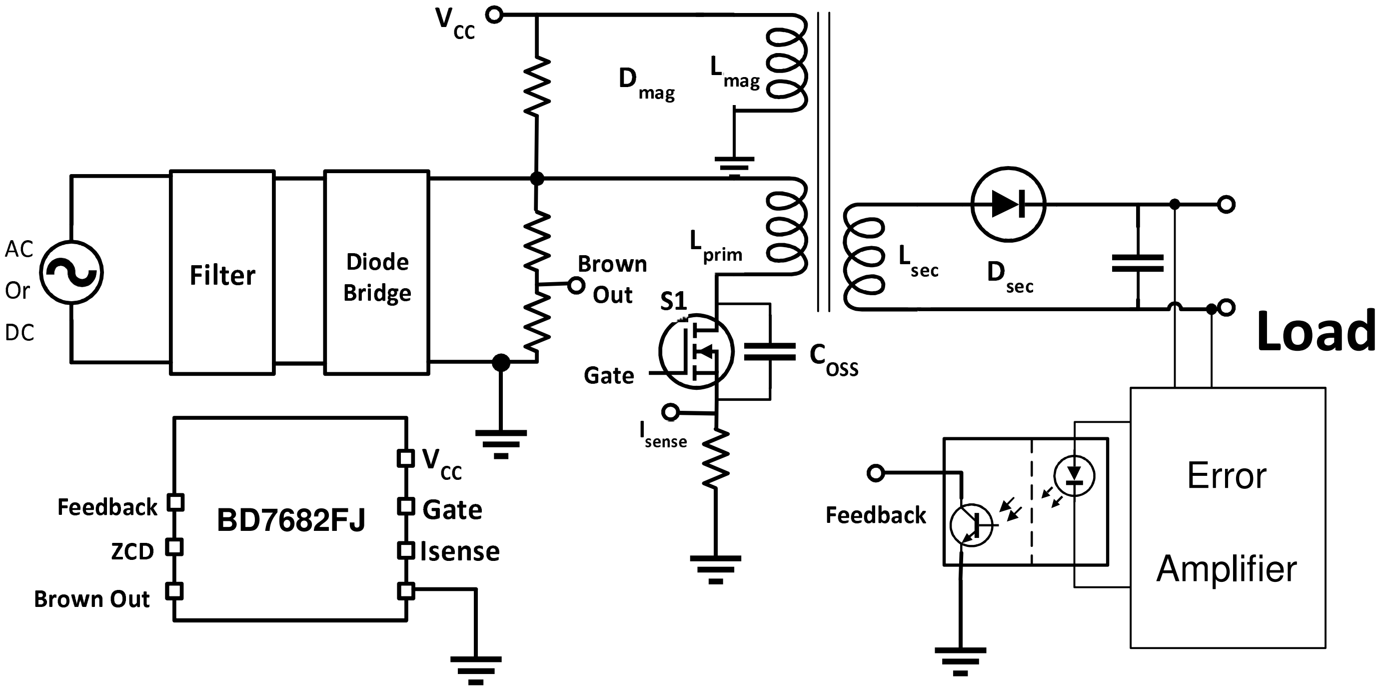


Figure 2 – Simplified schematic of the AUX board.

The next sections will describe the design of the AUX board, including its protection features like under-voltage, over-voltage and overcurrent. In addition, experimental results illustrate the operation and the performance of the board. The full schematic and the bill of materials from the AUX board are included in the appendices at the end of this document.

Contents

1 Design of the Quasi-resonant Flyback AUX Board

Quasi-resonant converters are a good alternative to reduce the dynamic losses, especially in low power applications. They make use of the oscillation between the output capacitance C_{OSS} of the switch and the primary side inductance L_{pri} of the transformer. These oscillations happen when the circuit operates in discontinuous current mode (DCM). If turn-on occurs in the nearby of one of the oscillation valleys, the dynamic losses of the switch are minimized. Figure 3 illustrates one of these cases.

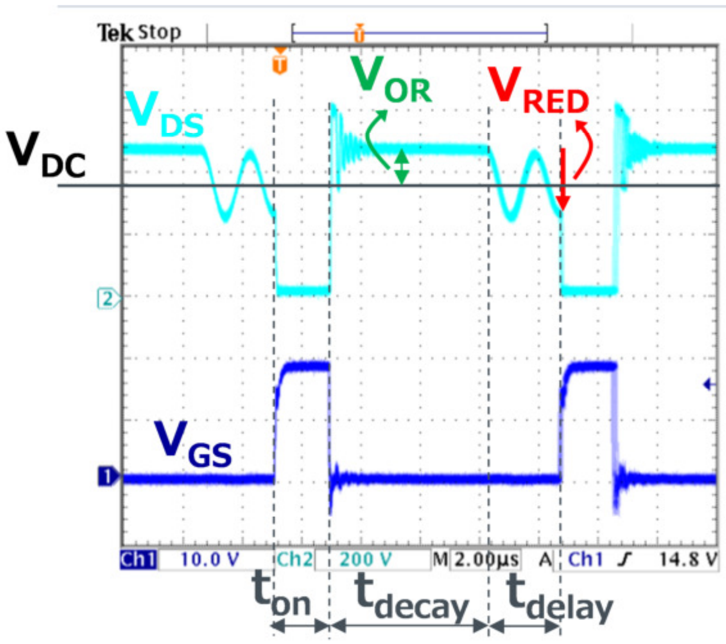


Figure 3 – Drain-to-source and gate-to-source waveforms in a quasi-resonant Flyback.

The switch stays on during t_{on}. During t_{decay} the free-wheeling current is flowing through the secondary side. In t_{delay} the current is zeroed, and the resonant tank, formed by the transformer primary winding L_{pri} and the output capacitance C_{OSS} of the Flyback switch starts to oscillate. The resonant frequency f_{res} is given by:

$$f_{res} = \frac{1}{2\pi\sqrt{L_{pri} \cdot C_{OSS}}} \tag{1}$$

The BD7682FJ controller is able to recognize a valley and to trigger the turn-on in the nearby of the valley. In Figure 3 the turn-on happens at the second valley of the oscillation. There is therefore a difference V_{RED} between the blocked voltage and the effective switched voltage. This will result in reduction of the turn-on losses, as it will be explained in section 1.2.

1.1 Flyback Transformer

The transformer dimensioning starts considering the reflected voltage V_{OR} to primary side, when the switch turned off. The V_{OR} is shown in Figure 3, and shall be chosen as to leave enough margins for the Flyback switch. Considering the maximum DC voltage – after the rectifying bridge - $V_{DC,MAX}$=900V, V_{OR} has been defined as V_{OR}=130V. From V_{OR} value it is possible to define the transformer turn ratio *Np/Ns*, and the maximum duty cycle of the switch, calculated for the minimum input voltage $V_{DC,MIN}$.

$$\boldsymbol{N_P/N_s = \frac{V_{OR}}{V_o+V_{f,Dsec}} = \frac{130\,V}{12\,V+1\,V} \rightarrow N_P/N_s = 10} \quad (2)$$

$$D_{max} = \frac{V_{OR}}{V_{OR}+V_{DC,MIN}} = \frac{130\,V}{130\,V+300\,V} \rightarrow D_{max} = 0.30 \quad (3)$$

This is well below 50% duty cycle, and guaranteed thus operation at DCM. Where $V_{f,Dsec}$ is the forward voltage of the secondary diode D_{sec}. The maximum value $L_{p,max}$ for primary side inductance L_{pri} is calculated to guarantee that DCM will occur for the entire range of power, input voltage and switching frequency. The equation below is used, derived from the Flyback operation. Please refer to Appendix A for detailed explanation.

$$L_{p,max} = \left(\frac{D_{max}\cdot V_{DC,MIN}}{\sqrt{\frac{2\cdot P_{out,max}\cdot f_{sw,min}}{\eta}}+D_{max}\cdot V_{DC,MIN}\cdot\pi\cdot f_{sw,min}\cdot\sqrt{C_{OSS}}}\right)^2 = \left(\frac{0.30\cdot 300V}{\sqrt{\frac{2\cdot 30W\cdot 60kHz}{0.85}}+0.30\cdot 300V\cdot\pi\cdot 90kHz\cdot\sqrt{100pF}}\right)^2 \rightarrow L_{p,max} = 1{,}07\ mH \quad (4)$$

Where $f_{sw,min}$=90 kHz is the minimum switching frequency – defined by design, – $P_{out,max}$ =30 W, as for the minimum input voltage – see Figure 1, –and η=85% is the expected efficiency of the converter. The chosen value of C_{OSS} was taken from the datasheet of SCT2H12NZ, see Figure 4. As the value is not a constant, the value at V_{DS}=1 V (C_{OSS}=100 pF.) was taken as worst case. In practice the voltage over the switch is much higher. However, by choosing at V_{DS}=1 V, the necessary design margin is given to compensate the effect of further parasitic capacitances present in the circuit. They can be due to e.g. the board layout, the winding capacity of the transformer, among others.

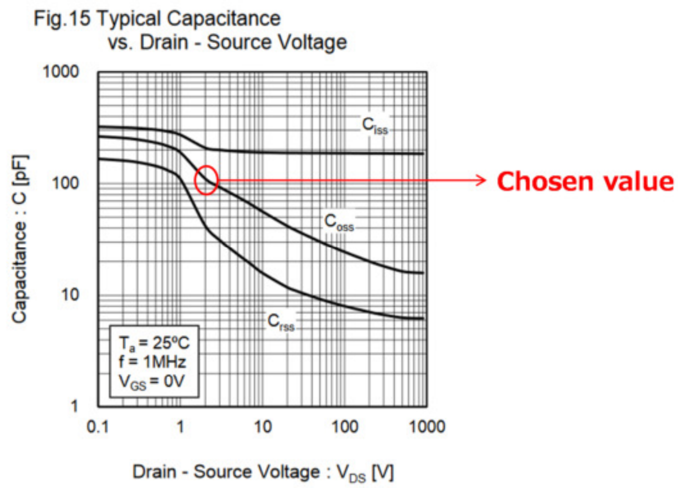


Figure 4 – Typical capacitances of SCT2H12NZ as function of drain-to-source voltage.

The peak current in the primary side I_{ppk} of the transformer is then calculated as:

$$I_{ppk} = \sqrt{\frac{2 \cdot P_{out,max}}{\eta \cdot L_{pri} \cdot f_{sw,min}}} = \sqrt{\frac{2 \cdot 48W}{0.85 \cdot 1.mH \cdot 90\ kHz}} \rightarrow I_{ppk} = 0.86\ A \qquad (5)$$

And consequently the peak current of the secondary side I_{spk}:

$$I_{spk} = I_{ppk} \cdot {}^{N_p}/_{N_s} \rightarrow I_{ppk} = 8.6\ A \qquad (6)$$

Finally, the auxiliary winding shall be designed. To properly drive the SIC MOSFET with a minimum gate-to-source voltage $V_{g.min}$=18 V, the controller BD-768xFJ-LB needs an auxiliary voltage V_{AUX} above 22 V. The value V_{AUX}=24V has been chosen. The number of turns for the auxiliary winding can be calculated from the secondary winding as:

$${}^{N_A}/_{N_S} = \frac{V_{AUX} + V_{D,aux}}{V_o + V_{D,sec}} = \frac{24\ V + 1\ V}{12\ V + 1\ V} \rightarrow {}^{N_A}/_{N_s} = 1.92 \qquad (7)$$

Table 1 summarizes the above calculated parameters of the transformer, as well as the characteristics of the transformer used in the AUX board. It is a customized transformer manufactured by Würth Elektronik (www.we-online.com), whose order number is 750316318. The datasheet of the transformer can be found in Appendix B.

The primary side is composed by two windings in series, while the secondary side has been implemented with two windings in parallel. The half-windings are interposed, in order to reduce the leakage inductance around 1% of L_{pri}. This will impact the switching behavior of the MOSFET. In addition, the windings have been implemented with Litz wire to reduce the losses due to skin effect.

Table 1 – Calculated parameters and characteristics of the used transformer.

Parameter	Calculated	Transformer (E25)
Primary inductance	1.07 mH	0.95 mH ±10%
Leakage inductance	--	1% (9 µH)
Maximum primary current	0.86 A	1.5 A *
Turn-ratio primary to secondary	10	10 ± 1%
Turn-ratio secondary to auxiliary	1.92	2 ± 1%

* Core saturation current

1.2 Flyback Switch

For the following sections, the full schematic depicted in Figure 5 shall be used as reference. The complete bill of materials of the board can be found in Appendix C.

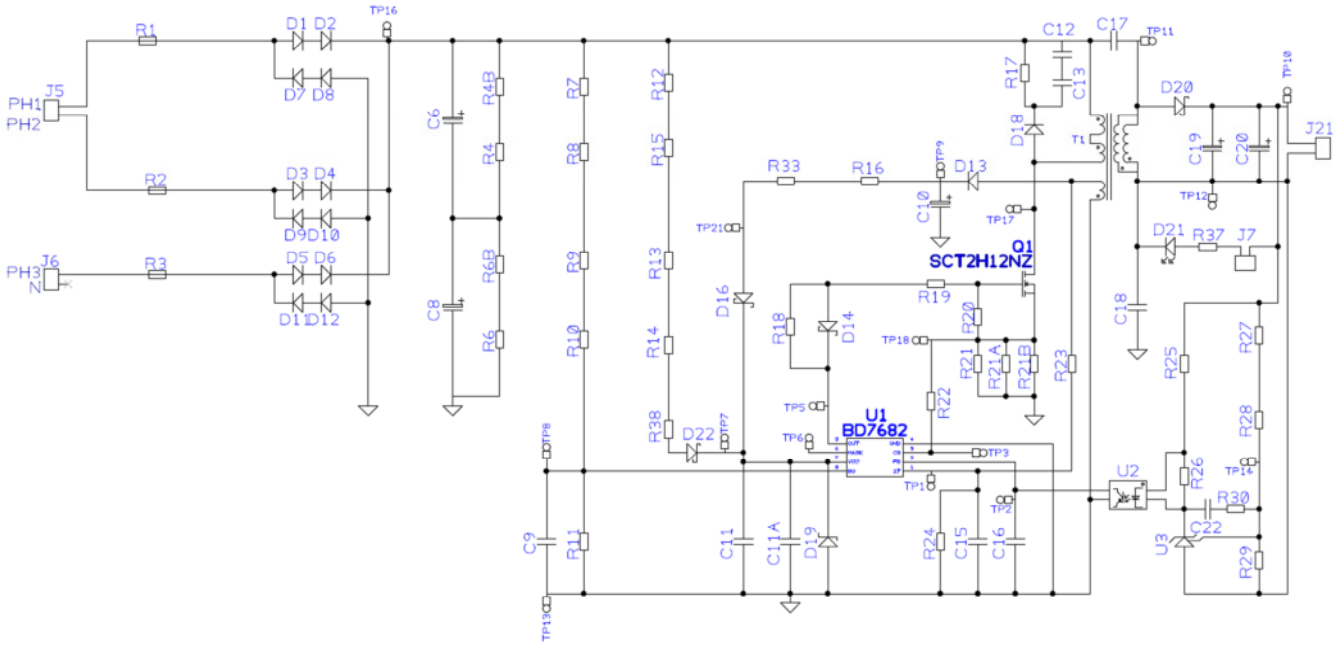


Figure 5 – Full schematic of the AUX board.

For the choice of the switch Q1, the following parameters will be considered:

- The root means square (RMS) value of the drain current $i_{d.Q1}$, to calculate the switch static losses;
- The switched voltage $V_{DS,sw}$ to calculate the dynamic losses
- The peak drain-to-source voltage, to determine the safety margin from the device breakdown voltage $V_{DS,BR}$.

1.2.1 Static losses

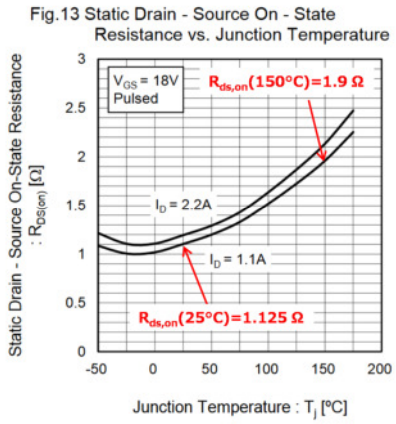
During the MOSFET conduction time t_{on}, the primary current flows through the MOSFET drain. After MOSFET turns off, the current ceases to flow. The instantaneous drain current is thus given as:

$$i_{d.Q1}(t) = \begin{cases} \frac{V_{DC} \cdot t}{L_{pri}} & for \quad 0 < t \le d \cdot T \\ 0 & for \quad d \cdot T < t < T \end{cases} \tag{8}$$

Where *d* is the instantaneous duty cycle. As *d* and *T* are functions from DC voltage and output power, so will be also $i_{d.S1.RMS}$:

$$i_{d.Q1.RMS}(V_{DC}, Po) = \sqrt{\frac{1}{T}\int_0^T i_{d.Q1}(t)^2 dt} \rightarrow i_{d.Q1.RMS}(300\,V, 30\,W) = 0.267\,A \tag{9}$$

For minimum input voltage and maximum power, the value of $i_{d.Q1.RMS}$=0.267 A. For the chosen MOSFET, this will lead to the static losses $P_{cond.Q1}$, calculated from the datasheet curve of on resistance $R_{ds,on}$ as function of junction temperature– see Figure 6.



$$P_{cond.Q1}(T_j) = R_{ds,on}(T_j) \cdot i_{d.Q1.RMS}{}^2 \qquad (10)$$

$$P_{cond.Q1}(25°C) = 1.125\ \Omega \cdot (0.267\ A)^2 \rightarrow P_{cond}(25°C) = 80\ mW$$

$$P_{cond.Q1}(150°C) = 1.9\ \Omega \cdot (0.267\ A)^2 \rightarrow P_{cond}(150°C) = 135\ mW$$

Figure 6 – $R_{ds,on}$ curve of SCT2H12NZ, and the calculated conduction losses for T_j=25°C and T_j=150°C.

As expected, due to much lower $R_{ds,on}$ of the SiC MOSFET, the static losses are very low. The majority of the losses are thus expected to come from the commutation of the device.

1.2.2 Dynamic losses

Figure 7 contains some graphs extracted from the datasheet of SCT2H12NZ. They show the dependency of turn-on and turn-off energies to the drain to source voltage (left) and to the drain current (middle). In addition, the value of the stored energy E_{OSS} in the MOSFET output capacitance is shown in the right side of Figure 7.

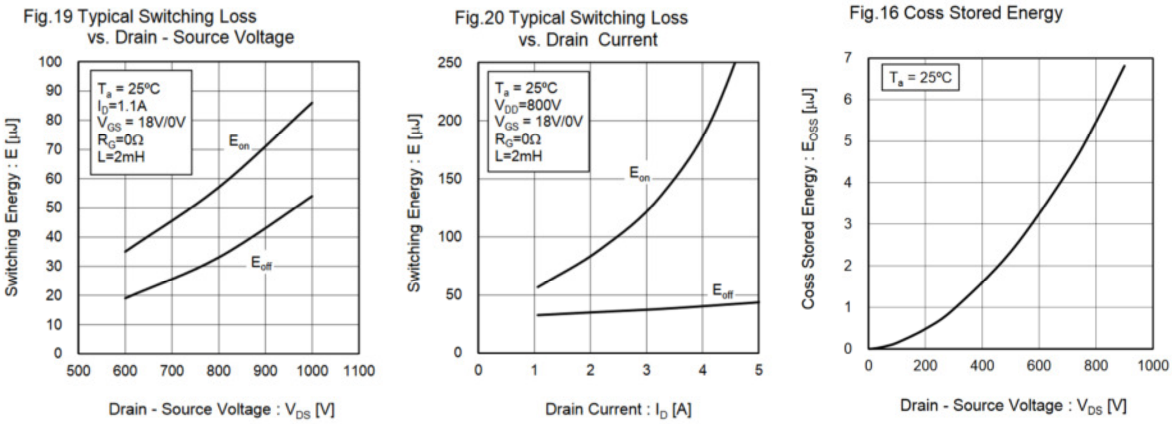


Figure 7 – SCT2H12NZ curves of E_{on}, E_{off} and E_{OSS}, extracted from datasheet.

The turn-off in the quasi-resonant Flyback is done through hard commutation. This causes a turn-off energy E_{off}, given in the device datasheet and shown in Figure 7 (left). It can be seen that the dependence on the switched voltage is quite strong. The dependence on the switched current - Figure 7 (middle), –is relatively low, instead. For an accurate calculation, the value of the energy stored in the output capacitor E_{OSS} - Figure 7 (right) - shall be subtracted from E_{off}. This energy will be used later to calculate turn-on losses.

Regarding the turn-on, as the Flyback works in discontinuous current mode (DCM), it will always occur at zero current. Therefore, in practice the only energy related to turn-on is related to the E_{OSS}, which will be dissipated through the MOSFET channel – see Figure 8.

The E_{OSS} has an exponential dependency to the drain-to-source voltage - Figure 7 (right). With the use of quasi-resonance technique, the voltage over C_{OSS} is reduced before turn-on – see V_{RED} in Figure 3. As consequence, part of E_{OSS} will return to the circuit, and the turn-on losses are consequently reduced.

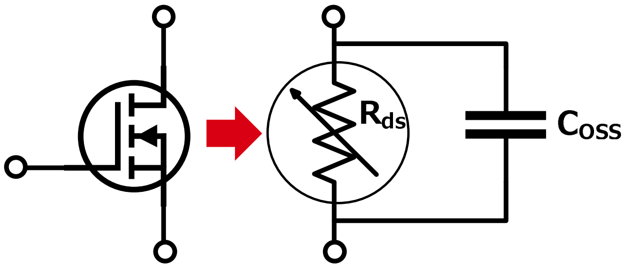


Figure 8 – Equivalent circuit of the MOSFET during turn-on.

The total switching energy of **Q1** for a certain input voltage V_{DC} can be then calculated as below:

$$E_{on.Q1}(V_{DC}) = E_{OSS}(V_{DC} + V_{OR} - V_{RED}) \quad (11)$$

$$E_{off.Q1}(V_{DC}) = E_{off}(V_{DC} + V_{OR}) - E_{OSS}(V_{DC} + V_{OR}) \quad (12)$$

E_{off} and E_{OSS} are extracted from datasheet curves in Figure 7. To obtain the dissipated power, the energies calculated above must be multiplied by the switching frequency. Therefore, the dynamic losses $P_{sw.Q1}$ can be calculated as:

$$P_{sw.Q1}(V_{DC}, f_{sw}) = [E_{on.Q1}(V_{DC}) + E_{off.Q1}(V_{DC})] \quad (13)$$

And the total losses of **Q1** as:

$$P_{Q1}(V_{DC}, f_{sw}, T_j) = P_{sw.Q1}(V_{DC}, f_{sw}) + \mathrm{P}_{\mathrm{cond.Q1}}(T_j) \quad (14)$$

$$P_{Q1}(300\,V, 90\,kHz, 125°C) = 0.91\,W$$

$$P_{Q1}(900\,V, 120\,kHz, 125°C) = 5.01\,W$$

Tests results at room temperature presented in section 2.3 demonstrate that it is possible to operate the AUX board without any heat-sink applied to the switch **Q1**, for the full range of input voltage and output power.

1.2.3 Gate circuitry

The recommended gate circuitry is for the SCT2H12NZ is depicted in Figure 9:

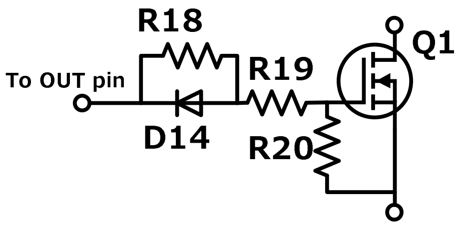


Figure 9 – Gate circuitry of SCT2H12NZ.

In order to reduce the turn-off losses, a small off resistor **R19** shall be used. A value of **R19**=10 Ω has been chosen. As mentioned before, the turn-on of the switch occurs at zero current. Therefore, the on gate resistor, given by the sum of **R18** and **R19**, is not relevant for the switch performance. The design rule for **R18** as 10 times higher than **R19**. Therefore **R18** = 100 Ω is used. To avoid oscillations, a resistor between gate and source is recommended, whose value is between 10 kΩ and 100 kΩ. A resistor **R20** = 47 kΩ was placed. Finally, the Schottky diode RB160M-60, rated for 60 V and 1 A, was chosen as **D14**.

1.2.4 Peak drain-to-source voltage

The peak V_{DS} voltage over the switch has three main components: the DC voltage V_{DC}, the reflected voltage V_{OR}, and the overvoltage during turn-off V_{spike}. By assuming V_{spike}=300 V:

$$V_{DS.PK} = \mathrm{V_{DC.MAX}} + \mathrm{V_{OR}} + \mathrm{V_{spike}} = 900\,V + 130\,V + 300\,V = 1330\,V \tag{15}$$

This means there is a margin of 20% from the breakdown voltage of SCT2H12NZ.

1.3 Input capacitor

For the choice of the input capacitor C_{IN} it was used the empirical design rule of 1 µF for each 1 W output power. This results in 40 µF, to which an additional 20% margin applied, leading to C_{IN}=48 µF. Due to availability, and also to accomplish the voltage requirements, the input capacitance have been implement with two capacitors (**C6** and **C8**) in series. Each of them has 100 µF capacitance and 450 V nominal voltage, resulting in C_{IN}=50 µF, rated for 900 V.
The resistors **R4**, **R4B**, **R6** and **R6B** have been implemented to equalize the voltage over both capacitors. Each of them has a resistance of 470 kΩ.

1.4 Current sensing resistor

The resistance R_{sense} senses the primary side current. It is connected between the source of **Q1** and the primary side ground. The signal is send to pin **CS**, and if it reaches 1.0 V (typ), the switch turned-on. The top and bottom limits of **CS** are $V_{lim,top}$=1.05 V and $V_{lim,bot}$=0.95 V respectively. Considering them, values for R_{sense} can be calculated as:

$$R_{sense1} = \frac{V_{lim,top}}{I_{ppk}} = \frac{1.05\ V}{0.86\ A} = 1.22\ \Omega \tag{16}$$

$$R_{sense2} = \frac{V_{lim,bot}}{I_{ppk}} = \frac{0.95\ V}{0.86\ A} = 1.16\ \Omega \tag{17}$$

The chosen value is R_{sense1}, based on the top limit of **CS**. In the AUX board it is implement through resistors **R21**=3 Ω, **R21A**=3 Ω and **R21B**=6.8 Ω, connected in parallel. Together they form an R_{sense}=1.23 Ω.

1.5 Configurable Overload Protection

The pin **ZT** of BD7682FJ-LB can be used to reduce the limits of **CS** for high values of V_{DC}. The voltage through the auxiliary winding is sensed through the resistor **R23** – see Figure 10 – when **Q1** is turned-on. If I_{ZT} > 1 mA, **CS** level is lowered.

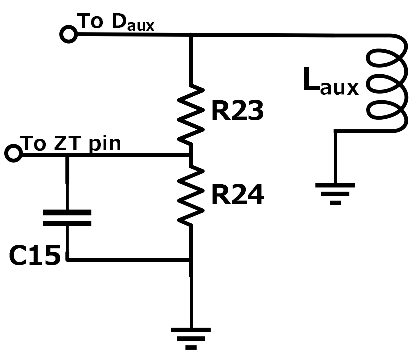


Figure 10 – Circuitry for output overload detection.

The resistor R23 can be calculated as below:

$$R23 = V_{change} \cdot {}^{N_A}/_{N_P} \cdot \frac{1}{I_{ZT}} \tag{18}$$

In the AUX board, this function has not been used. Therefore R23 was chosen 120 kΩ.

1.6 Valley detection

The pin **ZT** has also the function to detect the valleys of V_{DS} oscillation when **Q1** is off. The resistor **R24** - Figure 10 – is calculated so as not to generate a sensing voltage above the overvoltage protection level V_{ZT}=3.25 V (min). Assuming a 20% margin, V_{R24}=2.7 V, **R24** can be calculated as:

$$V_{R24} = \left(V_o + V_{f,Dsec}\right) \cdot {}^{N_A}/_{N_S} \cdot \frac{R24}{R23+R24} \tag{19}$$

$$R24 = \frac{R23}{\frac{\left(V_o+V_{f,Dsec}\right)}{V_{24}} \cdot {}^{N_A}/_{N_S} - 1} \rightarrow R24 = 13.9\ k\Omega \tag{20}$$

The chosen value for **R24**=12 kΩ. The ZT capacitor **C15** has the function to stabilize V_{ZT}, and avoid flickering of bottom detection. Its value can be defined empirically, in the AUX board it is **C15**=47 pF.

1.7 Flyback Snubber

The leakage inductance L_{leak} of the transformer causes a voltage overshoot over the switch **Q1** during its turn-off. This overvoltage appears on the drain-to-source voltage of the MOSFET and can be reflected also to other components in the circuit. Therefore a snubber circuit is recommended to limit this surge-voltage. In the AUX board, an RCD (resistor-capacitor-diode) snubber has been implemented. The configuration is shown in Figure 11. The design procedure is explained in the following.

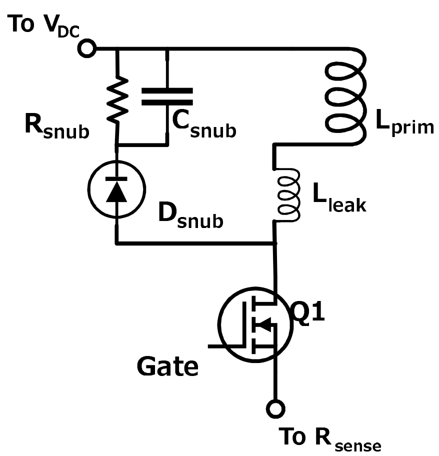


Figure 11 – Circuitry of the Flyback snubber.

1.7.1 Snubber resistor

As assumed in section 1.2.4 , the allowed overshoot voltage V_{spike}=300V. The snubber resistor R_{snub} is calculated from the power generated by the leakage current L_{leak} at maximum I_{ppk} and maximum f_{sw}. As this power must be dissipated inside the snubber:

$$P_{leak} = \frac{1}{2} \cdot L_{leak} \cdot I_{pri}{}^2 \cdot \frac{V_{SPIKE}+V_{OR}}{V_{spike}} \cdot f_{sw} \tag{21}$$

$$R_{snub} =\cdot \frac{(V_{SPIKE}+V_{OR})^2}{P_{leak}} = \frac{(300\,V+130\,V)^2}{P_{leak}} \rightarrow R_{snub} = 326\ k\Omega \tag{22}$$

R_{snub} is implemented through resistors **R17**=330 kΩ

1.7.2 Snubber capacitor

The snubber capacitor C_{snub} is calculated from accepted voltage ripple ΔV_{Csnub}. As a design rule, it is defined as 5% of the overshoot voltage V_{spike}. Therefore:

$$\Delta V_{Csnub} = \frac{V_{snub}}{R_{snub}} \cdot \frac{1}{C_{snub}} \cdot \frac{1}{f_{sw}} \rightarrow \frac{V_{spike}}{10} = \frac{V_{spike}+V_{OR}}{R_{snub}} \cdot \frac{1}{C_{snub}} \cdot \frac{1}{f_{sw}} \tag{23}$$

$$C_{snub} =\cdot \frac{(V_{spike}+V_{OR})}{\frac{(V_{spike}+V_{OR})}{20} \cdot R_{snub} \cdot f_{sw}} \rightarrow C_{snub} = 0.61\ nF \tag{24}$$

C_{snub} is implemented through capacitors **C12** and **C13** in series, each one with capacitance of 2.2 nF and rated for 1 kV.

1.7.3 Snubber diode

D_{snub} is implemented through diodes **D15** and **D15B** in series. Each one is a fast diode, rated for 1 kV and 1.5 A.

1.8 V_{CC} Diode

When **Q1** is ON, the auxiliary diode D_{aux} is reversely polarized. The voltage blocked by D_{aux} is calculated below, where $V_{CC.MAX}$ = 31.5 V is the maximum voltage supported by the controller:

$$V_{Daux} = V_{CC.MAX} + V_{DC.MAX} \cdot {}^{N_A}/_{N_p} = 31.5\,V + 900V \cdot {}^{1}/_{5} \rightarrow V_{Daux} = 211.5\,V \tag{25}$$

The auxiliary diode **D13** has been implemented with a fast diode RF101L4S, rated for 400V and 1A.

1.9 V_{CC} Surge limiting resistor

The V_{spike} caused by the turn-off of **Q1** can generate overshoots in the auxiliary winding and consequently trigger the OVP of the controller. To avoid that, a resistor **R16**=1.5 kΩ has been place between the auxiliary diode and the V_{CC} pin.

1.10 Start-up circuit

During the start-up, the energy for the controller comes from the input voltage source. A start resistance R_{START} is then put in between V_{IN} and V_{CC}. As the BD7682FJ-LB needs a minimum current I_{START}=40 µA through the VCC pin to start, RSTART can be derived from inequations:

$$R_{START} \leq \cdot \frac{V_{DC.START}-V_{UVLO}}{I_{START}} \rightarrow R_{START} \leq \frac{300\,V-20\,V}{40\,\mu A} \rightarrow R_{START} \leq 7000\,k\Omega \tag{26}$$

$$R_{START} \geq \cdot \frac{V_{DC.MAX}-V_{OVP}}{I_{CC.PROT}} \rightarrow R_{START} \geq \frac{900\,V-31.5\,V}{300\,mA} \rightarrow R_{START} \geq 800\,k\Omega \tag{27}$$

Where $V_{DC,START}$ is the minimum input voltage for the system start, V_{UVLO} is the under voltage lockout of the controller, V_{OVP} is the overvoltage protection, and $I_{CC.PROT}$ is the maximum current through V_{CC} pin.

The start resistance was implemented through resistors **R12**, **R13**, **R14** and **R15**, associated in series. Each of them has 470 kΩ, therefore R_{START} = 1880 kΩ. The dissipated power in R_{START} after start-up can be calculated as:

$$P_{los.START} = \frac{(V_{DC}-V_{CC})^2 \cdot}{R_{START}} \tag{28}$$

For maximum V_{DC} = 900 V, $P_{los.START}$= 412 mW. For minimum V_{DC} = 300 V, losses are reduced to $P_{los.START}$= 41.7 mW. The start-up time will be defined by R_{START} in combination with the V_{CC} capacitor **C11**=2.2 µF. The start-up time T_{START} can be calculated as:

$$T_{START} = \frac{C_{11} \cdot V_{UVLO} \cdot R_{START}}{V_{DC}} \tag{29}$$

From which the start-up is T_{START}=276 ms for V_{DC}=300 V, and T_{START}=92 ms for V_{DC}=900 V. If a faster start-up time is required, the resistance of R_{START} shall be reduced. The drawback is though the increase of $P_{los.START}$. Appendix E presents an alternative start-up, where $P_{los.START}$ is totally avoided without compromising the start-up time.

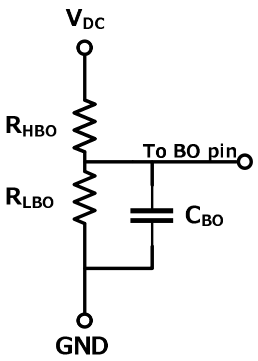
1.11 Brown-out circuit

The brown-out (BO) pin of micro-controller can identify fails in the input voltage fails due to e.g. grid failure. BD7682FJ-LB has typical values of brown-out detection voltage V_{BO}=1.0 V and detection hysteresis current I_{BO}=15 µA.
The high and low voltage limits for brown-out detection – V_{BOH} and V_{BOL} respectively – have been defined as function of the minimum input voltage as:

$$V_{BOH} = 98\% \cdot V_{DC.MIN} \rightarrow V_{BOH} = 294\,V \quad (30)$$

$$V_{BOL} = 90\% \cdot V_{DC.MIN} \rightarrow V_{BOL} = 270\,V \quad (31)$$

From these definitions, it is possible to calculate the resistances R_{HBO} and R_{LBO} – see Figure 12.



$$\mathrm{R_{HBO}} = \frac{V_{BOH}-V_{BOL}}{I_{BO}} = \frac{294\,V-270\,V}{15\,\mu A} = 1.6\,M\Omega \quad (32)$$

Chosen R_{HBO}=1.88 MΩ

$$\mathrm{R_{LBO}} = \frac{V_{BO}\cdot \mathrm{R_{HBO}}}{(V_{BOL}-V_{BO})} = \frac{1\,V\cdot 1.88\,M\Omega}{(270\,V-1\,V)} = 6.9\,k\Omega \quad (33)$$

Chosen R_{LBO}=10 kΩ

Figure 12 – Brown-out circuitry and calculation of its elements.

R_{HBO} has been implemented through the series association of resistors **R8**, **R9**, **R10**, each of them with 470 kΩ, whilst R_{LBO} has been implemented with **R10**. For the brown out capacitance C_{BO}, the capacitor **C9**= 00 nF is placed.
With the chosen values, the real brown-out voltage will be then:

$$V_{BO.real} = \frac{V_{BO}\cdot(R_{HBO}+R_{LBO})}{R_{LBO}} = \frac{1\,V\cdot(1.88\,M\Omega+10\,k\Omega)}{10\,k\Omega} \rightarrow V_{BO.real} = 204\,V \quad (34)$$

The brown out function stops only the Flyback operation. The controller itself continues to operate as long as V_{CC} does not go below under voltage lockout.

1.12 Output Diode

In order to reduce conduction losses, a Schottky barrier diode is recommended for the output rectification diode **D20**. The maximum blocking voltage is given by:

$$V_{D,sec} = V_{OUT} + V_{f,Dsec} + V_{DC.MAX} \cdot {}^{N_S}/_{N_P} = 12\,V + 1.0\,V + 900\,V \cdot {}^{8}/_{80} \rightarrow V_{D,sec} = 103\,V \quad (35)$$

The Schottky diode MBRF30200T, rated for 200 V has been chosen. The device is packaged in isolated TO-220, and contains two diode chips, each one rated for 10 A. For the maximum average output current I_{Dsec}=40 W /12 V = 3.33 A, the forward voltage is around $V_{f,Dsec}$=0.7 V for T_j > 25°C. This leads to a power dissipation of 2.3W. For a better thermal dissipation, a small heat-sink has been connected to the back side of the diode.

1.13 Output capacitance

The choice of the output capacitor is based on its equivalent series resistance (ESR). Given the peak-to-peak ripple ΔV_O:

$$\Delta V_O = 1\% \cdot V_O \rightarrow \Delta V_O = 0.12\,V \tag{36}$$

For the condition that the MOSFET **Q1** is turned off, the current from secondary winding charges the output capacitor and the load current is also supplied. Therefore:

$$R_{Co} < \frac{\Delta V_O}{I_{sec}-I_O} = \frac{\Delta V_O}{\left(I_{pri} \cdot {}^{N_P}/_{N_S} - I_O\right)\cdot} = \frac{0.12\,V}{0.86\,A \cdot 10 - 3.33\,A} \rightarrow R_{Co} < 20.5\,m\Omega \tag{37}$$

The rated voltage of the capacitor shall be twice V_O, or 24 V. Two 35 V electrolytic capacitors, **C19** and **C20** from Würth Electronics have been implemented in parallel. Each one has 470 µF, and ESR=34 mΩ (max).

1.14 Output Voltage Sensing

The sensing of output voltage is done through the optocoupler PC817. The sensing loop is composed by the resistors **R25**, **R26**, **R27**, **R28** and **R29**, in combination to the voltage reference **U3** – please refer to Figure 13.

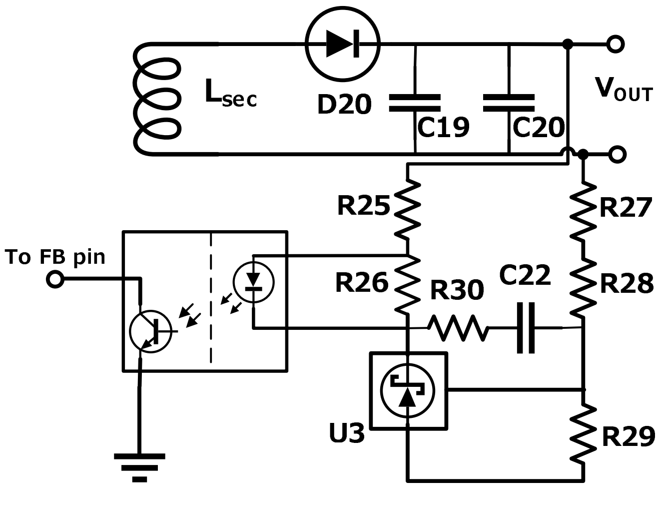


Figure 13 – Feedback circuitry of the output voltage.

The integrated circuit, TL431, has a reference voltage V_{ref} = 2.495 V (typ). The relationship between the resistances values are given by:

$$\frac{R29}{R27+R28+R29} = \frac{V_{ref}}{V_O} \rightarrow (R27 + R28) = R29 \cdot \left(\frac{V_{ref}}{V_O} - 1\right) \quad (38)$$

If one defines **R29**=51 kΩ, then **(R27 + R28)**=194.3 kΩ. Chosen values were then **R27**=15 kΩ and **R29** = 180 kΩ.

1.15 Adjustments in the control circuit

In Figure 13 **R30** and **C22** are parts for phase compensation. Recommended values are **C22**=100 nF, and a valur between 1 kΩ<**R30**<30kΩ. In the AUX board the value **R30** = 12 kΩ.
R25 is a resistor which limits a control circuit current. By defining an optocoupler current I_{OC}=30 mA, the resulting forward voltage of the LED is around V_{OC}=1 V. **R25** can be calculated as

$$R25 = \frac{V_{out} - V_{ref} - V_{OC}}{I_{OC}} \rightarrow R25 = 283\Omega \quad (39)$$

Chosen values was **R25** = 300Ω.
R26 guarantees a minimum operating current for TL431 $I_{ref.min}$=1 mA. As V_{OC}=1 V, **R26**=1kΩ.

1.16 Testing points

The AUX board contains several testing points, from which it is possible to observe the board operation. The test points and the related signals are given in Table 2.

Table 2 – Testing points in AUX board.

Test Point	Signal
TP1	Controller ZT
TP2	Controller FB
TP5	Controller OUT
TP7	V_{CC}
TP8	Brown-out
TP10	V_{OUT}
TP11	Trafo sec. terminal
TP13	Primary GND
TP16	V_{IN}
TP18	Current sense

2 Implementation and practical tests with AUX Board

The AUX board has been implemented in a printed circuit board (PCB), whose dimensions are 8 cm x 8 cm – see Figure 14. All surface mount devices (SMD) components have been assembled on the bottom side. On the top side were soldered the thru hole devices (THD) and connectors. The layout of both sides is given in Appendix D. In the following sections, experimental results at different input voltages and output power are presented and discussed.

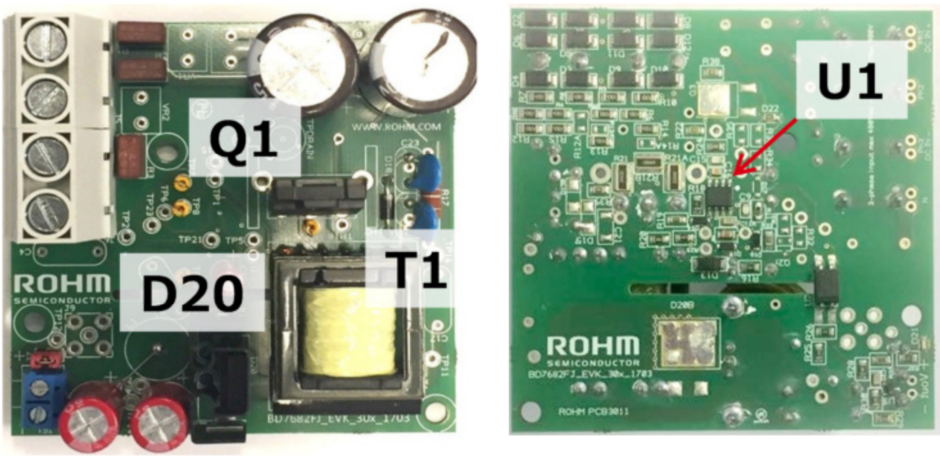
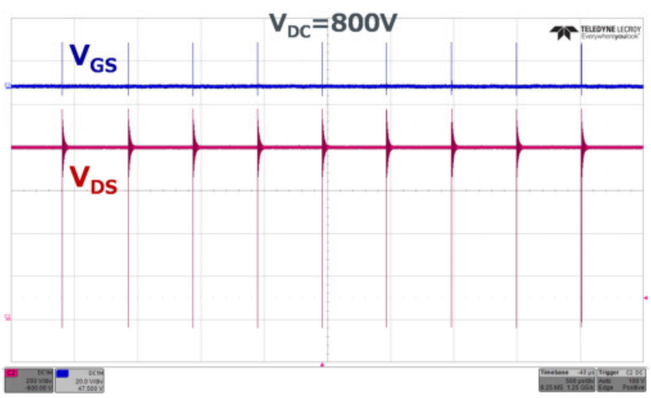


Figure 14 – Top side (left) and bottom side (right) of the AUX board.

2.1 Operation at no load

At no load operation, the controller goes in burst mode – see Figure 16 – and the switching frequency is reduced to some kHz. The dynamic losses of the Flyback components are consequently reduced. Measured stand-by losses are given in the table on the right side of Figure 15. They are expected to come mainly from the resistive dividers present on the circuit: input capacitor balance, start-up and input voltage sense.



DC voltage	Stand-by losses
300 V	0.372 W
900 V	1.7 W

Figure 15 – Waveforms from Fyback switch during burst mode, for V_{DC} = 800 V.

2.2 Normal operation

Figure 16 presents the waveforms from SCT2H12NZ during normal operation of the Flyback circuit, for V_{DC} = 800 V and different values of output power. Time periods t_{on}, t_{decay} and t_{delay} are indicated, according to the description in Figure 3. For light power – left side – the controller waits several valleys to switch the MOSFET on. Therefore, the switching frequency is quite low, eventually below the defined frequency range.

As the output power increases, the number of oscillations is reduced. As consequence, t_{delay} is reduced, and the switching frequency increases. At nominal power, the turn-on occurs already in the first valley.

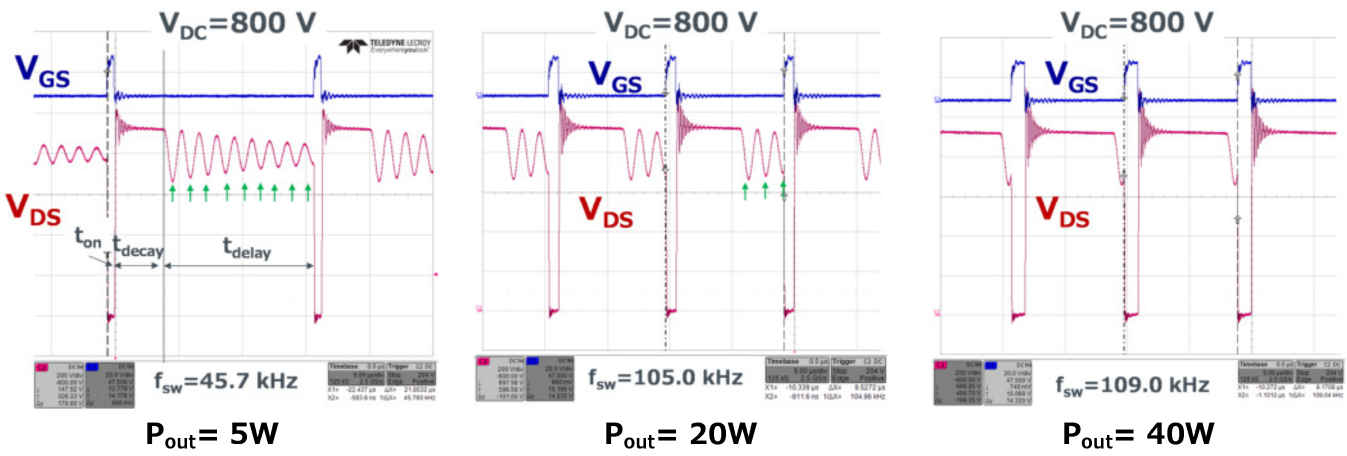


Figure 16 – Waveforms from Flyback switch during different output power conditions, V_{DC} = 800 V.

2.3 Efficiency and temperature measurements

The efficiency of the AUX board has been measured for three different input voltage values. The efficiency curves are shown in Figure 17. As a DC power source was used, it was connected directly to the input capacitors. This way, the rectifying bridge is by-passed, saving the losses that would otherwise come from the bridge diodes.

Efficiency is increasing with the output power, and it is higher for lower levels of input voltage. For V_{DC} = 300 V, the measured peak efficiency η=88% at P_{OUT}=33W – above that the overload protection was activated.

The temperature of the main components of AUX board has been measured, namely the SiC MOSFET (**Q1**), the Flyback transformer and the secondary diode (**D20**). The measurements were performed using an infrared camera. The thermal images are presented in Figure 18. They were taken at room temperature, V_{DC}=800 V and P_{OUT}=40W. The case temperature of the SiC MOSFET (Sp1) is around 84°C, even without the use of an external heatsink and without forced ventilation. The temperature of the Fyback transformer (Sp2), registered on the winding corner, is slightly above 70°C. The measured temperature of the output diode (Sp3) was around 95°C.

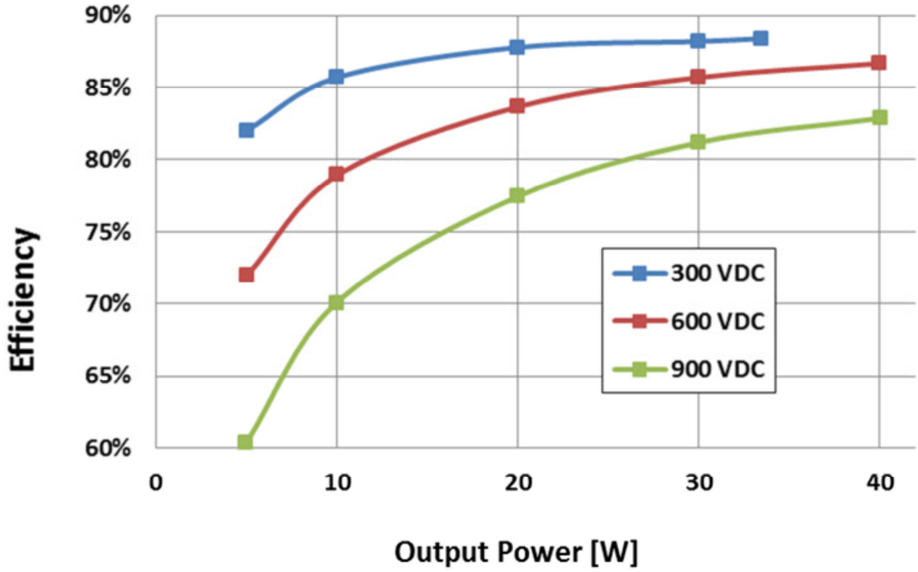


Figure 17 – Efficiency curve of the AUX board for several DC input voltage values.

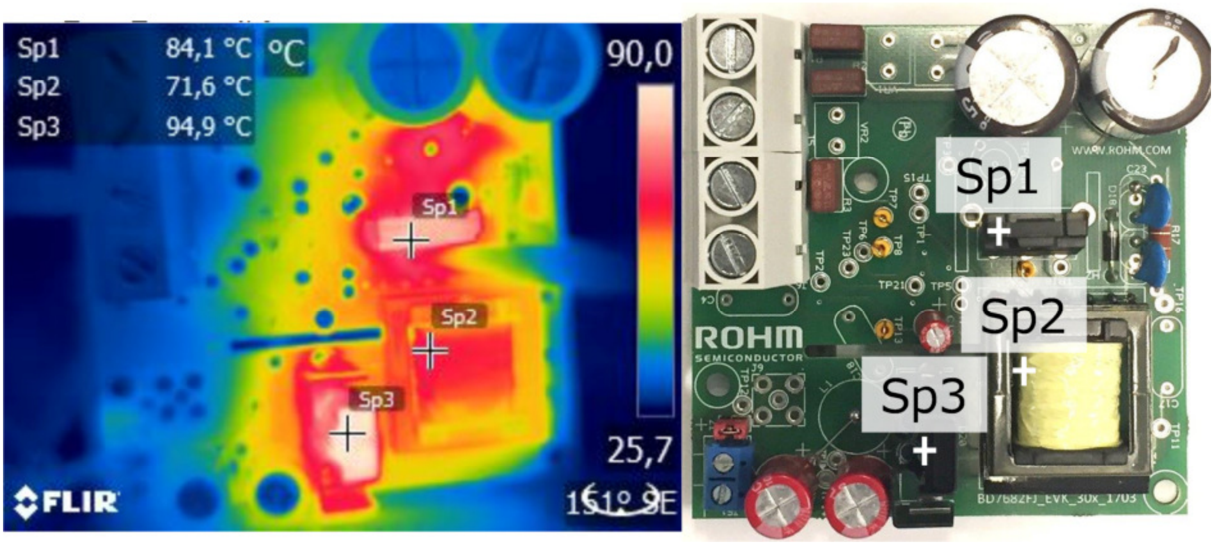


Figure 18 – Temperature measurements from main components of the AUX board.

3 Summary

This document presented the design procedure of an auxiliary power supply, based on Flyback topology, focused on industrial applications as auxiliary power supply. Main devices of this design are the SiC MOSFET SCT2H12NZ, with very low on resistance, and the quasi resonant controller BD7682FJ-LB. They enable a simple electrical and thermal design, reducing the amount of devices, and avoiding the use of heat-sink for the Flyback switch.
Experimental tests in the AUX board proved the operation principle of the quasi resonant controller. Thermal and efficient measurements showed also the reduced amount of losses in the SiC MOSFET, proving it is the right choice for auxiliary supplies in 3-phase industrial systems.

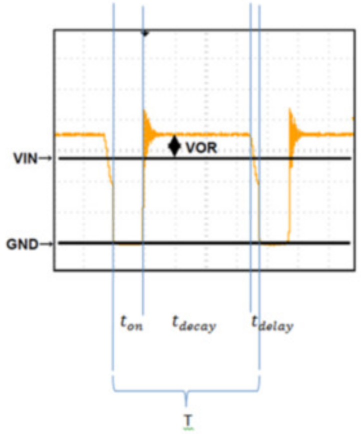
4 References

[1] Datasheet of SCT2H12NZ http://www.rohm.com/web/global/datasheet/SCT2H12NZ/sct2h12nz-e
[2] Datasheet of BD768xFJ-LB controller family, available at: http://www.rohm.de/web/de/products/-/product/BD7682FJ-LB
[3] Application Note "BD768xFJ-LB series Quasi-Resonant converter Technical Design", available at: http://rohmfs.rohm.com/en/products/databook/applinote/ic/power/acdc_converter/bd768xfj-lb_appli-e.pdf

Appendix A. Primary side current calculation equation.

This section presents the steps to reach the equation used to calculate the maximum current through the primary winding of the Flyback transformer. It starts from the time equations during Flyback operation – see Figure 16.

As worst case have to be used maximum load ($P_{out,max}$), minimum input voltage ($V_{DC.\min}$) and minimum target frequency ($f_{sw,min}$):



$$t_{on} + t_{decay} + t_{delay} = \frac{1}{f_{sw,min}} \tag{40}$$

$$\frac{L_{p,max} I_{ppk}}{V_{DC.min}} + \frac{L_{s,max} I_{spk}}{V_o} + \frac{1}{2}\cdot\frac{1}{f_{res}} = \frac{1}{f_{sw,min}} \tag{41}$$

$$\frac{L_{p,max} I_{ppk}}{V_{DC.min}} + \frac{L_{p,max} I_{ppk}\frac{N_S}{N_P}}{V_o} + \frac{1}{2}\cdot\frac{1}{\frac{1}{2\pi\sqrt{L_{p,max}C_{OSS}}}} = \frac{1}{f_{sw,min}} \tag{42}$$

$$\frac{L_{p,max} I_{ppk}}{V_{DC.min}} + \frac{L_{p,max} I_{ppk}}{V_{OR}} + \pi\sqrt{L_{p,max}C_{OSS}} = \frac{1}{f_{sw,min}} \tag{43}$$

Since $I_{ppk} = \sqrt{\frac{2\cdot P_{out,max}}{\eta\cdot L_{p,max}\cdot f_{sw,min}}}$ then:

$$L_p\, f_{sw,min}\sqrt{\frac{2\cdot P_{out,max}}{\eta\, L_{p,max}\cdot f_{sw,min}}}\left(\frac{1}{V_{DC.MIN}} + \frac{1}{V_{OR}}\right) + \pi\, f_{sw,min}\sqrt{L_{p,max}C_{OSS}} = 1 \tag{44}$$

$$\sqrt{\frac{2\cdot P_{out,max}\cdot L_{p,max}\cdot f_{sw,min}}{\eta}}\left(\frac{1}{V_{DC.MIN}} + \frac{1}{V_{OR}}\right) + \pi\, f_{sw,min}\sqrt{L_{p,max}C_{OSS}} = 1 \tag{45}$$

$$\sqrt{\frac{2\cdot P_{out,max}\cdot f_{sw,min}}{\eta}}\left(\frac{1}{V_{DC.MIN}} + \frac{1}{V_{OR}}\right) + \pi\, f_{sw,min}\sqrt{C_{OSS}} = \frac{1}{\sqrt{L_{p,max}}} \tag{46}$$

$$L_{p,max} = \frac{1}{\left(\sqrt{\frac{2\cdot P_{out,max}\cdot f_{sw,min}}{\eta}}\left(\frac{1}{V_{DC.MIN}}+\frac{1}{V_{OR}}\right)+\pi\, f_{sw,min}\sqrt{C_{OSS}}\right)^2} \tag{47}$$

Transforming it as function of D_{max} ($V_{OR} = \frac{D_{max}\cdot V_{in}}{1-D_{max}}$):

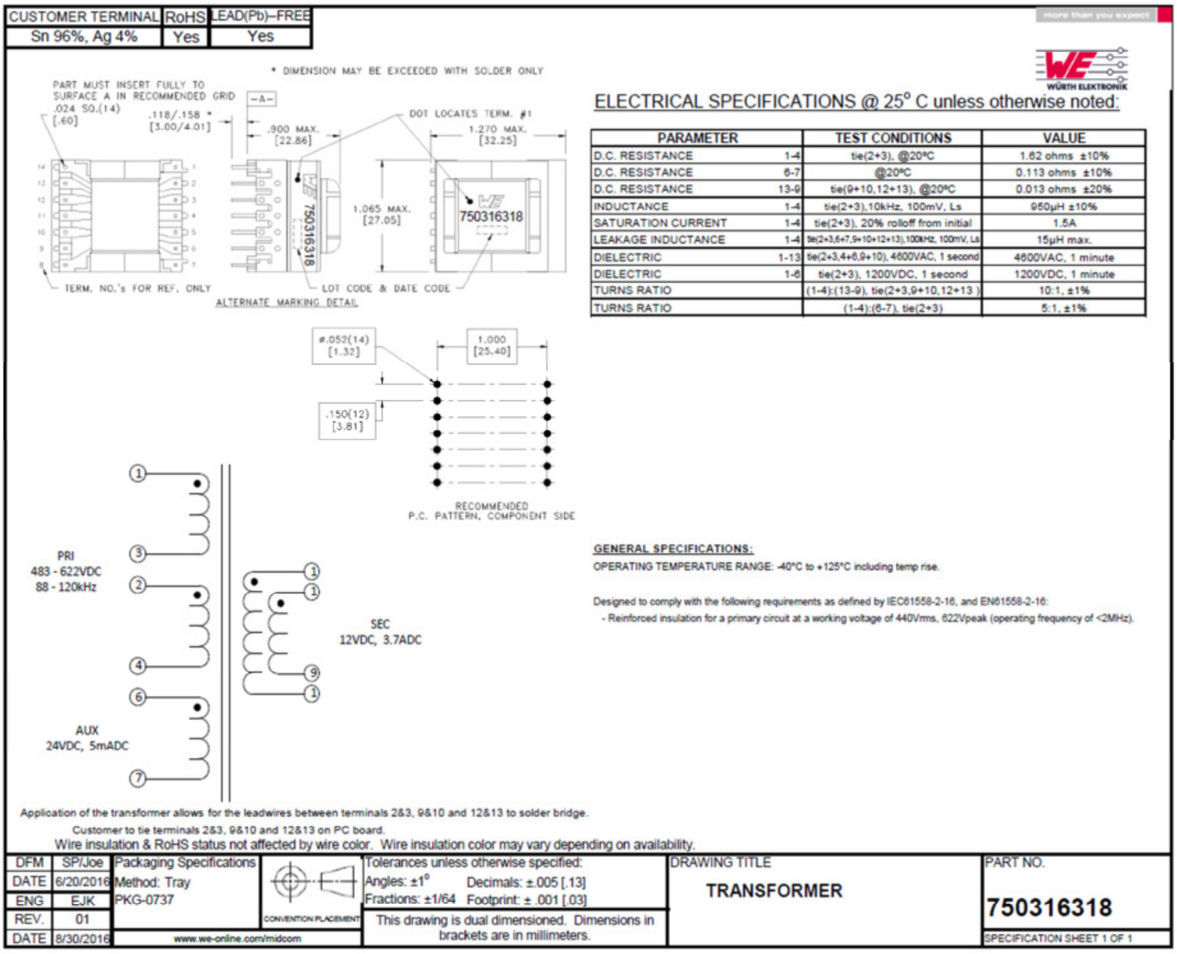
$$L_{p,max} = \frac{1}{\left(\sqrt{\frac{2\cdot P_{out,max}\cdot f_{sw,min}}{\eta}}\left(\frac{1}{V_{DC.MIN}}+\frac{1}{\frac{D_{max}\cdot V_{DC.MIN}}{1-D_{max}}}\right)+\pi\, f_{sw,min}\sqrt{C_{OSS}}\right)^2} \tag{48}$$

$$L_{p,max} = \frac{1}{\left(\sqrt{\frac{2\cdot P_{out,max}\cdot f_{sw,min}}{\eta}}\left(\frac{D_{max}+1-D_{max}}{D_{max}\cdot V_{DC.MIN}}\right)+\pi\, f_{sw,min}\sqrt{C_{OSS}}\right)^2} \tag{49}$$

Finally leading to the desired equation:

$$L_{p,max} = \left(\frac{D_{max}\cdot V_{DC.MIN}}{\sqrt{\frac{2\cdot P_{out,max}\cdot f_{sw,min}}{\eta}}+D_{max}\cdot V_{DC.MIN}\cdot\pi\, f_{sw,min}\sqrt{C_{OSS}}}\right)^2 \tag{50}$$

Appendix B. Transformer datasheet and pictures



ELECTRICAL SPECIFICATIONS @ 25° C unless otherwise noted:

PARAMETER		TEST CONDITIONS	VALUE
D.C. RESISTANCE	1-4	tie(2+3), @20°C	1.62 ohms ±10%
D.C. RESISTANCE	6-7	@20°C	0.113 ohms ±10%
D.C. RESISTANCE	13-9	tie(9+10,12+13), @20°C	0.013 ohms ±20%
INDUCTANCE	1-4	tie(2+3),10kHz, 100mV, Ls	950µH ±10%
SATURATION CURRENT	1-4	tie(2+3), 20% rolloff from initial	1.5A
LEAKAGE INDUCTANCE	1-4	tie(2+3,6+7,9+10+12+13),100kHz, 100mV, Ls	15µH max.
DIELECTRIC	1-13	tie(2+3,4+6,9+10), 4600VAC, 1 second	4600VAC, 1 minute
DIELECTRIC	1-6	tie(2+3), 1200VDC, 1 second	1200VDC, 1 minute
TURNS RATIO		(1-4):(13-9), tie(2+3,9+10,12+13)	10:1, ±1%
TURNS RATIO		(1-4):(6-7), tie(2+3)	5:1, ±1%

GENERAL SPECIFICATIONS:
OPERATING TEMPERATURE RANGE: -40°C to +125°C including temp rise.

Designed to comply with the following requirements as defined by IEC61558-2-16, and EN61558-2-16:
- Reinforced insulation for a primary circuit at a working voltage of 440Vrms, 622Vpeak (operating frequency of <2MHz).

Application of the transformer allows for the leadwires between terminals 2&3, 9&10 and 12&13 to solder bridge.
Customer to tie terminals 2&3, 9&10 and 12&13 on PC board.
Wire insulation & RoHS status not affected by wire color. Wire insulation color may vary depending on availability.

DFM	SP/Joe	Packaging Specifications	Tolerances unless otherwise specified:	DRAWING TITLE	PART NO.
DATE	6/20/2016	Method: Tray	Angles: ±1° Decimals: ±.005 [.13]	TRANSFORMER	750316318
ENG	EJK	PKG-0737	Fractions: ±1/64 Footprint: ± .001 [.03]		
REV.	01		This drawing is dual dimensioned. Dimensions in brackets are in millimeters.		
DATE	8/30/2016	www.we-online.com/midcom			SPECIFICATION SHEET 1 OF 1

Fig. B.1 – Datasheet of the constructed Flyback transformer.

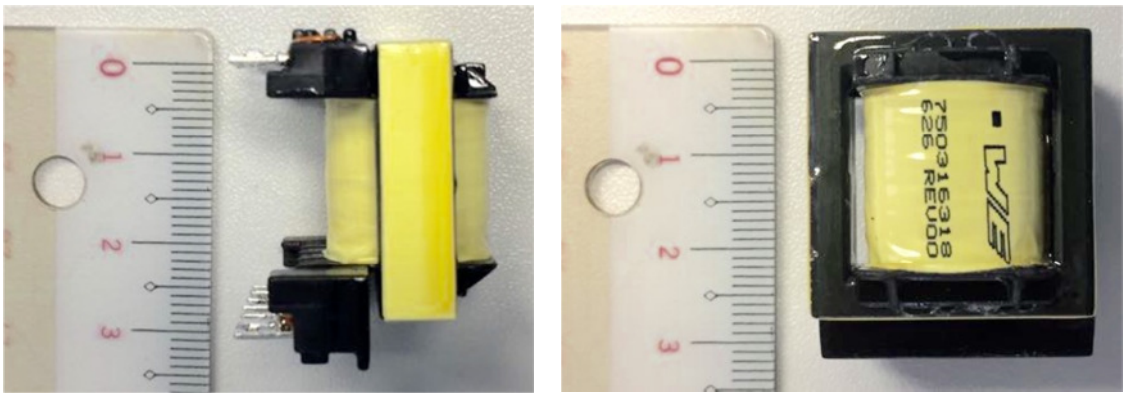


Fig. B.2 – Side view (left) and top view (right) of the Flyback transformer.

Appendix C. Bill of Materials

Name	Value	Description	Producer	Producer Code	Assembled
C4, C17, C18, C23	---	----	----	---	**No**
C6, C8	100 uF	Electrolytic capacitor 100uF 450V	NICHICON	UCY2W101MHD	**Yes**
C9, C15	47 pF	Ceramic Cap 0805 47pF 10% 50V COG	WURTH	885012007055	**Yes**
C10	22 uF	Electrolytic capacitor 22uF 50V	WURTH	860040672001	**Yes**
C11	2.2 uF	Ceramic cap 0805 2.2uF 35V X7R TDK	TDK	C2012X7R1V225K085AC	**Yes**
C11A, C22	100nF	Ceramic cap 0805 100nF 50V X7R	WURTH	885012207098	**Yes**
C12, C13	2.2 nF	Ceramic cap 2.2nF 1kV	TDK	CK45-B3AD222KYNNA	**Yes**
C16	2.2 nF	Ceramic cap 0805 2.2nF 50V X7R	WURTH	885012207088	**Yes**
C19, C20	470 uF	Electrolytic cap 470uF 35V	WURTH	860080575017	**Yes**
C21	---	----	----	---	**No**
D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12	S1M-E3/61T	Rectifier Diode S1M Vishay	VISHAY	S1M-E3/61T	**Yes**
D13	---	Fast Diode 400V 1A	ROHM	RF101L4S	**Yes**
D14, D16	---	Schottky Diode 60V 1A	ROHM	RB160M-60	**Yes**
D15, D15B	---	----	----	---	**No**
D17	---	Zener Diode 20V 1W	ROHM	KDZVTR20B	**No**
D18	---	Ultrafast Diode 1200V 1A	STM	STTH112RL	**Yes**
D19	---	Zener Diode 24V 1W	ROHM	KDZVTR24B	**Yes**
D20	---	Schottky Barrier Diode 200V 30A	SANGDEST	MBRF30200CT	**Yes**
D20B	---	----	----	---	**No**
D21	---	SML-A12P8T Side LED Green 20mA	ROHM	SML-A12P8T	**Yes**
D22	0 Ohm	Resistor 0 Ohm 0805 footprint	ROHM	MCR10EZPJ000	**Yes**
D22 (ASC)	---	Schottky Diode 60V 1A	ROHM	RB160M-60	**No**
H1	---	Heatsink for TO220 Transistor	AAVID THERMALLOY	574602B03700G	**Yes**
H2	---	Heatsink for TO247 Transistor	OHMITE	WA-T247-101E	**No**
J5, J6	---	Connector pitch 10.16mm Horiz. Entry	Wurth	691 219 610 002	**Yes**
J7	---	Header connector male pitch 2,54mm	3M	961102-6404-AR	**Yes**
J21	---	Connector pitch 5mm Horiz. Entry	Wurth	691102710002	**Yes**
Q1	---	1700V 3,7A SIC MOSFET	ROHM	SCT2H12NZ	**Yes**
Q2	---	NPN transistor 50V 0.5A	ROHM	2SD1484KT146R	**No**
Q3	---	500V 800mA normally on MOSFET	IXYS	IXTY08N50D2	**No**
R1, R2, R3	3.15 A	Fuse 3.15A 250V	Littelfuse	4001315	**Yes**
R4, R4B, R6, R6B, R7, R8, R9, R10	470 kOhm	Resistor 470kOhm 1206 footprint	ROHM	MCR18ERTF4703	**Yes**
R11	10 kOhm	Resistor 10kOhm 0805 footprint	ROHM	MCR10ERTF1002	**Yes**
R12A, R13A, R14A, R35, R39	0 Ohm	Resistor 0 Ohm 0805 footprint	ROHM	MCR10EZPJ000	**No**
R16	4.7 kOhm	Resistor 4.7kOhm 0805 footprint	ROHM	MCR10ERTF4701	**Yes**
R17	330 k	Resistor 330 KOhm 2W VISHAY	VISHAY	PR02000203303JR500	**Yes**

Name	Value	Description	Producer	Producer Code	Assembled
R17	330 k	Resistor 330 KOhm 2W VISHAY	VISHAY	PR02000203303JR500	**Yes**
R18	100 Ohm	Resistor 100 Ohm 0805 footprint	ROHM	MCR10ERTF1000	**Yes**
J21	---	Connector pitch 5mm Horiz. Entry	Wurth	691102710002	**Yes**
Q1	---	1700V 3,7A SIC MOSFET	ROHM	SCT2H12NZ	**Yes**
Q2	---	NPN transistor 50V 0.5A	ROHM	2SD1484KT146R	**No**
Q3	---	500V 800mA normally on MOSFET	IXYS	IXTY08N50D2	**No**
R1, R2, R3	3.15 A	Fuse 3.15A 250V	Littelfuse	4001315	**Yes**
R4, R4B, R6, R6B, R7, R8, R9, R10	470 kOhm	Resistor 470kOhm 1206 footprint	ROHM	MCR18ERTF4703	**Yes**
R11	10 kOhm	Resistor 10kOhm 0805 footprint	ROHM	MCR10ERTF1002	**Yes**
R12A, R13A, R14A, R35, R39	0 Ohm	Resistor 0 Ohm 0805 footprint	ROHM	MCR10EZPJ000	**No**
R16	4.7 kOhm	Resistor 4.7kOhm 0805 footprint	ROHM	MCR10ERTF4701	**Yes**
R17	330 k	Resistor 330 KOhm 2W VISHAY	VISHAY	PR02000203303JR500	**Yes**
R18	100 Ohm	Resistor 100 Ohm 0805 footprint	ROHM	MCR10ERTF1000	**Yes**
R19	10 Ohm	Resistor 10 Ohm 0805 footprint	ROHM	MCR10ERTF10R0	**Yes**
R20	47 kOhm	Resistor 47kOhm 0805 footprint	ROHM	MCR10ERTF4702	**Yes**
R21, R21A	3 Ohm	Resistor footprint 1020 Wide	ROHM	LTR50UZPF3R00	**Yes**
R21B	6.8 Ohm	Resistor footprint 1020 Wide	ROHM	LTR50UZPF6R80	**Yes**
R22, R38	0 Ohm	Resistor 0 Ohm 0805 footprint	ROHM	MCR10EZPJ000	**Yes**
R23	120 kOhm	Resistor 120kOhm 0805 footprint	ROHM	MCR10ERTF1203	**Yes**
R24, R30	12 kOhm	Resistor 12kOhm 0805 footprint	ROHM	MCR10ERTF1202	**Yes**
R25	300 Ohm	Resistor 300Ohm 0805 footprint	ROHM	MCR10ERTF3000	**Yes**
R26, R37	1kOhm	Resistor 1kOhm 0805 footprint	ROHM	MCR10ERTF1001	**Yes**
R27	15kOhm	Resistor 15kOhm 0805 footprint	ROHM	MCR10ERTF1502	**Yes**
R28	180kOhm	Resistor 180kOhm 0805 footprint	ROHM	MCR10ERTF1803	**Yes**
R29	51kOhm	Resistor 51kOhm 0805 footprint	ROHM	MCR10ERTF5102	**Yes**
R31	---	----	----	---	**No**
R34	4.7kOhm	Resistor 4.7kOhm 0805 footprint	ROHM	MCR10ERTF4701	**No**
R36	10kOhm	Resistor 10kOhm 0805 footprint	ROHM	MCR10ERTF1002	**No**
T1	---	FLyback Transformer	WURTH	750316318	**Yes**
U1	---	ACDC flyback driver for SIC MOSFET	ROHM	BD7682	**Yes**
U2	---	5kV Optocoupler	SHARP	PC817XNNIP0F	**Yes**
U3	---	Voltage reference 2.49V	TI	TL431AIDBZR	**Yes**

Appendix D. AUX Board layout

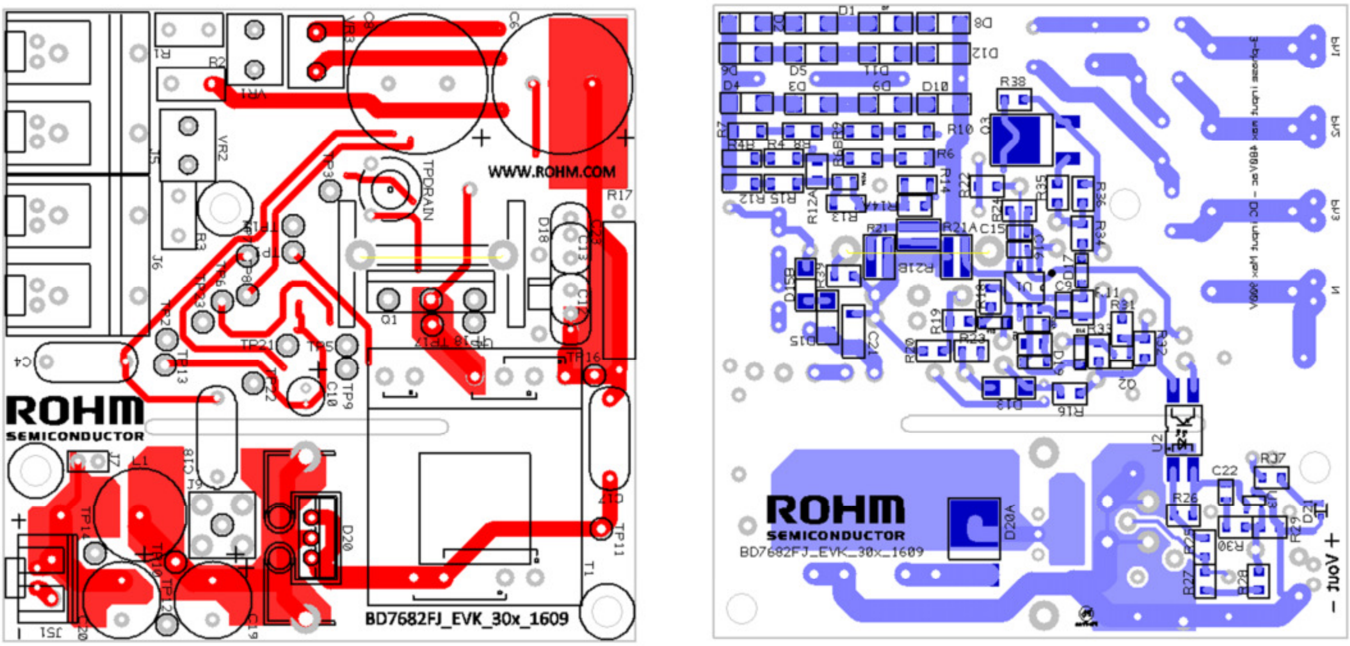


Fig. D.1 – Layout of top side (left) and bottom side (right) of the AUX board.

Appendix E. Alternative Start-up Circuitry

This section presents an alternative start-up circuitry (ASC) for the AUX board. It aims to reduce the start-up time, avoiding at the same time extra losses coming from the start-up resistor divider. The working principle of the ASC is depicted in Fig. E.1.

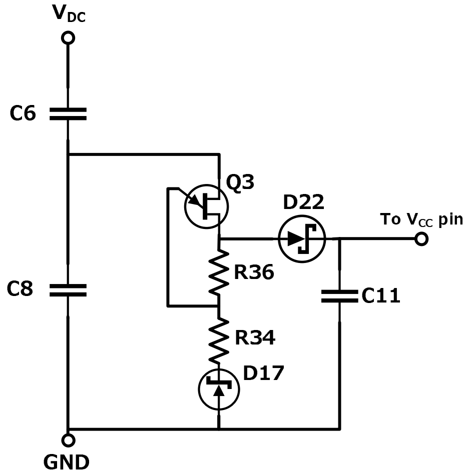


Fig. E.1 – Work principle of the alternative start-up circuitry (ASC).

During start-up a current flows from input capacitor **C8** through the depletion mode MOSFET **Q3** (normally-on). This current will charge the V_{CC} capacitor **C11**. The gate pin of **Q3** is connected in the middle of the resistor divider formed by **R36** and **R34**. As the voltage over **C11** increases, the gate voltage of **Q3** becomes negative with respect to its source voltage. When threshold voltage of **Q3** is achieved, it turns off. Resistors **R36** and **R34**, and Zener diode **D17** are dimensioned so that V_{CC} achieves the minimum value (UVLO) for the controller to start. From this point, controller will be fed by the auxiliary winding, and **Q3** will stay off until the next start-up. Diode **D22** is placed to avoid losses through **R36** and **R34** after start-up.

The dimensioning of ASC starts from the choice of the MOSFET **Q3**. Since silicon FETs rated for 900 V are not available, **Q3** is connected to the middle point between the input capacitors **C6** and **C8**. This enables the MOSFET to be rated to 500 V. The recommended part is IXTY08N50D2, from IXYS. According to datasheet, the threshold voltage has minimum and maximum levels of -4 V and -2 V, respectively. The minimum V_{CC} voltage for the controller to start is $UVLO$ = 20 V (max), and the overvoltage protection of V_{CC} is OVP = 27.5 V (min).

During start-up, the voltage over resistor **R36** is the voltage between gate and source of **Q3**. By setting **R36** = 10 kΩ:

$$R36 \cdot i_{R36} < 2\,V \; only \; if \; V_{C11} > 19.5\,V \rightarrow i_{R36} < 0.2\,mA \; for \; V_{C11} = 19.5\,V \tag{51}$$

$$R36 \cdot i_{R36} > 4\,V \; only \; if \; V_{C11} < 27.5\,V \rightarrow i_{R36} > 0.4\,mA \; for \; V_{C11} = 27.5\,V \tag{52}$$

By using a 20 V Zener diode as **D17**, the first condition is automatically satisfied.

For the second condition, the current through **R36** can be calculated as:

$$i_{R36} = \frac{V_{C11} + V_{D22} - V_{D17}}{R36 + R34} \tag{53}$$

Which leads to:

$$R34 < \frac{27.5\,V + 0.3\,V - 20V}{0.4\,mA} - 10\,k\Omega \rightarrow R34 < 9.5\,k\Omega \quad (54)$$

Chosen value for **R34** = 4.7 kΩ.

Fig. E.2 presents the waveforms of the start-up of the AUX board, done by standard configuration and with ASC. It is possible to observe that the start-up time is reduced by a factor of 100. Moreover, since the start-up resistive divider is not used in ASC, the losses caused by those resistors are not present in the ASC configuration

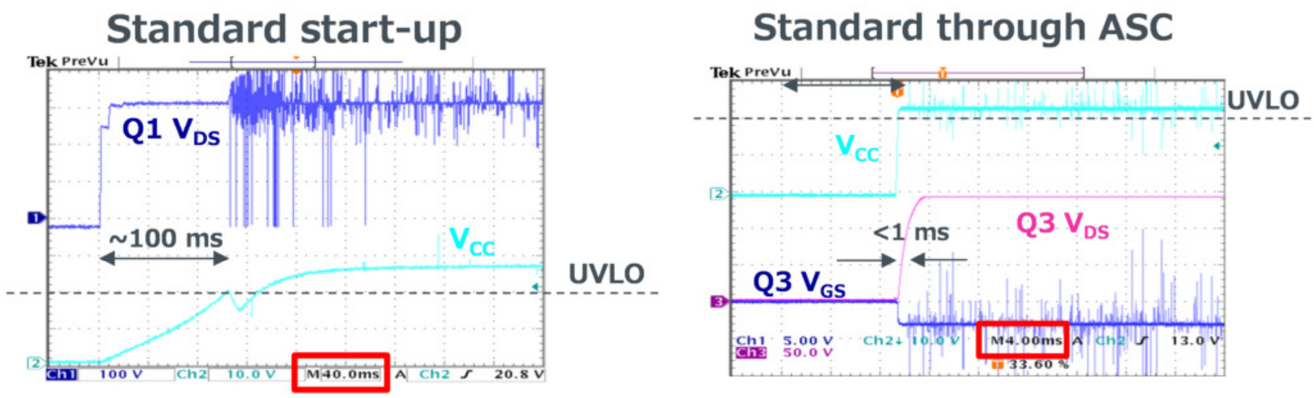


Fig. E.2 – Schematics of the AUX board with alternative start-up circuitry (ASC).

The full schematic of AUX board with implemented ASC is depicted in Fig. E.3. Devices different from original schematics are drawn in a different color. Please note they are not assembled in the original board. However, their respective footprints are present on the board, assuming the devices given in the bill of materials list – see Appendix C.

In addition to extra components, the resistors **R38** and **R12** must be removed. Finally, before **D22** is placed, the originally soldered 0 Ω resistor must be removed.

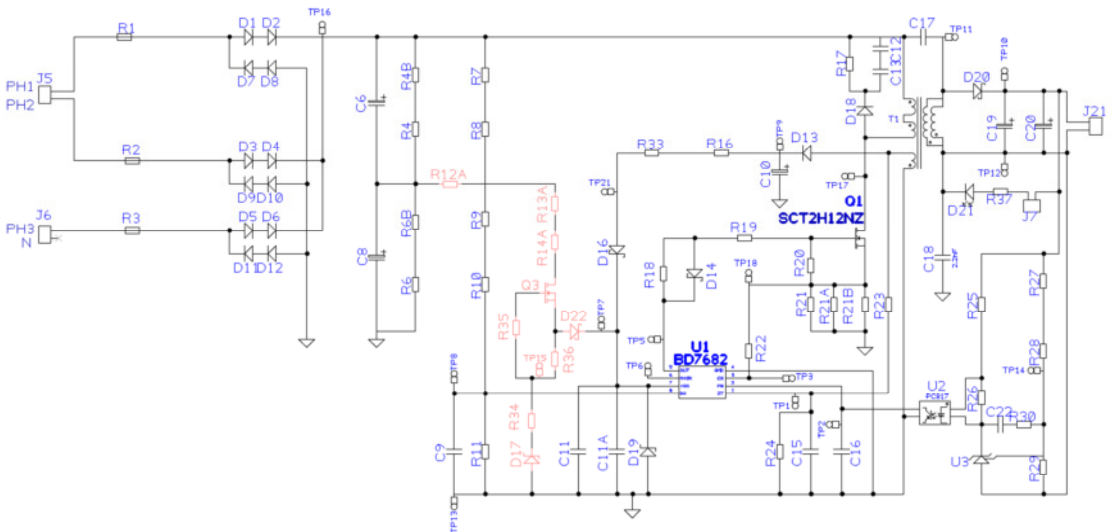


Fig. E.3 – Schematics of the AUX board with alternative start-up circuitry (ASC).

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■<High Voltage Safety Precautions>

◇ Read all safety precautions before use

Please note that this document covers only the BD7682FJ-LB evaluation board (BD7682FJ-EVK-301) and its functions. For additional information, please refer to the datasheet.

To ensure safe operation, please carefully read all precautions before handling the evaluation board

Depending on the configuration of the board and voltages used,

Potentially lethal voltages may be generated.

Therefore, please make sure to read and observe all safety precautions described in the red box below.

Before Use

[1] Verify that the parts/components are not damaged or missing (i.e. due to the drops).
[2] Check that there are no conductive foreign objects on the board.
[3] Be careful when performing soldering on the module and/or evaluation board to ensure that solder splash does not occur.
[4] Check that there is no condensation or water droplets on the circuit board.

During Use

[5] Be careful to not allow conductive objects to come into contact with the board.
[6] **Brief accidental contact or even bringing your hand close to the board may result in discharge and lead to severe injury or death.**
Therefore, DO NOT touch the board with your bare hands or bring them too close to the board.
In addition, as mentioned above please exercise extreme caution when using conductive tools such as tweezers and screwdrivers.
[7] If used under conditions beyond its rated voltage, it may cause defects such as short-circuit or, depending on the circumstances, explosion or other permanent damages.
[8] Be sure to wear insulated gloves when handling is required during operation.

After Use

[9] The ROHM Evaluation Board contains the circuits which store the high voltage. Since it stores the charges even after the connected power circuits are cut, please discharge the electricity after using it, and please deal with it after confirming such electric discharge.
[10] Protect against electric shocks by wearing insulated gloves when handling.

This evaluation board is intended for use only in research and development facilities and should by handled **only by qualified personnel familiar with all safety and operating procedures.**
We recommend carrying out operation in a safe environment that includes the use of high voltage signage at all entrances, safety interlocks, and protective glasses.