1-4 cells
Li-ion battery manager charging application note
BD99954MWV，BD99954GW

This document describes the BD99954 (used in this document as a combined expression of BD99954MWV and BD99954GW), including the IC design concept, peripheral application circuit constants to be considered, and necessary register settings. In addition, some phenomena that are likely to be encountered and workarounds will also be described. For default values and recommended settings of registers related to basic functions, please refer to "Li-ion Battery Manager Quick Reference" as well.

Features

- Dual Source Battery Charger
- 1-4 Cell Li-ion / Li-polymer Battery High Efficiency Step-up / Step-down Switching Charger
- Two separate input sources for USB-VBUS and DC adapter
- Two port BC1.2 detectors
- JEITA compliant charging profile
- Programmable parameters for Preconditioning, Pre-charge current, and Fast-charge current
- Programmable charging Voltage
- Programmable charge current
- Programmable Switching Frequency: 600kHz to 1.2MHz
- Support USB BCS 1.2, ACA, ID pin, OTG
- USB-VBUS Over Voltage Protection
- Over Voltage Battery Protection
- Battery Short Circuit Detection
- Power Path Management with charge pump gate driver
- Battery FET Power Path Control
- Reverse Buck/Boost Option for USB/USB-PD
- Supports thermistor temperature detection function
- Thermistor temperature monitoring function.
- IMVP8 support
- Auto charging function
- Battery Learn function
- Input voltage range: 3.8V to 25V
- SMBus interface

Applications

- Ultrabook
- Notebook PC
- Ultra-Mobile PC
- Tablet PC

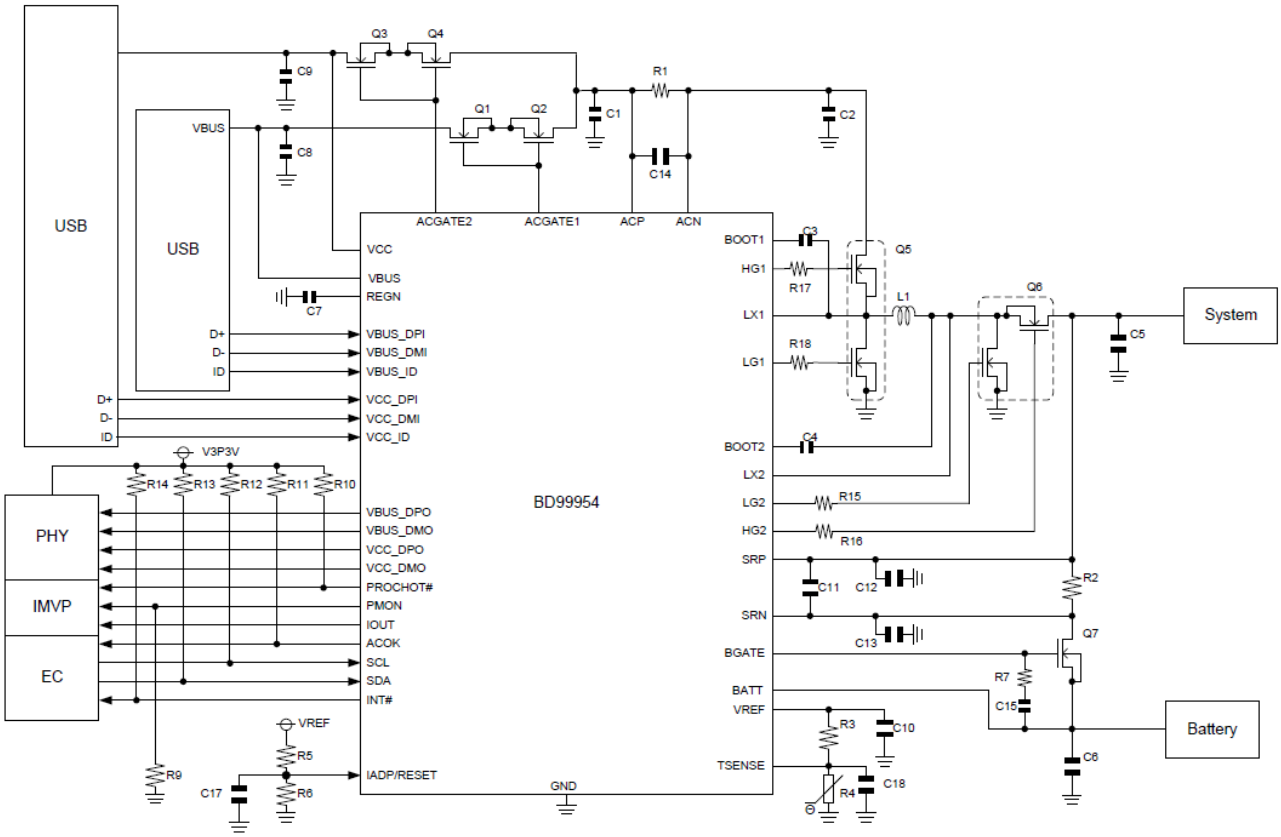

Figure 1. Application circuit

Related Materials

Data Sheet BD99954MWV/GW datasheet Rev.001

Contents

1 IC Design Concept

1 - 1 Mainly 2S (cell), expanded to support 1-4S (cell)

Due to OTP loading, the default value of the register is representative of two cells. To support other cell numbers, the register needs to be rewritten to a value appropriate for the battery used.

1 - 2 Adopt an architecture that avoids power supply conflicts

The BD99954 has three externally supplied voltages, VBUS, VCC and VBATT. The architecture of the BD99954 is such that these voltages do not conflict with the peripheral circuits including the IC. The BD99954 is designed in such a way that these voltages do not conflict with the peripheral circuits including the IC.

1 - 3 Supports semi-standalone operation

The BD99954 does not support stand-alone operation, such as starting charging autonomously when power is supplied. However, once charging is started with the appropriate register settings, the BD99954 can manage the charging state by itself, including transition to fast charging, charging termination current detection, full charge detection, and recharge start.

1 - 4 JEITA temperature profile compatible

When equipped with a thermistor, it is possible to support (JEITA) temperature profiles for safety reasons.

1 - 5 Battery Charger 1.2 Specification (BC1.2) Support

It has two ports of BC1.2 port detection and input current limit function according to it.

2 Application Settings

This section describes the flowchart for judging whether the BD99954 can be used or not, and the flowchart for setting the registers according to the application. For detailed explanation of the setting method, chapters are listed in the flowchart. Clicking on the underlined blue text will take you to the linked chapter.

2 - 1 Flowchart for use (package, input voltage range)

The following is a flowchart for determining whether or not BD99954 can be used.

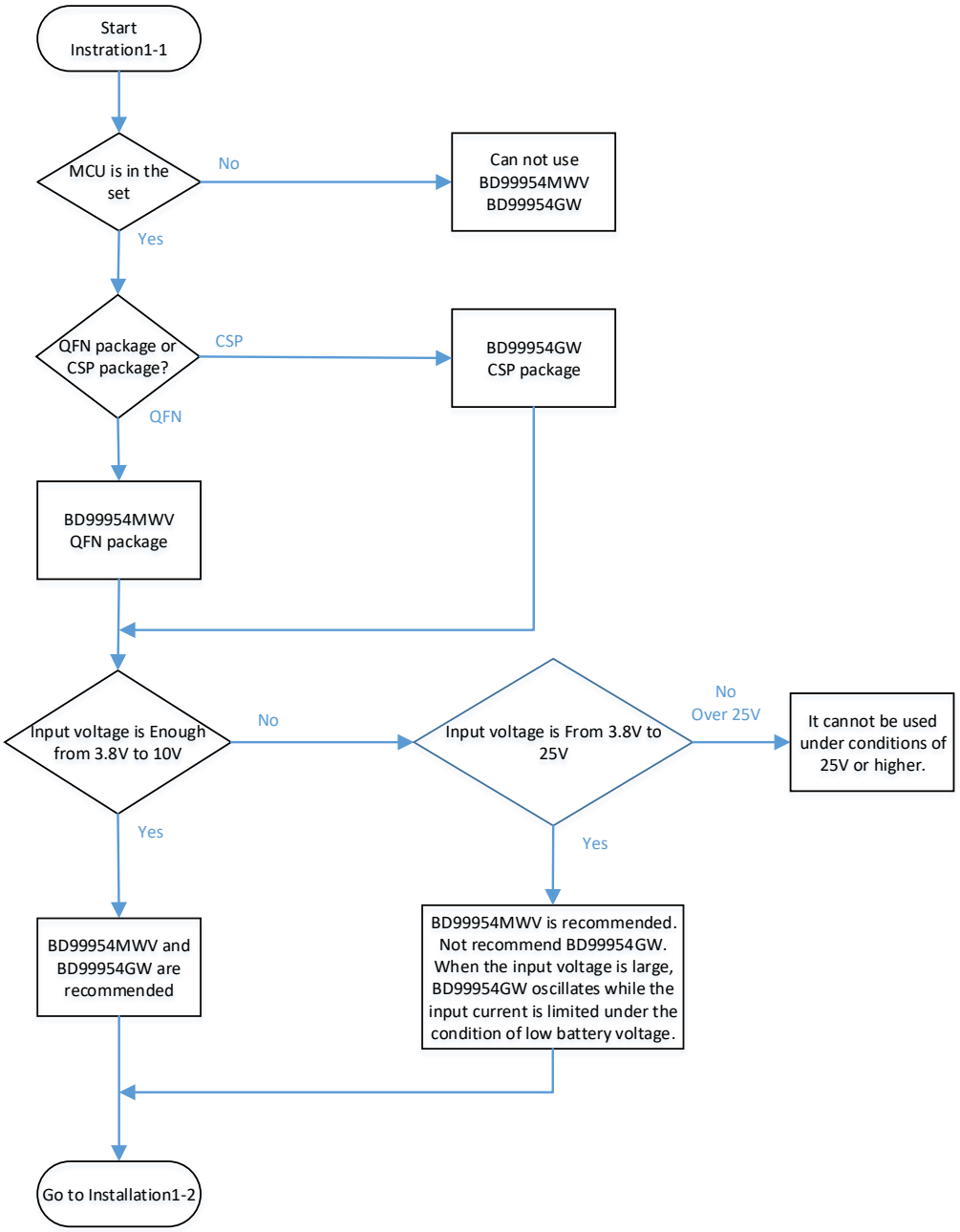

Figure 2-1. BD99954MWV/BD99954GW Selection Flowchart (Package, Input Voltage Range)

2 - 2 Flowchart for use (Input current, Termination current, IMVP8, Reverse current protection)

The following is a flowchart for determining whether or not BD99954 can be used.

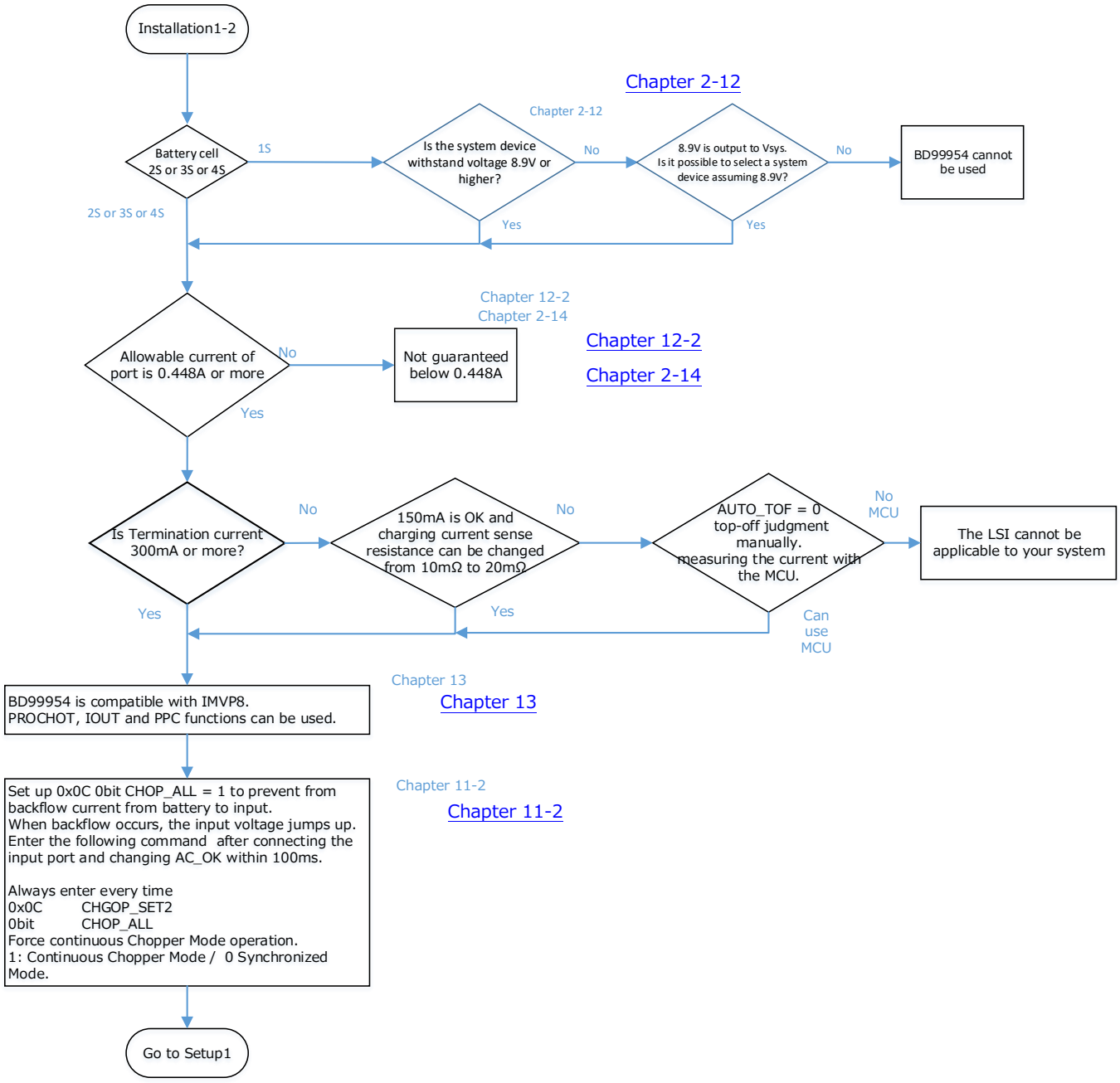

Figure 2-2. Flowchart of BD99954MWV/BD99954GW selection
(Input current, Termination current, IMVP8, Reverse current protection)

2 - 3 Flowchart of Setup1 register setting (VCC and VBUS priority and number of battery cells)

The flowchart for setting the priority of the input ports of VCC and VBUS and the register setting for the number of battery cells is shown below.

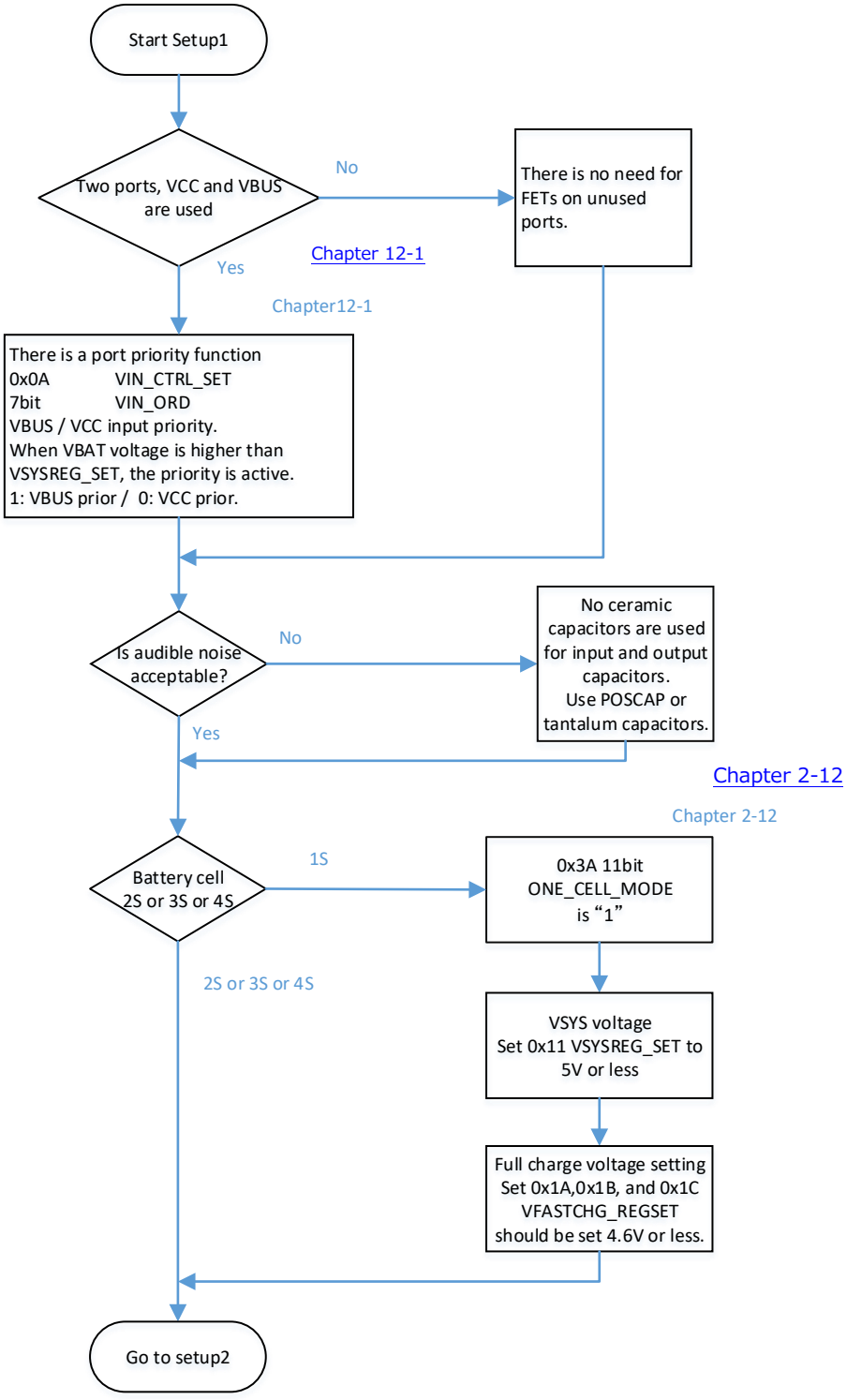

Figure 2-3. Selection Flowchart by Number of Battery Cells

2 - 4 Flowchart of Setup2 Register Settings (Termination Current, Charge Current, Charge Voltage Settings)

The flowchart of the register settings for the termination current, charge current, and charge voltage is shown below.

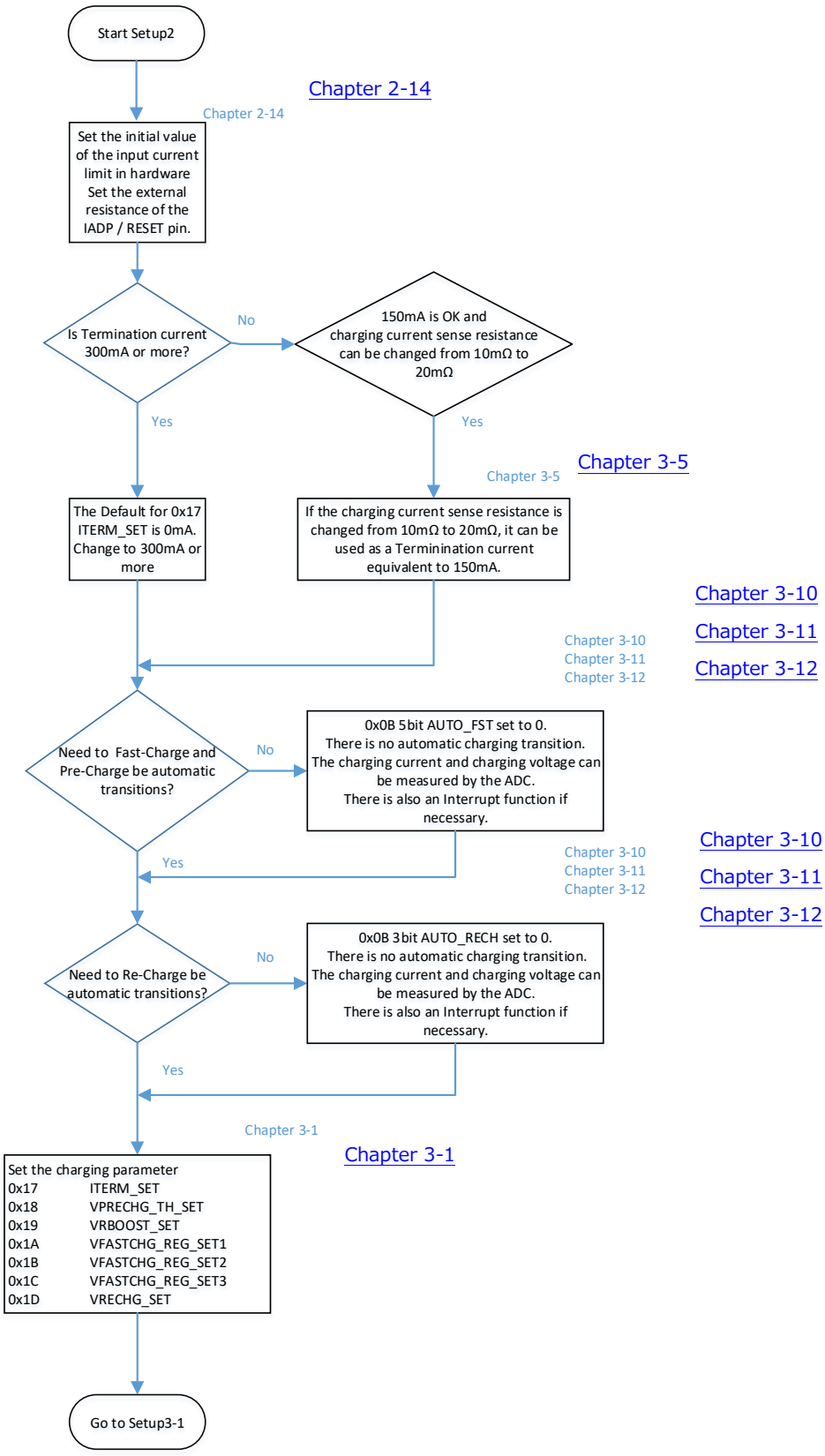

Figure 2-4. Flowchart of charging setup

2 - 5 Setup3-1 Flowchart of register setting (BC1.2, USB port detection)

The flowchart of the register settings for BC1.2 USB port detection for VCC and VBUS input ports is shown below.

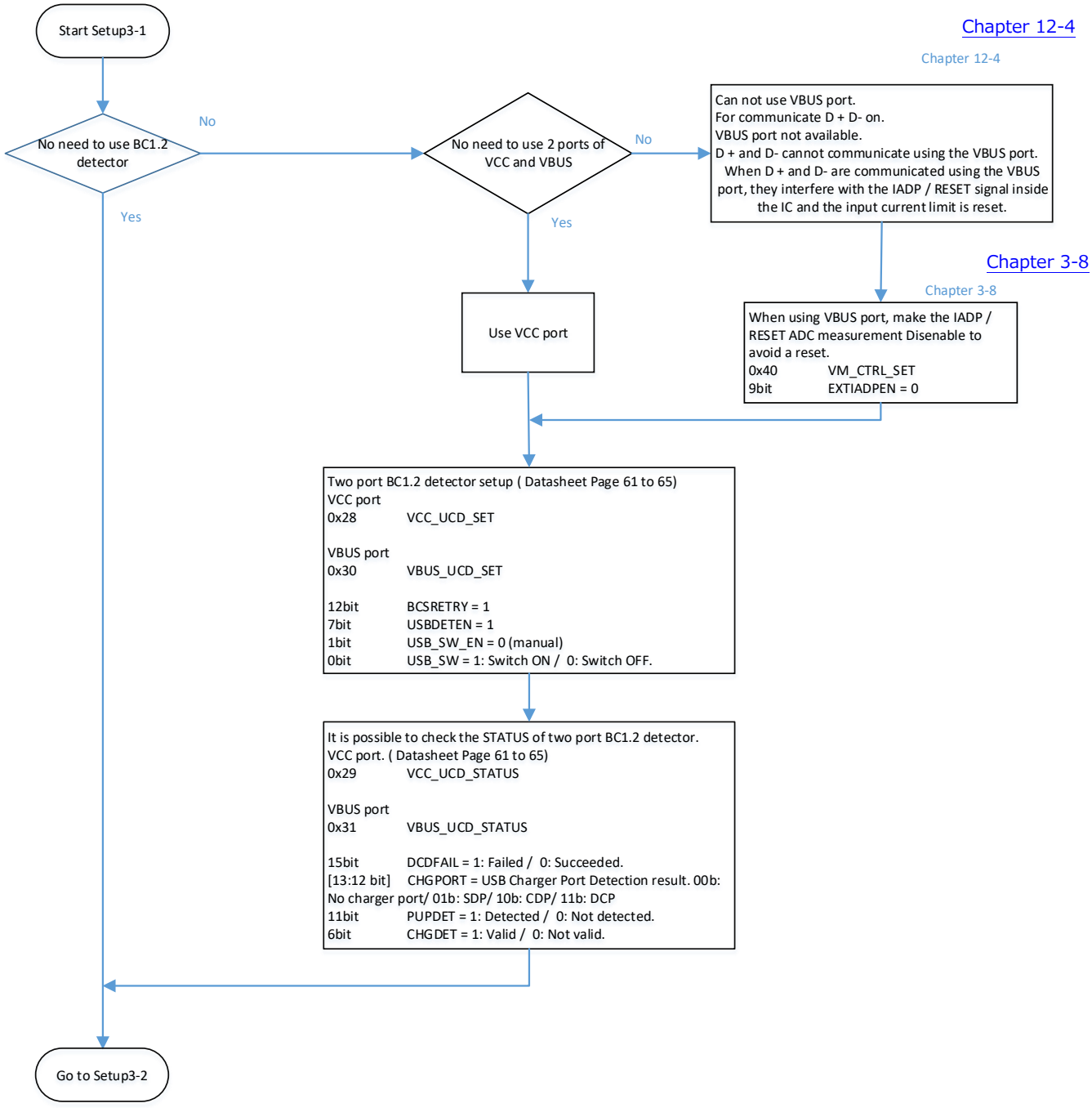

Figure 2-5. Flowchart of BC 1.2 configuration

2 - 6 Setup3-2 Flowchart of register setting (BC1.2, USB ID detection)

The flowchart of the register settings for BC1.2 USB port ID detection for VCC and VBUS input ports is shown below.

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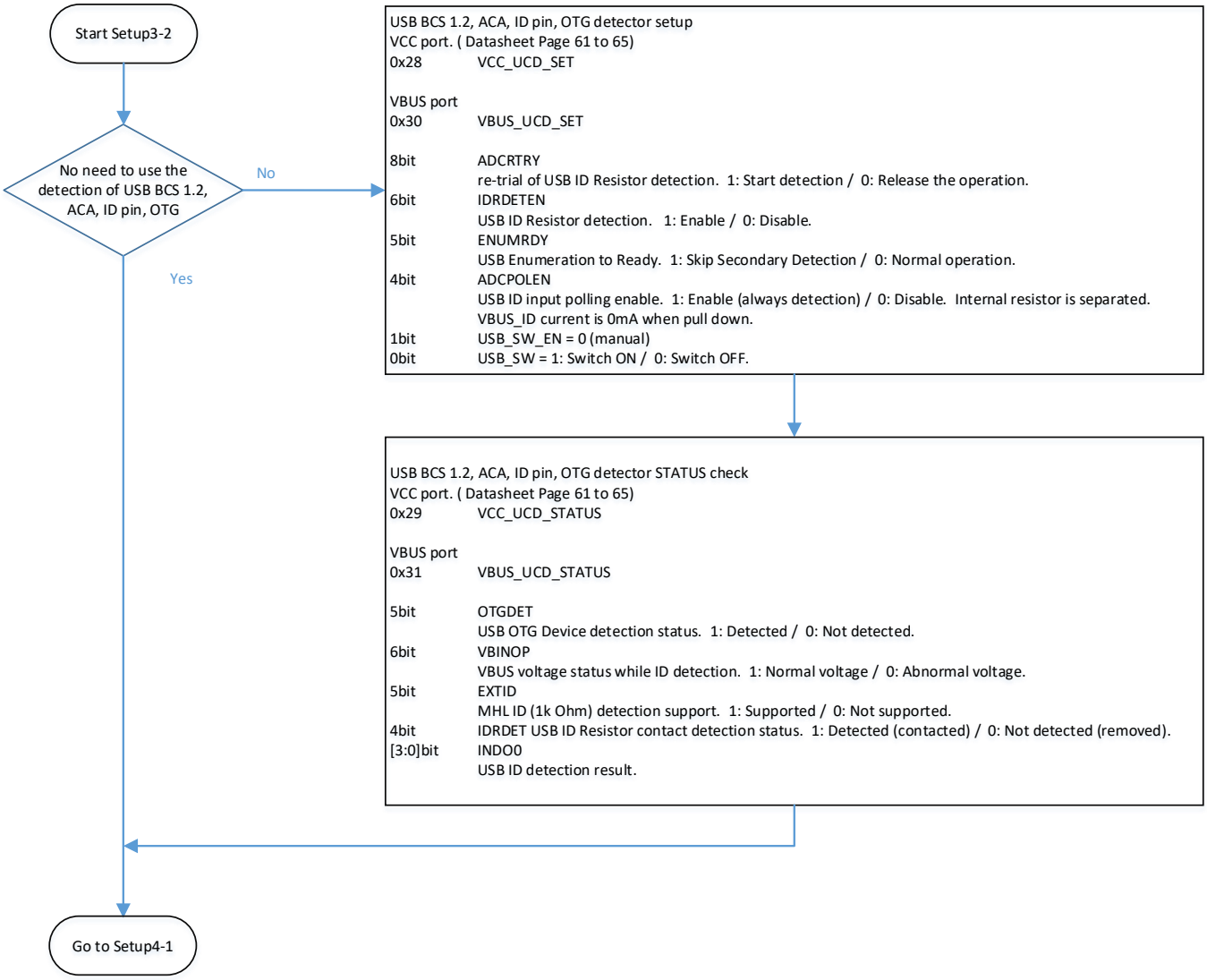


Figure 2-6. BC 1.2 Flowchart of ID detection setting

2 - 7 Setup4-1 Flowchart of register setting (JEITA profile setting)

The flowchart of register setting regarding JEITA profile setting is shown below.

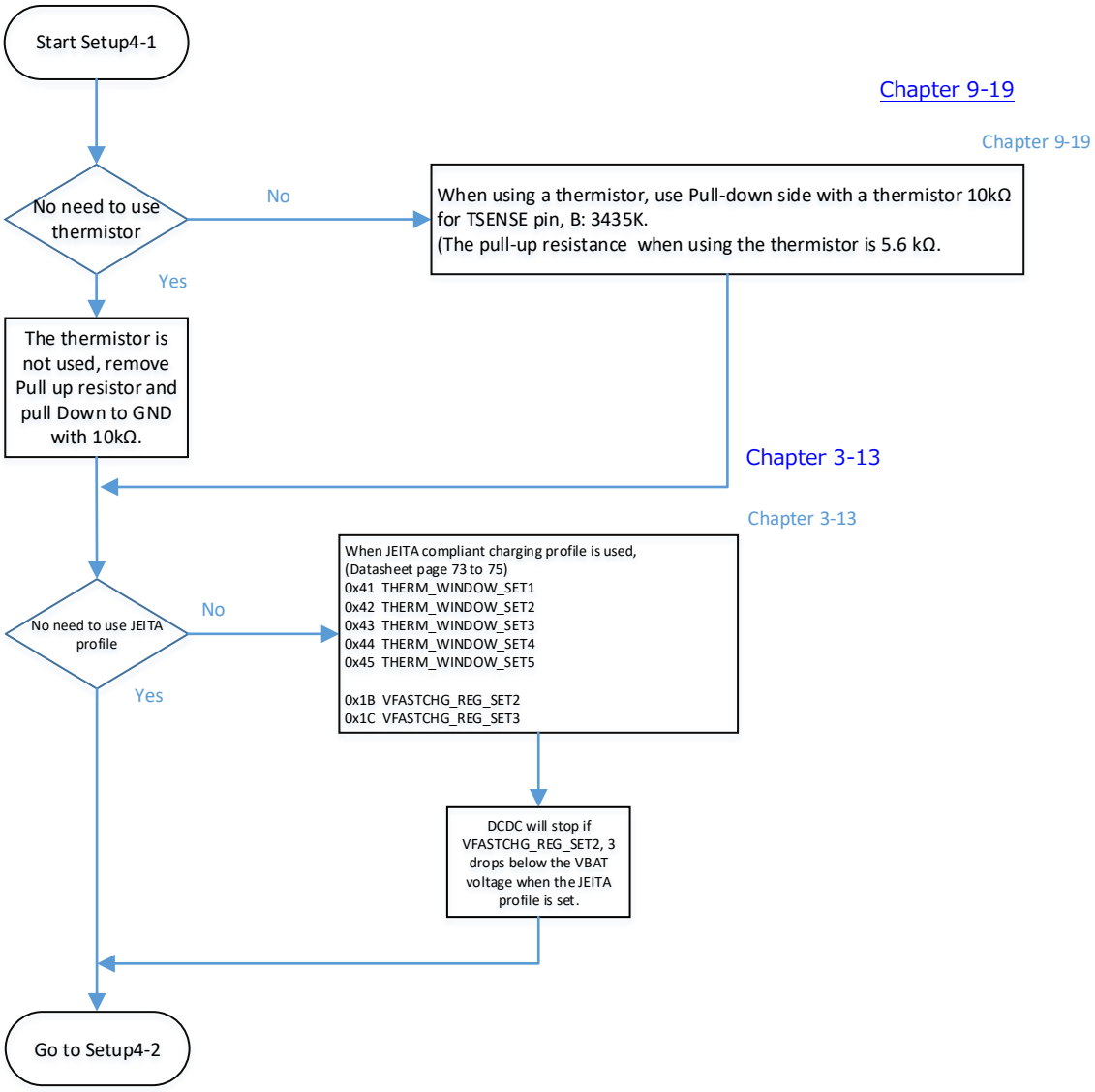


Figure 2-7. Flowchart of JEITA profile setting

2 - 8 Flowchart of Setup4-2 register settings continued (IMVP8, PROCHOT, PMOM settings)

The flowchart of register settings for IMVP8, PROCHOT, and PMOM settings is shown below.

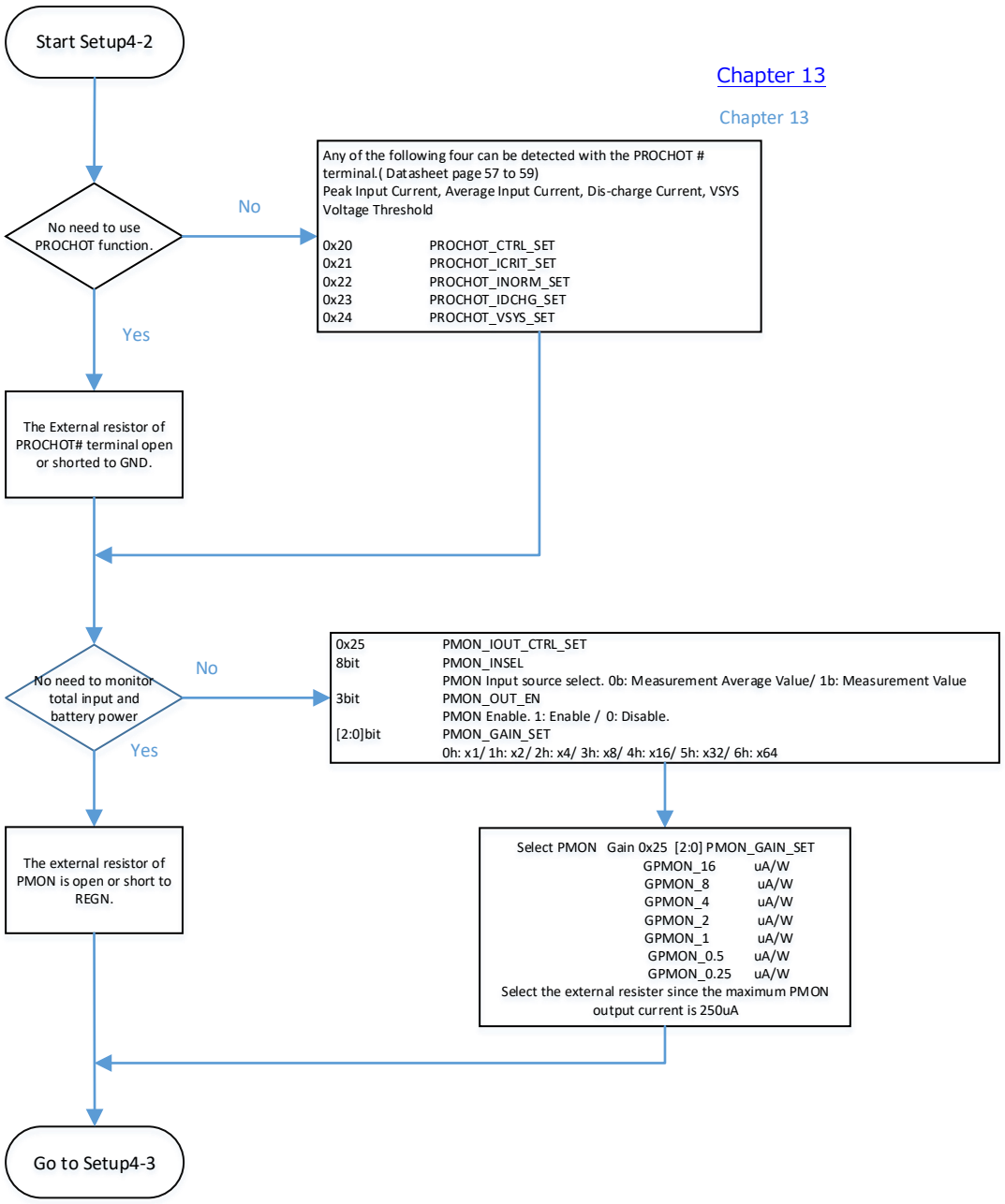


Figure 2-8. Flowchart of IMVP8, PROCHOT and PMON settings

2 - 9 Flowchart of Setup4-3 Register Settings continued (IMVP8, IOUT settings)

The flowchart of register settings for IMVP8 and IOUT settings is shown below.

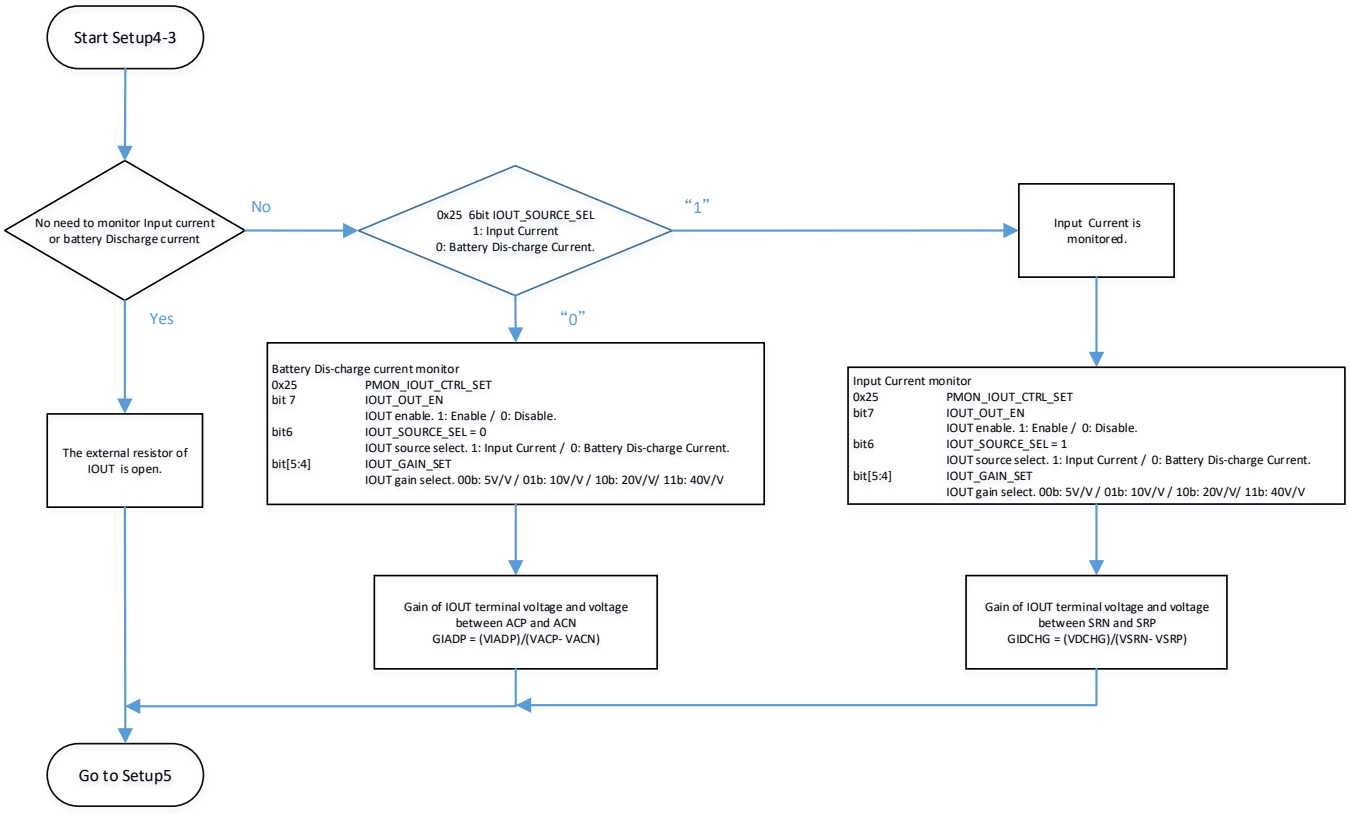


Figure 2-9. Flowchart of IMVP8 IOUT setting

2 - 10 Flowchart of Setup5 register setting (VBAT learn, Operation Frequency, Power save mode setting)

The flowchart of register settings for VBAT learn, Operation Frequency, and Power save mode settings is shown below.

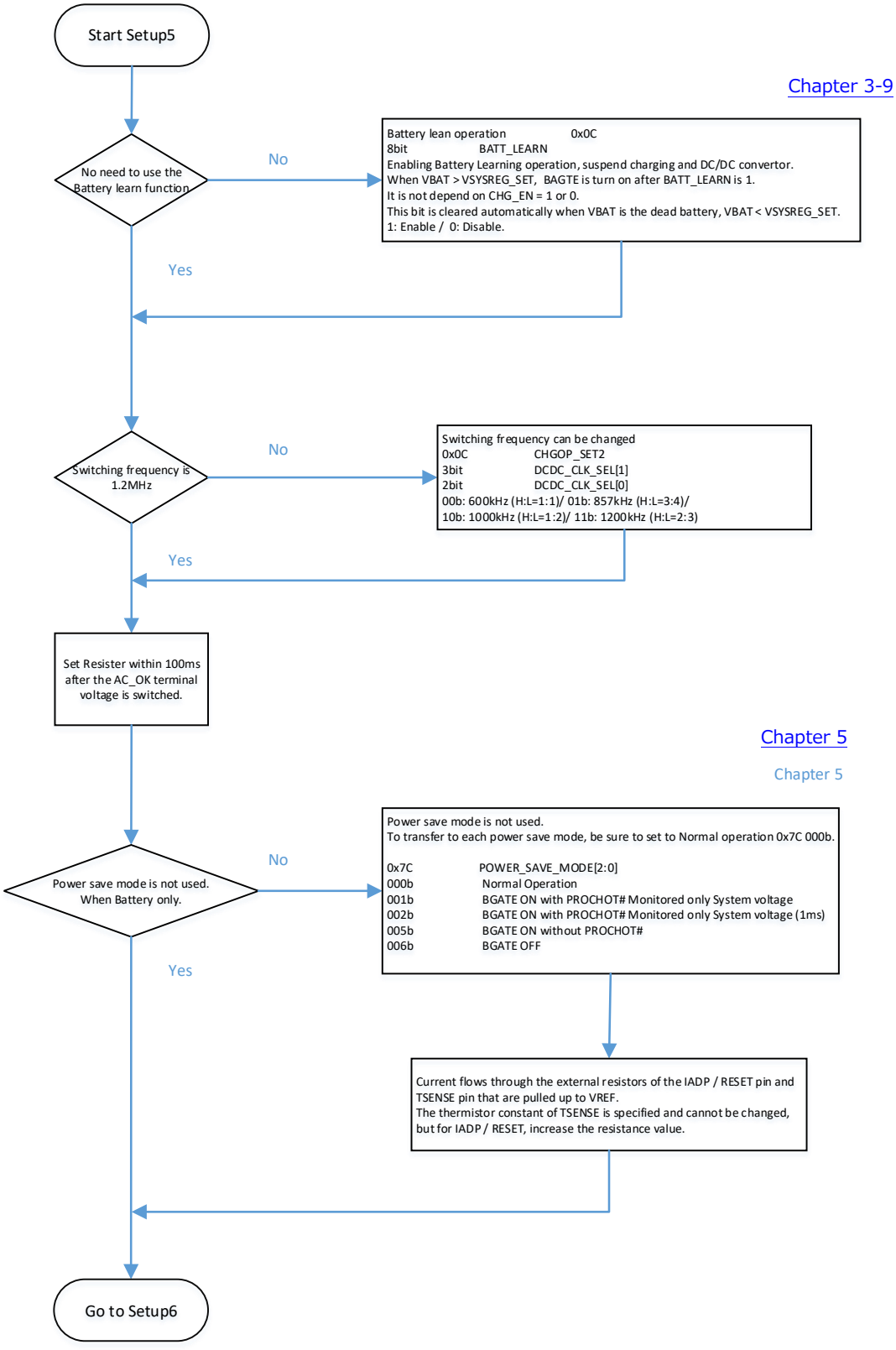


Figure 2-10. Flowchart of VBAT learn, Operating Frequency, and Power save mode settings

2 - 11 Setup6 Flowchart of external component selection and layout pattern design

The flowchart below shows the component selection and layout pattern notes for MOSFET, inductor, the input current detection circuit of ACP ACN and charge current detection circuit.

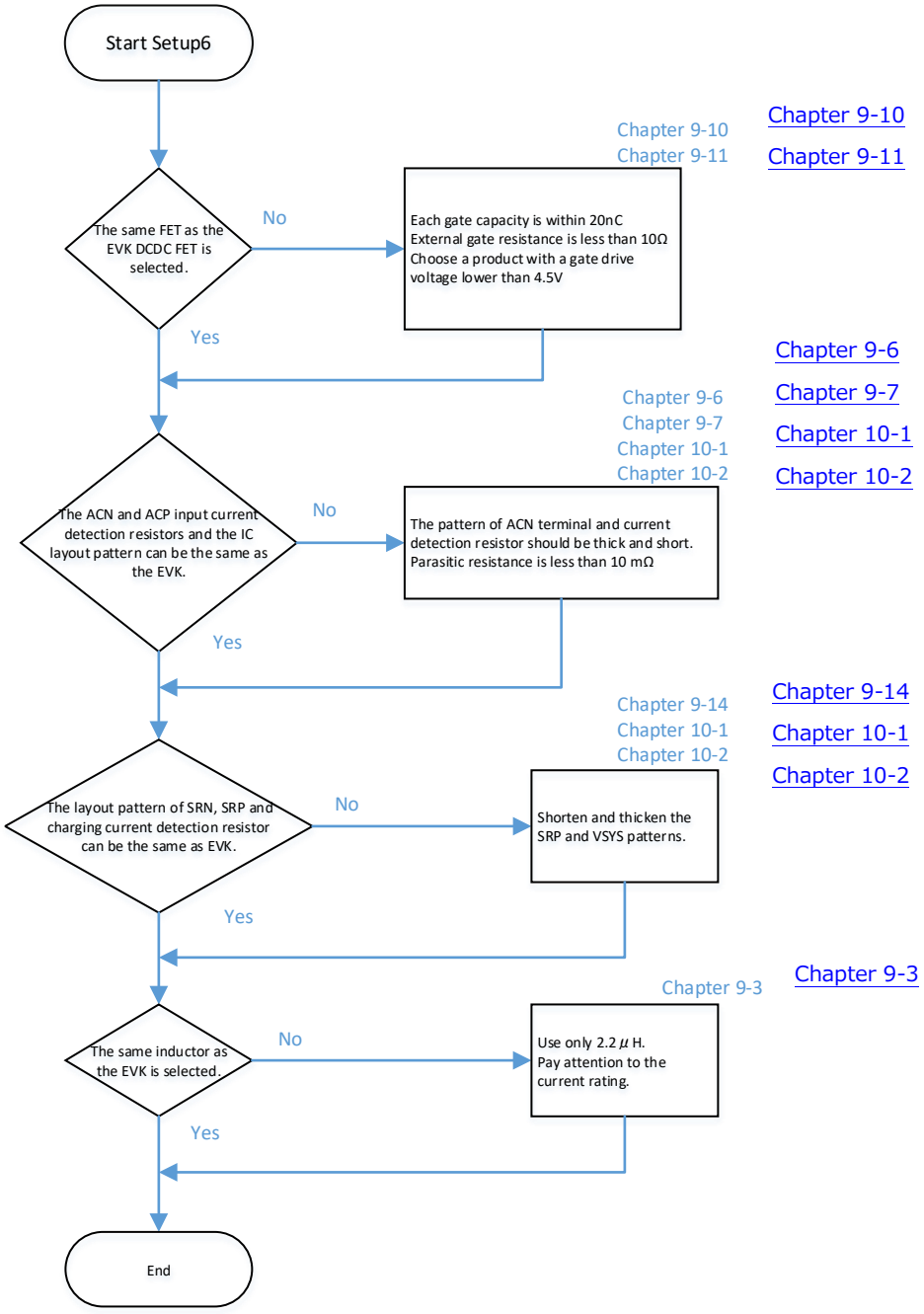


Figure 2-11. Flowchart of parts selection

2 - 12 Setting in battery 1S (cell) and 2S (cell)-4S (cell)

When the BD99954 is powered on the input, the system side outputs 8.9V. When using the BD99954 with one cell, the system side device should be selected with a higher breakdown voltage than 8.9V. 0x3A 11bit ONE_CELL_MODE should be set to 1 before the DCDC starts. 0x11 VSYSREG_SET should be set to 5.5V or lower, and VFASTCHG_REG_SET of 0x1A, 0x1B, and 0x1C should be set to 4.55V or lower. The default setting is 2 cells. When using for 3 cells and 4 cells, it is necessary to change the charging profile setting and set again the VBAT OVP.

2 - 13 Input voltage

The recommended operating range of VCC and VBUS input voltage is 3.8V to 25V, assuming 5V to 20V applications. The UVLO detection of the input voltage is 3.67V typical. When the input voltage falls below 3.67V, the DCDC and charging operations are turned off. When the input voltage rises to 3.8V or more again, it is recovered.

2 - 14 Input Current Limit

The input current limit can be set in the following way

・Default setting at startup: IADP/RESET pin voltage divider resistance or default minimum value of 128 mA

・Port detection value of BC1.2 when VCC_BC_DISEN or VBUS_BC_DISEN of 0x0B is 0

・Write 0x07 IBUS_LIM_SET and 0x08 ICC_LIM_SET registers from host

Input current limit during startup or input voltage insertion

When bit EXTIADPEN = 0 (bit 9, register 0x40), the input current limit is set to 128 mA (the default minimum value).

When bit EXTIADPEN = 1 (bit 9, register 0x40), the input current limit is set by the voltage divider on the IADP/RESET pin.

Input current limit after startup or input voltage insertion

When the value of VCC_BC_DISEN or VBUS_BC_DISEN of 0x0B is 0, input current limit can be set to the BC1.2 detection value when VCC or VBUS is inserted.

Otherwise, the input current limit will maintain the default setting at startup.

In normal operation

The input current limit can be set by the SMBus command from the host. Write register IBUS_LIM_SET or ICC_LIM_SET, depending on the input used.

When the input voltage is removed, the input current limit is reset as follows

When EXTIADPEN = 0 (bit 9, register 0x40), the default minimum value is 128 mA.

When EXTIADPEN = 1 (Bit 9, Register 0x40), it is determined by the voltage divider value of the IADP / RESET pin.

A flowchart of how to set the input current limit is shown in Figure 2-12. Clicking on the underlined blue text in the flowchart will take you to the linked chapter.

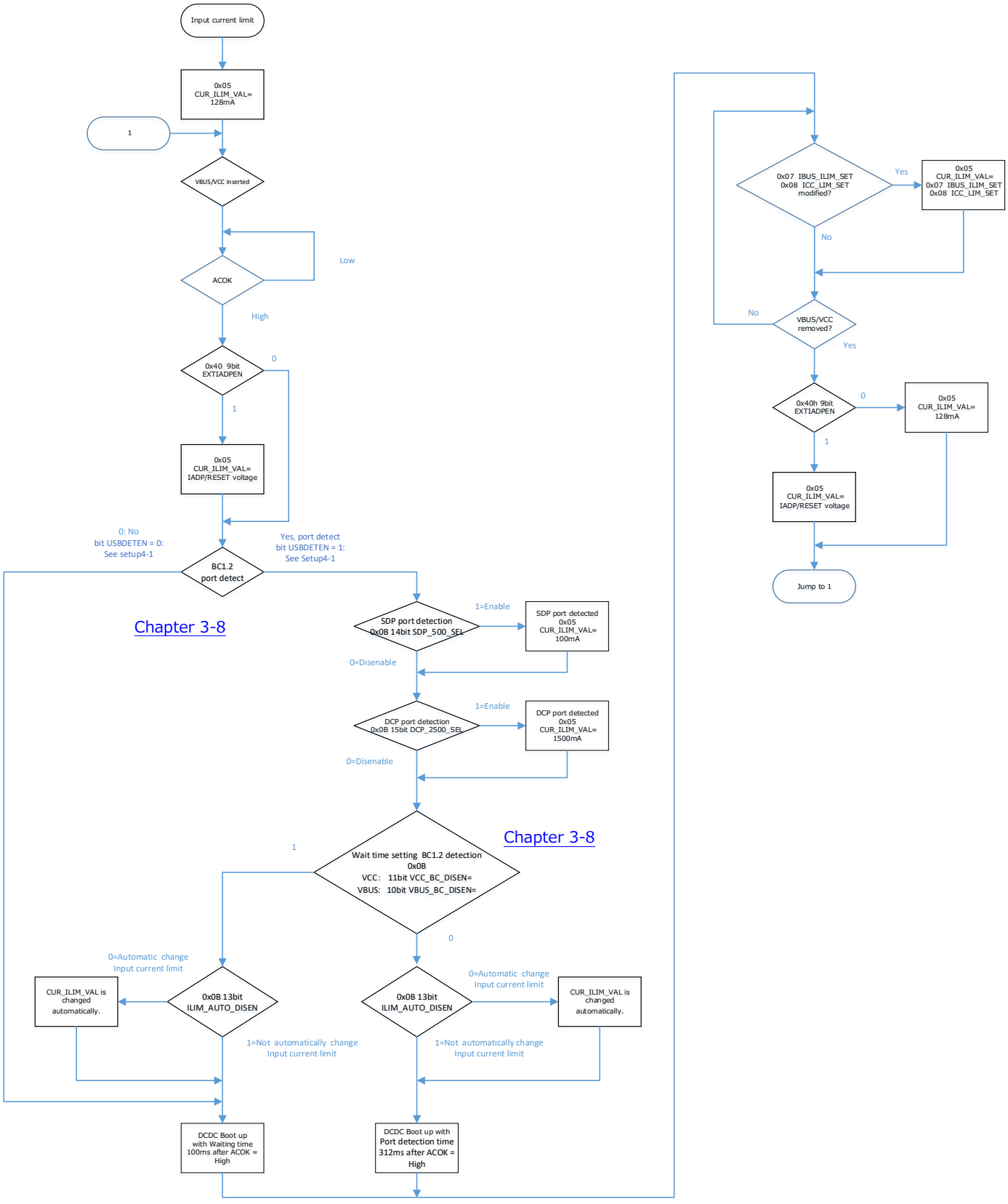
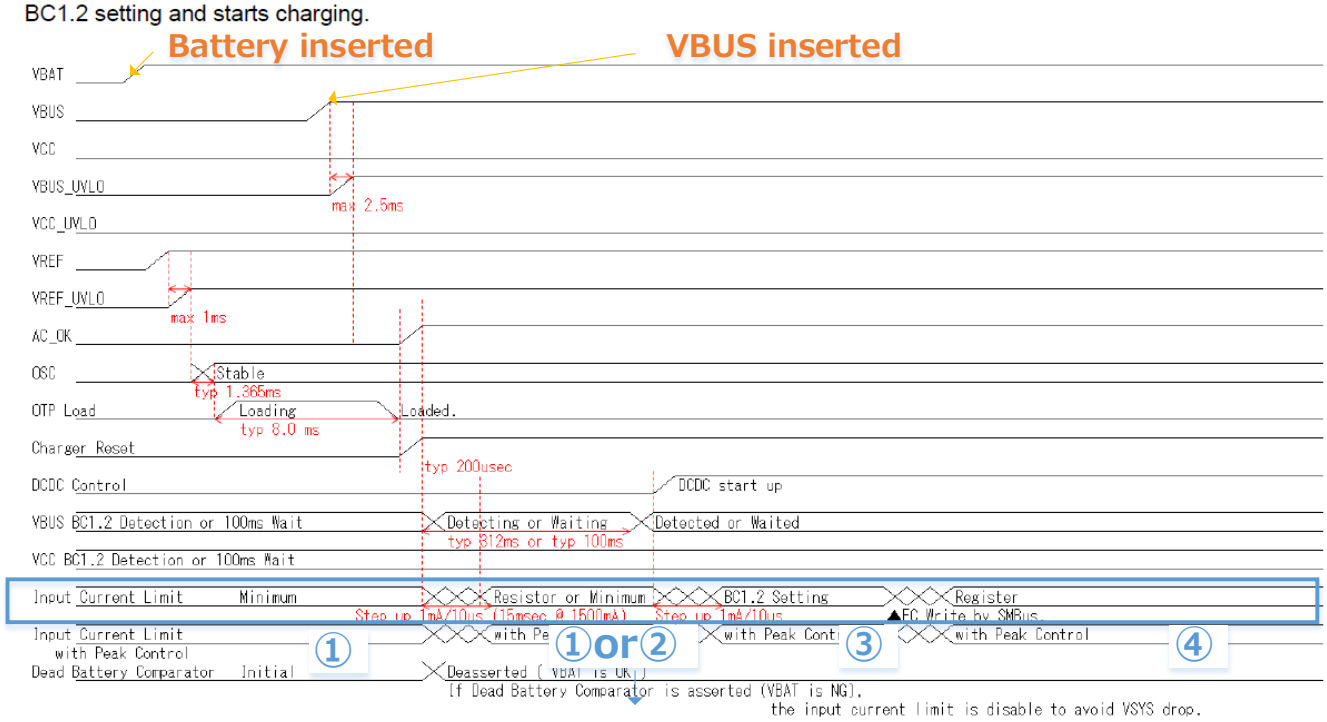


Figure 2-12. Input Current Limit Setting Flowchart

When VBAT, VBUS and VCC are connected, the input current limit is as shown in Figure 2-13 and Figure 2-14. Before VBUS is connected, it is set to the minimum value of 128mA. When the AC_OK pin becomes High after connection, if 0x40 9-bit EXTIADPEN = 1, the input current limit value is set by the external resistor of the IADP / RESET pin. When BC1.2 detection is set, the current limit is set to the current limit of BC1.2 port. The input current limit can be changed by writing the registers 0x07 IBUS_LIM_SET and 0x08 ICC_LIM_SET from the host.

7.9.1. VBAT power on and VBUS/VCC plugged-in

At the first VBAT power on, BD99954 starts OTP loading. And when VBUS or VCC is eventually plugged in, BD99954sserts ACOK and starts the BC1.2 Detection sequence. After the BC1.2 Detection is completed, BD99954 limits the input current, reflects the BC1.2 setting and starts charging.



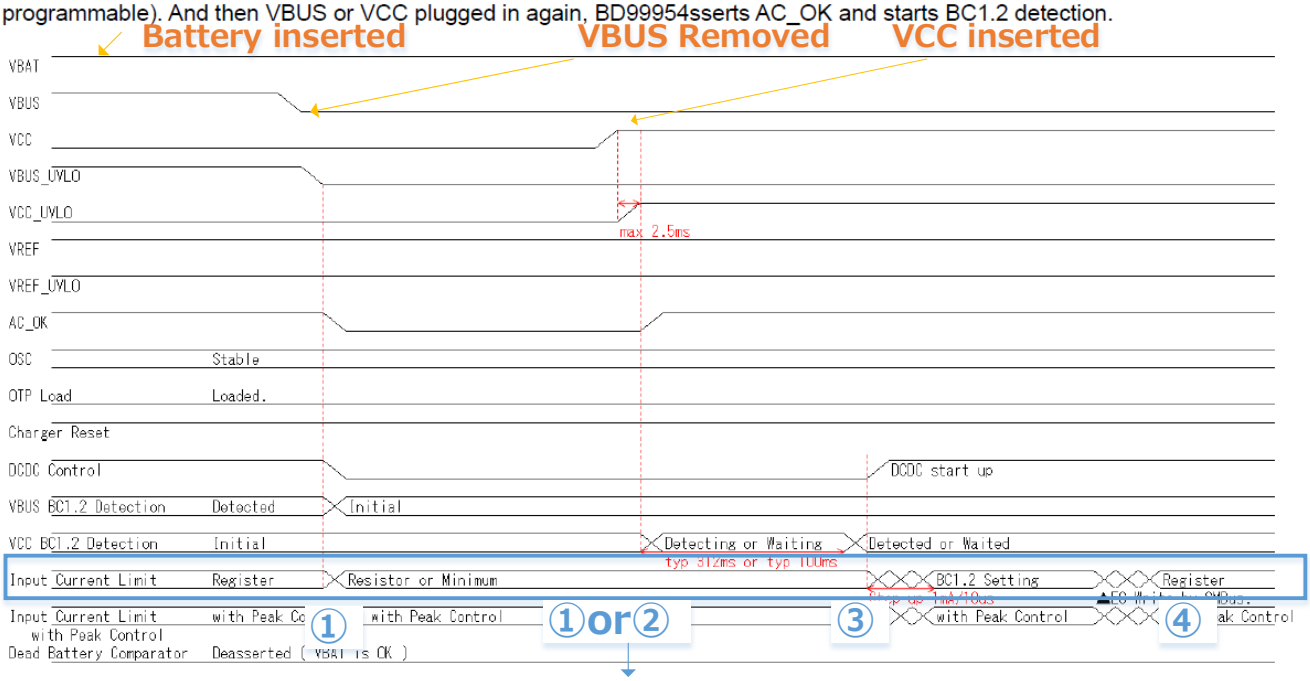
When EXTIADPEN = 1, the resistance voltage divider of the IADP / RESET pin is set. Otherwise, minimum = 128mA

Input Current Limit:
① Minimum: 128mA (default)
② Resistor: Voltage Divider on IADP/RESET pin (if EXTIADPEN=1)
③ BC1.2: if BC1.2 is enabled, Input current limit is set by BC1.2
④ Register: Input current limit set by MCU over SMBus

Figure 2-13. Relationship between input current setting values when Plug in

7.9.2. VBUS/VCC plugged-off

When VBUS plugged off, BD99954 deasserts AC_OK and limits input current as IADP external pin or minimum setting (it is programmable). And then VBUS or VCC plugged in again, BD99954sserts AC_OK and starts BC1.2 detection.



When EXTIADPEN = 1, the resistance voltage divider of the IADP / RESET pin is set. Otherwise, minimum = 128mA

Input Current Limit:
① Minimum: 128mA (default)
② Resistor: Voltage Divider on IADP/RESET pin (if EXTIADPEN=1)
③ BC1.2: if BC1.2 is enabled, Input current limit is set by BC1.2
④ Register: Input current limit set by MCU over SMBus

Figure 2-14. Relationship between input current setting value when Plug off

By connecting a voltage divider resistor to the IADP/RESET pin as shown in Figure 2-15, you can set the input current limit as shown in Figure 2-16.

This input current limit is set at the timing shown in (2) of Figure 2-13 and Figure 2-14.

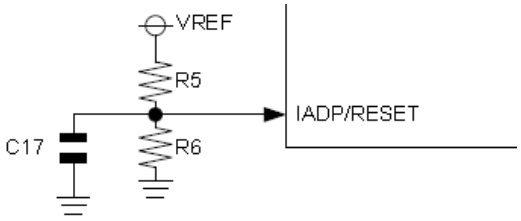


Figure 2-15. IADP / RESET terminal voltage divider resistor circuit

By setting the IADP/RESET pin voltage below 0.44V, the BD99954 stops all functions including DCDC and charging operations.

All register settings will be reset to their default values. It is possible to reset the device during operation, but it will force all operations to stop.

Note that the device may start up with a charge remaining in the capacitor when rebooting.

The BD99954 has a self-consumption current of about 50mA because the gate charge current flows through the external FET during DCDC operation. If the input current limit is set to as small as 100mA, it may result in a no-start state. When the IC is started up (OTP is loaded), the input current is limited by the IADP/RESET pin voltage setting, so the IC will not start up.

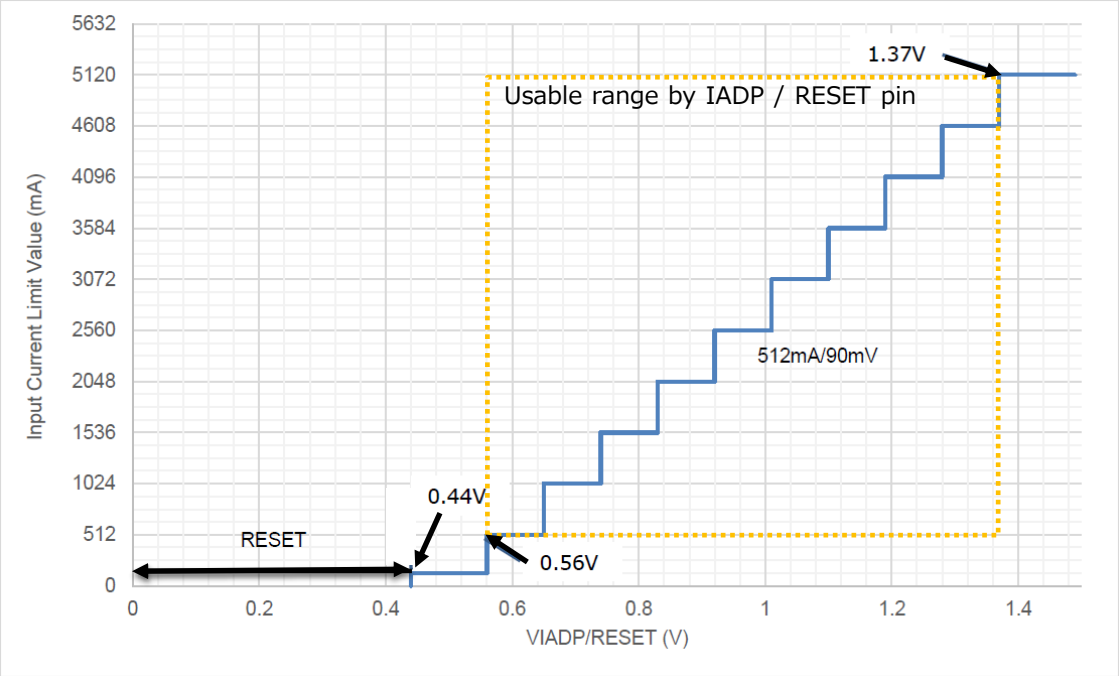


Figure 2-16. Relationship between IADP/RESET terminal voltage and input current setting value

The VBUS / VCC port setting register Address 0x07 / 0x08 IBUS_LIM_SET / ICC_LIM_SET guarantees only the accuracy shown in Table 7-2 on page 12 of the data sheet, surrounded by the red line in Figure 2-17. The accuracy of other values is not guaranteed.

Table 7-2 Electrical Characteristics for DC/DC Converter

Adapter=18.0V, Battery=7.4V, LX1=LX2=0.0V, GND=0V, Ta=25℃ (unless otherwise noted.)

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
<INPUT CURRENT>						
USB 500mA Current Accuracy	I_{USB500}	398	448	500	mA	REG0x07h/08h=01C0h
USB 900mA Current Accuracy	I_{USB900}	764	832	900	mA	REG0x07h/08h=0340h
BC1.2 1500mA Current Accuracy	$I_{USB1500}$	1380	1440	1500	mA	REG0x07h/08h=05A0h
USB-PD 3A Current Accuracy	$I_{USB3000}$	2824	2912	3000	mA	REG0x07h/08h=0B60h
USB-PD 5A Current Accuracy	$I_{USB5000}$	4792	4896	5000	mA	REG0x07h/08h=1320h
Input Current Setting Range	I_{ADPRNG}	96	-	16352	mA	REG0x07h or REG0x08h
Charge Current Setting LSB	I_{ADPLSB}	-	32	-	mA	

Figure 2-17. Lower limit setting of input current limit register (Address 0x07/0x08)

3 Charging profile

The charge profile is formed by setting the threshold voltage, target voltage, and the appropriate charge current for the battery, corresponding to the number of cells in the battery, and Figure 3-1 based on Figure 7-5 of the datasheet shows a typical example and related registers.

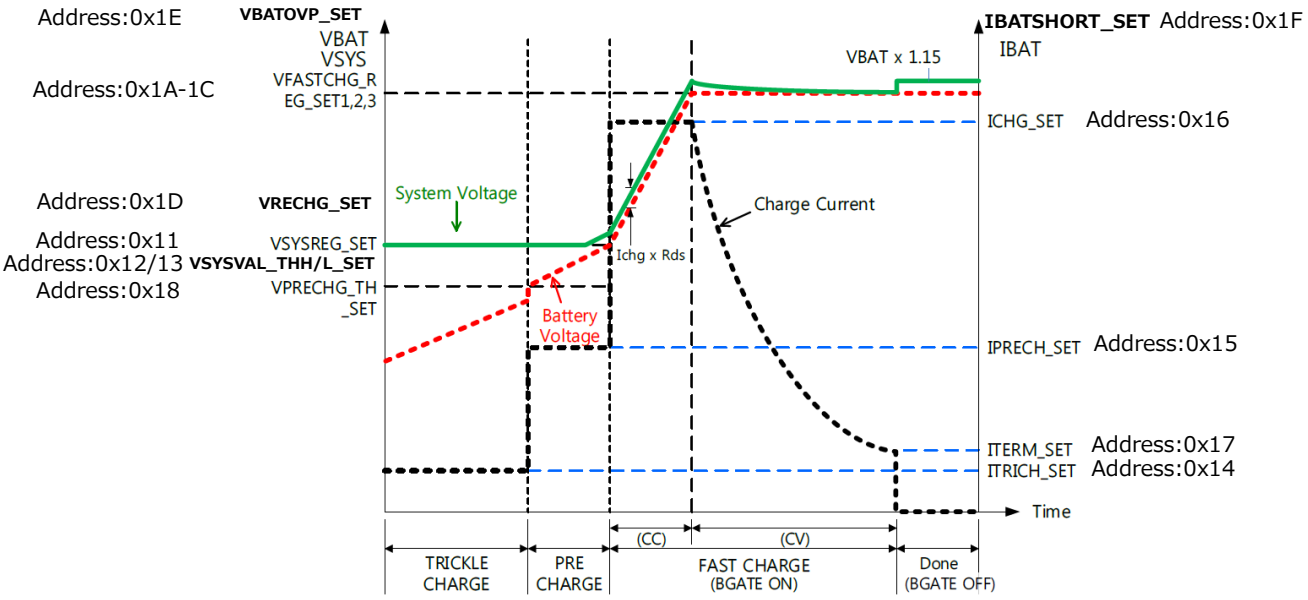


Figure 3-1. Charging profile and related registers

Refer to the vertical relationship of the charge profile related voltage/current shown in Figure 3-1.
For charging current, ITERM_SET should be set to 300mA or more as described in 3-5 Termination current (Termination current). ITERM_SET can be larger than IPRECH_SET or ITRICH_SET depending on the application, but this is not a problem.

・Charge current
IBATSHORT_SET ＞ ICHG_SET ＞ IPRECH_SET ≧ ITRICH_SET ＞ ITERM_SET

・Charging voltage
VFASTCHG_REG_SET1,2,3 to start CV charging voltage can set the voltage according to the temperature profile as described in 3-13 JEITA temperature profile. If you do not want to use JEITA temperature profile, set VFASTCHG_REG_SET1,2,3 to the same value.

VBATOVP_SET ＞ VFASTCHG_REG_SET1,2,3 ＞ VRECHG_SET ＞ VSYSREG_SET ＞ VSYSVAL_THH_SET ＞ VSYSVAL_THL_SET ＞ VPRECHG_TH_SET

3 - 1 Charge profile related register group

Table 3-1a and Table 3-1b summarize the charge profile-related registers, their usage, and the operation in the charge profile according to the settings.

Table 3-1a. Charging profile-related registers, their usage, and behavior during charging profile by setting

address	Write Registers Name	Description in Datasheet	Behavior during charging profile depending on usage/setting
0x11	VSYSREG_SET	VSYS regulation voltage setting and threshold voltage from Pre-charging to Fast-charging.	This is the lower limit of the VSYS output voltage. It rises toward FASTCHG_REG_SET with CC charging.
0x12	VSYSVAL_THH_SET	VSYS voltage rising detection threshold with hysteresis.	This is the threshold voltage setting value to stop VSYS voltage output.
0x13	VSYSVAL_THL_SET	VSYS voltage falling detection threshold with hysteresis.	This is the threshold voltage setting value to stop VSYS voltage output. When the voltage exceeds VSYS_THH_SET, VSYS is output, and when the voltage drops below VSYS_THL_SET, DCDC switching stops and the output is stopped. During charging, VSYSVAL_THH/L_SET is changed, and even if the VSYS voltage exceeds the threshold, the operation of VSYS voltage will not change.
0x14	ITRICH_SET	Trickle-charging current setting.	Trickle charge current setting. 1/10 of CC charge current is recommended.
0x15	IPRECH_SET	Pre-charging current setting.	This is the pre-charge charge current setting. 1/10 of the CC charge current is recommended.
0x16	ICHG_SET	Fast-charging current setting.	This is the CC charge current setting. Set according to the battery.
0x17	ITERM_SET	Charging Termination Current.	This is the end-of-charge current setting; when IBAT falls below this setting, charging is terminated.
0x18	VPRECHG_TH_SET	Threshold voltage from Trickle-charging to Pre-charging.	The threshold voltage setting for Tricle to Pre-charge.
0x1A	VFASTCHG_REG_SET1	Fast Charging Regulation Voltage.	Full charge voltage setting value. If thermistor is not used, please check 0x41-45: THERM_WINDOW_SET1-5 must be set correctly by OTP load value to make VFASTCHG_REG_SET2/3 setting effective.
0x1B	VFASTCHG_REG_SET2	Fast Charging Regulation Voltage for the JEITA temperature range T3-T5.	
0x1C	VFASTCHG_REG_SET3	Fast Charging Regulation Voltage for the JEITA temperature range T5-T4 and T1-T2.	
0x1D	VRECHG_SET	Re-charge Battery Voltage.	This is the threshold setting for recharge start voltage, which should be within the CC charge voltage range.
0x1E	VBATOVP_SET	Battery over-voltage detection threshold.	OVP threshold setting for BATT voltage, recommended to be +10% of VFASTCHG_REG_SET1.

Table 3-1b. Charging profile-related registers and their usage and configuration during charging profile (continued)

address	Write Registers Name	Description in Datasheet	Behavior during charging profile depending on usage/setting
0x1F	IBATSHORT_SET	Battery Short Current Protection Threshold.	BATT current OCP threshold setting. When the threshold is set at 0x1F and the WDT_IBAT_SHORT of the watchdog timer 0x10 is completed, the bit <6> IBAT_SHORT of 0x01 becomes "1". Because this is only the Interrupt function DCDC and charging will not stop and will continue to operate.
0x48	VBAT_TH_SET	Battery Voltage Interrupt Threshold. 0 to 19,200mV, 1mV steps.	BATT voltage interrupt threshold setting. 0x6B: Judgment value for INT3_SET[9:8].

Figure 3-2 shows the internal circuit of the IC in which the charge profile related registers function.

The light blue cells in the figure represent the charge profile-related registers, and their locations (signal names on the right side of the light blue cells) indicate where they function. The same signal name in the figure indicates the state of the connection. The same signal name in the diagram indicates the status of the connection (e.g., BATT pin and BATT in the MUX input).

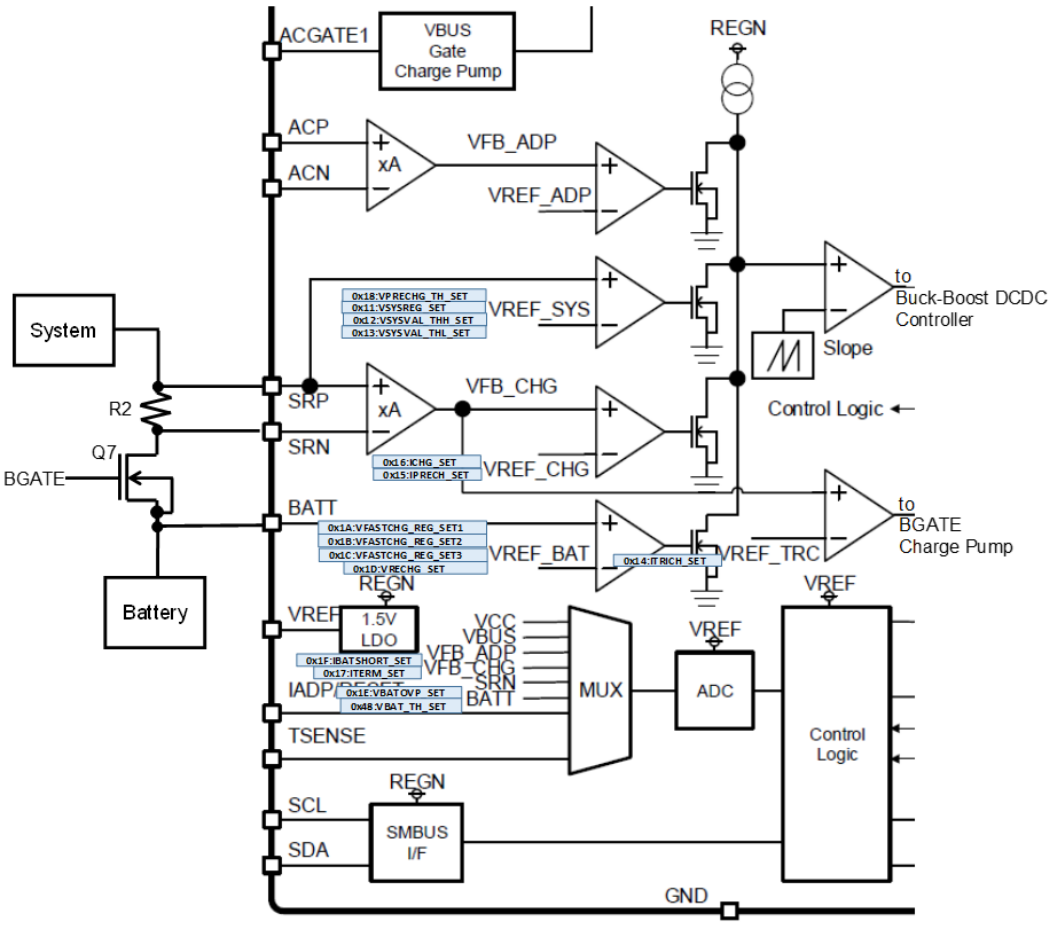


Figure 3-2. Block diagram in which the charging profile related register function

3 - 2 The block in which the charging profile-related register group functions

The accuracy of the charge profile related registers (light blue cells) in Figure 3-2 varies depending on the register settings. For example, VSYSREG_SET, which is the set value of VSYS voltage, functions as a reference voltage for the amplifier circuit, so its accuracy is ± several percent as shown in Table 3-2 (partially excerpted from Data Sheet Table 7-2).

Table 3-2. Accuracy of VSYSREG_SET

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
<MINIMUM SYSTEM VOLTAGE>						
Minimum System Voltage Setting Range	V_{MSVRNG}	2.560	-	19.2	V	VSYSREG_SET=2,560 ~ 19,200mV, 64mV steps.
Minimum System Voltage Setting LSB	V_{MSVLSB}	-	64	-	mV	
Minimum System Voltage accuracy	V_{MSV1}	-2.0%	3.072	+2.0%	V	REG0x11h=0C00h
	V_{MSV2}	-1.0%	6.144	+1.0%	V	REG0x11h=1800h
	V_{MSV3}	-2.0%	9.216	+2.0%	V	REG0x11h=2400h
	V_{MSV4}	-2.0%	12.288	+2.0%	V	REG0x11h=3000h

3 - 3 Fast charge current, Pre-Charge current, Trickle-Charge current

The accuracy of the charge current settings, ICHG_SET for Fast-Charge current, IPRECH_SET for Pre-Charge current, and ITRICH_SET for Trickle-Charge current, ranges from ±2% to ±40% depending on the conditions, as shown in Table 3-3 (excerpt from Table 7-4 of the datasheet).

Table 3-3. Accuracy of charging current

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
<CHARGE CURRENT>						
Charge Current Setting Range	I_{CHGRNG}	0	-	16384	mA	REG0x16h
Charge Current Setting LSB	I_{CHGLSB}	-	64	-	mA	
Charge Current accuracy (10mΩ current sense resistor, BATT > Minimum System Voltage)	I_{CHG1}	-2%	4096	+2%	mA	REG0x16h=1000h
	I_{CHG2}	-3%	2048	+3%	mA	REG0x16h=0800h
	I_{CHG3}	-5%	1024	+5%	mA	REG0x16h=0400h
	I_{CHG4}	-20%	256	+20%	mA	REG0x16h=0100h
	I_{CHG5}	-40%	128	+40%	mA	REG0x16h=0080h
Trickle Charge Current Setting Range	$I_{TRCCHGRNG}$	0	256	1024	mA	REG0x14h or REG0x15h
Trickle Charge Current Setting LSB	$I_{TRCCHGLSB}$	-	64	-	mA	
Maximum Trickle Charge Current (10mΩ current sense resistor, BATT < Minimum System Voltage)	I_{CHG6}	-	1024	-	mA	REG0x14h or REG0x15h

3 - 4 Charge stop voltage

The accuracy of VFASTCHG_REG_SET1, 2, and 3 of the termination voltage, which is the set value of the full charge voltage, is ±0.5%, as shown in Table 3-4 (excerpt from Table 7-4 of the datasheet).

Table 3-4. Accuracy of full charge voltage

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
<CHARGE VOLTAGE>						
Charge Voltage Setting Range	V_{CVRNG}	2.560	-	19.200	V	REG0x1A, REG0x1Bh or REG0x1Ch
Charge Voltage Setting LSB	V_{CVLSB}	-	16	-	mV	
Charge Voltage accuracy	V_{CV1S}	-0.5%	4.192	+0.5%	V	REG0x1Ah/0x1Bh/0x1Ch=1060h
	V_{CV2S}	-0.5%	8.400	+0.5%	V	REG0x1Ah/0x1Bh/0x1Ch=20D0h
	V_{CV3S}	-0.5%	12.592	+0.5%	V	REG0x1Ah/0x1Bh/0x1Ch=3130h
	V_{CV4S}	-0.5%	16.800	+0.5%	V	REG0x1Ah/0x1Bh/0x1Ch=41A0h
VBAT OVP Detection range	V_{OVPRNG}	2.56	-	19.2	V	REG0x1Dh

3 - 5 Termination current

ITERM_SET, etc., located on the left side of the MUX, are judged to be above or below their setting values in comparison with the ADC measurement values, so these will include the measurement error of the ADC and the effective measurement range of the ADC. These accuracies are described in Data Sheets 7.8.1 and 7.8.2 (page 17). These areas of particular interest are shown in Figure 3-3 with red boxes.

7.8. 12-bit ADC

7.8.1. Outline

- 12-bit Successive Approximation Register A/D Converter
- Input Voltage range: 2.0 to 19.2V (BATT)
- Input Voltage range: 2.0 to 25V (VBUS, VCC, ACP, SRP)
- Input Voltage range: 0.1 to 1.4V (TSENSE)
- Input Voltage range: 0.1 to 1.4V (IADP/RESET)
- Current monitor range: 0.3 to 16.384A (IACP)
- Current monitor range: 0.3 to 25A (IBAT)

7.8.2. Electrical Characteristics

Table 7-7 Electrical Characteristics for 12-bit SAR-ADC

(Unless otherwise specified, Ta=25°C, VREF=1.5V)

Parameter	Symbol	Specification			Unit	Condition
		Min	Typ	Max		
<12-bit SAR ADC>						
Resolution	RES	-	-	12	bit	
Conversion Period	TCONV	-	20	-	μs	
Gain Error 1	Gerr1	−1.1	-	+1.1	%	BATT,VBUS,VCC,ACP, SRP=5V and 15V
Gain Error 2	Gerr2	−1.1	-	+1.1	%	TSENSE,IADP/RESET =0.5V and 1.0V
Gain Error 3	Gerr3	−1.1	-	+1.1	%	IACP,IBAT=1.5A and 8A
VOffset error	Voffset	-110		110	mV	
IOffset error	Ioffset	-110	-	110	mA	

Figure 3-3. Accuracy of a group of registers using ADC measurement values as judgment material

In other words, the voltage accuracy is ± 110 mV ± 1.1% under the condition of VBUS is larger than 2.0 V, and the current accuracy is ± 110 mA ± 1.1% under the condition of ITERM is larger than 0.3 A. Reading values below the lower limit are not covered by the accuracy guarantee.

As for the current value such as ICHG_SET, Figure 3-2 shows that the voltage drop caused by the current flowing through R2 is monitored as a potential difference, so the comparable value changes depending on the value of the current detection resistor R2. In the data sheet P14, the guaranteed charging current values (“CHARGE CURRENT” part in the data sheet Table 7-4) are all when R2 is 10mΩ. The recommended values of R2 are 10mΩ and 20mΩ. If ICHG_SET is not large, it can be used for the purpose of improving the accuracy of ITERM_SET by setting R2 to 20 mΩ. The BD99954 converts the voltage at both ends of a 10mΩ current-sensing resistor into a current, and when R2 is 20mΩ, the voltage at both ends of the resistor is twice that of 10mΩ,

so the charge current setting value should be twice that of 10mΩ in the software design of the set.

In the case of R2=20mΩ, the accuracy depends on the judgment value by comparison with the ADC measurement value and the setting of the current detection amplifier gain ("xA" in Figure 3-2) with SRP-SRN input in Figure 3-2. The operation of this circuit is shown in Table3-5.

Table3-5. Change in accuracy when R2 are 10mΩ and 20mΩ

Value based on ADC measurements				
Item	Data Sheet Description	Accuracy at 10mΩ	Accuracy at 20mΩ	Circuit Operation
Gain Error3	Table 7-7, line 5.	±1.1%	±0.55%	Each ADC measurement that contains errors is compressed by the resistance ratio, which improves accuracy.
I Offset Error	Table 7-7, line 7.	±110mA	±55mA	
Value by current detection amplifier				
ICHG1 (4096mA target)	Table7-4 Charge Current accuracy	±2%	±2%	To change the current detection amplifier gain in steps according to the setting value of REG0x16 (ICHG_SET) (large register value = small gain). However, other than the guaranteed value in steps of 10mΩ, it is not guaranteed.
ICHG2 (2048mA target)		±3%		
ICHG3 (1024mA target)		±5%	±3%	
ICHG4 (256mA target)		±20%	±20%	
ICHG5 (128mA target)		±40%		

If the current detection resistance R2 is made larger, the current detection amplifier may malfunction, causing BGATE=OFF, and charging cannot be performed correctly.

3 - 6 Example of representative register values for each number of battery cells in the charge profile-related register group

Table 3-6 shows a typical example of the setting values of each register when 2, 3, or 4 cells are used. The charging current in the table is the value when R2=10mΩ.

Although these values are based on safety considerations, we ask that you carefully consider and evaluate the battery characteristics used when evaluating the EVK as well as the actual set board.

The rightmost column of Table 3-6 shows the ratio of the reference cell voltage (4.2V) to the number of cells in series (N), which can be used as a reference for designing the setting value. In addition, for the examples of typical current setting values, the recommended ratio to 1C is shown in italics, assuming that a 3000mAh battery is charged to 1C. (For ITERM_SET, the lower limit value is shown according to the description in the previous section 3-5.

Table 3-6. Example of representative register values for each number of battery cells in the charge profile-related register group

address	Code name	Unit	1 Cell write (HEX)	Phisical (DEC)	2 Cell write (HEX)	Phisical (DEC)	3 Cell write (HEX)	Phisical (DEC)	4 Cell write (HEX)	Phisical (DEC)
0x11	VSYSREG_SET	mV	0BB8	3000	1880	6272	24C0	9408	3140	12608
0x12	VSYSVAL_THH_SET	mV	09C4	2500	1580	5504	2040	8256	2B00	11008
0x13	VSYSVAL_THL_SET	mV	08A0	2208	1340	4928	1D40	7488	2700	9984
0x14	ITRICH_SET	mA	0100	256	0100	256	0100	256	0100	256
0x15	IPRECH_SET	mA	0140	320	0140	320	0140	320	0140	320
0x16	ICHG_SET	mA	0BA0	2976	0BA0	2976	0BA0	2976	0BA0	2976
0x17	ITERM_SET	mA	0140	320	140	320	0140	320	0140	320
0x18	VPRECHG_TH_SET	mV	09C4	2500	1040	4160	1880	6272	20C0	8384
0x1A	VFASTCHG_REG_SET1	mV	1068	4200	20D0	8400	3140	12608	41A0	16800
0x1B	VFASTCHG_REG_SET2	mV	0FA0	4000	2000	8192	3010	12304	4010	16400
0x1C	VFASTCHG_REG_SET3	mV	0ED8	3800	1F40	8000	2EE0	12000	3E80	16000
0x1D	VRECHG_SET	mV	0F3C	3900	1FB0	8112	2C90	11408	3B60	15200
0x1E	VBATOVP_SET	mV	1168	4456	22D0	8912	3330	13104	47E0	18400
0x1F	IBATSHORT_SET	mA	1F40	8000	1F40	8000	1F40	8000	1F40	8000
0x48	VBAT_TH_SET	mV	0BEA	3050	1800	6144	2400	9216	3000	12288

The yellow cells in the table are the settings that have been changed from the OTP load values (see "Li-Ion Battery Manager Quick Reference (1)" for OTP load method/load values). The OTP load value is the target value for 2 cells (IC design concept 1), but the yellow cell needs to be changed to match the typical value example in Table 3-6.

When the current detection resistance R2 = 20mΩ, the true value of "Physical" of the charge current in the table becomes the register setting value (DEC) x (10/20). (Example: When 320mA (0140h) is set for ITERM_SET, the true value is 160mA)

3 - 7 Start charging

Charging is started by setting 0x0C:CHGOP_SET2 bit 7: CHG_EN = 1.

With only the register settings described in the previous section 3-6, the port (VBUS/VCC) settings and interrupt settings remain at the OTP-loaded values (assuming they are OTP-loaded), so they need to be optimized as necessary. However, it is possible to run a charging profile (IC Design Concept 3).

3 - 8 BC1.2 compatible

By setting USBDET_EN [6h] of VCC_UCD_SET 0x28 and VBUS_UCD_SET 0x30 to Enable, it is possible to check the result of D+ and D- adapter detection from STATUS of VCC_UCD_STATUS 0x29 and VBUS_UCD_STATUS 0x31. Ports other than BD1.2 are not supported.

Table 3-7. BC1.2 Detection results

	CHGDET	PUPDET	DCDFAIL	CHGPORT[1]	CHGPORT[0]
VBUS Open	0	0	0	0	0
SDP	0	0	0	0	1
CDP	1	0	0	1	0
DCP	1	0	0	1	1
Pull-up Port	0	1	1	0	1
Open Port	0	0	1	0	1
Unstable Port	0	0	1	0	1

The BD99954 has a built-in BC1.2 Detector function. The detected result can be confirmed as STATUS.
It has a built-in switch that outputs the resistance values of D+ and D- of the port directly to the HOST side. There is no restriction on the internal switch switching timing.

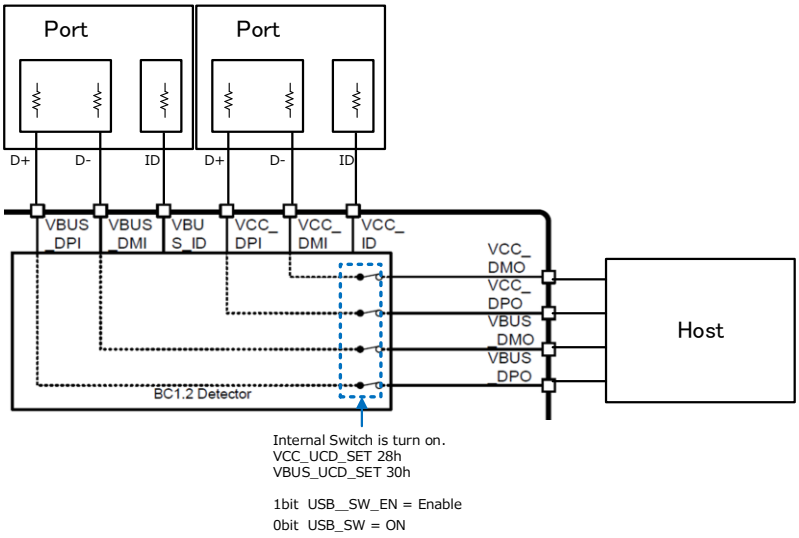


Figure 3-4. D+, D- port Detection circuit

Adapter detection settings for D+ and D-

The BC1.2 detection method can be set with the registers VCC_UCD_SET 0x28 and VBUS_UCD_SET 0x30, and the internal switches for D+ and D- detection can be controlled.

Table 3-8. D+, D- adapter detection setting

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	BCSRETRY	Trigger for re-trial of the USB Charger Port detection. "1": Start detection / "0": Release the operation.
11	reserved	
10	reserved	
9	reserved	
8	ADCRTRY	Trigger for re-trial of USB ID Resistor detection. "1": Start detection / "0": Release the operation.
7	USBDETEN	Enabling USB Charger port detection. "1": Enable / "0": Disable.
6	IDRDETEN	Enabling USB ID Resistor detection. "1": Enable / "0": Disable.
5	ENUMRDY	Setting USB Enumeration to Ready. "1": Skip Secondary Detection / "0": Normal operation.
4	ADCPOLEN	USB ID input polling enable. "1": Enable (always detection) / "0": Disable.
3	DCDMODE	DCD timeout period setting. "1": 1280 ms / "0": 640 ms.
2	reserved	
1	USB_SW_EN	Enabling automatic USB-Switch control. "1": Enable (auto) / "0": Disable (manual).
0	USB_SW	USB Switch manual control. "1": Switch ON / "0": Switch OFF.

Checking the STATUS of the D+ and D- adapter detection results

BC1.2 detection result can be confirmed by VCC_UCD_STATUS 0x29 and VBUS_UCD_STATUS 0x31.

Table 3-9. D+, D- adapter detection STATUS check

Bit	Symbol	Description
15	DCDFAIL	DCD (USB Data Contact Detection) failed (timeout) status. "1": Failed / "0": Succeeded.
14	reserved	
13	CHGPORT[1]	USB Charger Port Detection result. 00b: No charger port/ 01b: SDP/ 10b: CDP/ 11b: DCP
12	CHGPORT[0]	
11	PUPDET	Pull-up detected at Primary Detection after DCDFAIL. "1": Detected / "0": Not detected.
10	reserved	
9	reserved	
8	reserved	
7	VBUS_VLD	USB VBUS valid voltage detection status. "1": Valid / "0": Not valid.
6	CHGDET	USB Charger Port detection status. "1": Detected / "0": Not detected.
5	reserved	
4	reserved	
3	OTGDET	USB OTG Device detection status. "1": Detected / "0": Not detected.
2	reserved	
1	reserved	
0	reserved	

Checking the STATUS of the D+ and D- adapter detection results

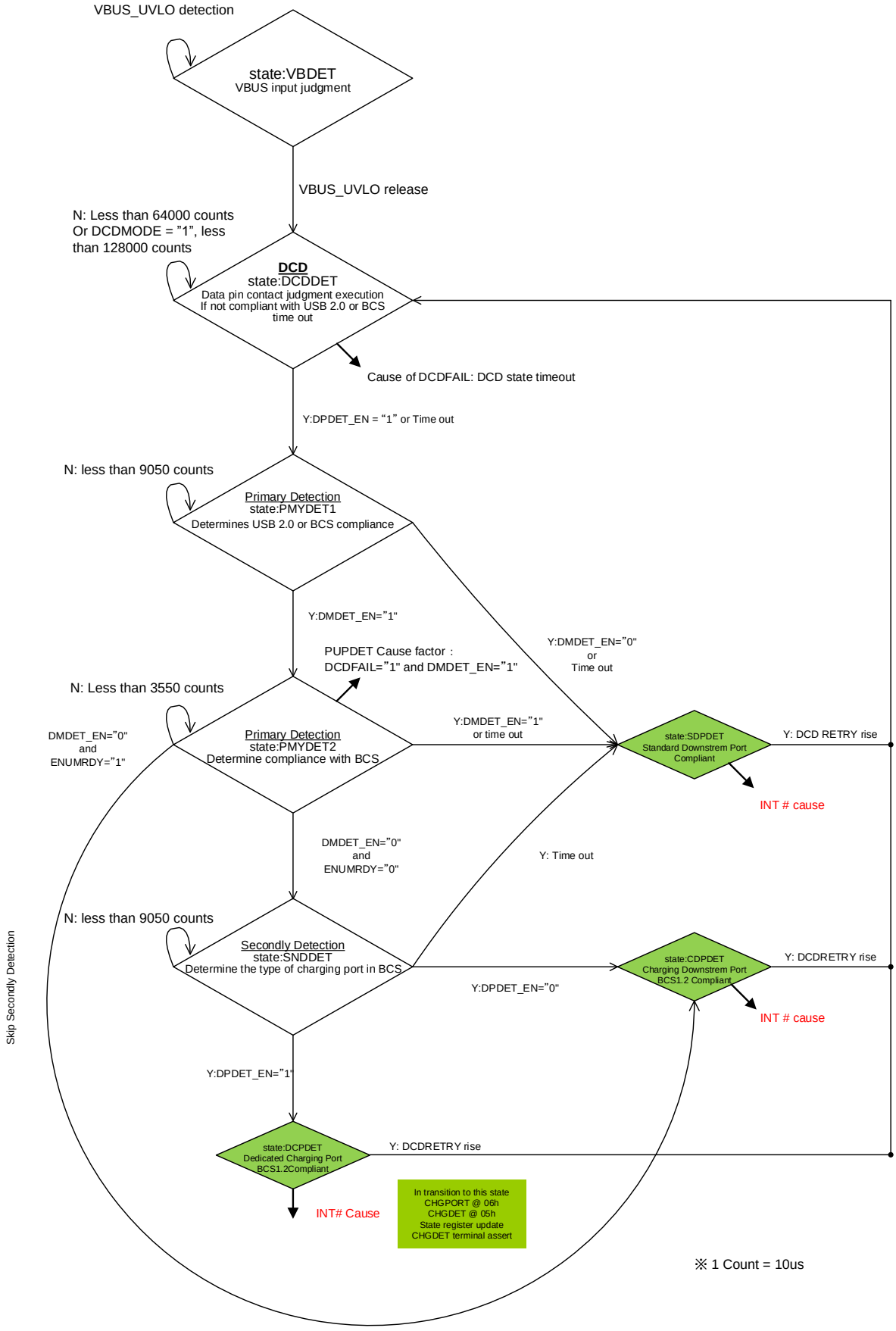


Figure 3-5. BC1.2 Detection flowchart

ID detection

ID detection STATUS can be confirmed by VCC_IDD_STATUS 0x2A and VBUS_IDD_STATUS 0x32.

ID detection result Check STATUS

Table 3-10. ID detection setting

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	reserved	
6	VBINOP	VBUS voltage status while ID detection. “1”: Normal voltage / “0”: Abnormal voltage.
5	EXTID	Check MHL ID (1k Ohm) detection support. “1”: Supported / “0”: Not supported.
4	IDRDET	USB ID Resistor contact detection status. “1”: Detected (contacted) / “0”: Not detected (removed).
3	INDO[3]	USB ID detection result.
2	INDO[2]	
1	INDO[1]	
0	INDO[0]	

USB ID detection result can be confirmed with INDO [3: 0].

Table 3-11. ID detection STATUS confirmation

INDO	ID Resistance	Detected Port/Device
0h	0 - 10Ω	RID_GND (OTG)
1h	36.5kΩ	RID_C (ACA_C, SDP)
2h	47kΩ	-
3h	68kΩ	RID_B (ACA_B, DCP)
4h	102kΩ	-
5h	124kΩ	RID_A (ACA_A, CDP)
6h	180kΩ	-
7h	200kΩ	RID_FLOAT
8h	287kΩ	-
9h	390kΩ	-
Ah	440kΩ	-
Bh	557kΩ	-
Ch	797kΩ	-
Dh	>1MΩ	-
Eh	1KΩ	(MHL)
Fh	Illegal ID	Unknown

3 - 9 Battery Learn

To perform a battery learn, set 0C CHGOP_SET2 8-bit BATT_LEARN to Enable as 1.
Charging operation and DCDC will be paused; if VBAT> VSYSREG_SET, BAGTE will be turned on after BATT_LEARN is 1. It does not depend on CHG_EN= 1 or 0. This bit is automatically cleared when the VBAT voltage becomes VBAT <VSYSREG_SET on Dead Battery.

3 - 10 Charge-related ADC measurements

The ADC measured values of charge voltage and charge current can be checked with the following registers.
"_VAL" is the value that the ADC measured once. _AVE_VAL" is the average value of two measurements.

Table 3-12. Charge-related ADC measurement registers

Address	Bit name	bit	Description
0x50	IBATP_VAL	[14:0]	Battery Current (Charge) Measurement Value. 0 to 25,000mA, 1mA steps.
0x51	IBATP_AVE_VAL	[14:0]	Battery Current (Charge) Measurement Value. 0 to 25,000mA, 1mA steps. Average value measured twice
0x52	IBATM_VAL	[14:0]	Battery Current (Dis-charge) Measurement Value. 0 to 25,000mA, 1mA steps.
0x53	IBATM_AVE_VAL	[14:0]	Battery Current (Dis-Charge) Measurement Value. 0 to 25,000mA, 1mA steps. Average value measured twice
0x54	VBAT_VAL	[14:0]	Battery Voltage Measurement Value. 0 to 19,200mV, 1mV steps.
0x55	VBAT_AVE_VAL	[14:0]	Battery Voltage Measurement Value. 0 to 19,200mV, 1mV steps. Average value measured twice

3 - 11 Setting Interrupt related to charging

3 - 11 - 1 1st Level Interrupt setting

The interrupt function consists of 1st Level and 2nd Level. To use the interrupt function, INT1 to INT7 of the 1st Level of 0x68 [7:1] can be enabled by setting INT0_EN of 0x68 to 1. Table 3-13 shows the 1st level interrupt setting registers and the corresponding status registers. 1 in the STATUS bit confirms that an interrupt has occurred. The STATUS bit can be reset to "0" by writing "1" to it. When an interrupt occurs, the INT# pin, which is pulled up by an external resistor, goes low.

Table 3-13. 1st Level Interrupt Enable Setting Register

0x68 INT0_SET 0x70 INT0_STATUS

Bit	Bit name	bit	Bit name	Description
0	INT0_EN	0	INT0_STATUS	1st Level Interrupt Enable.

Interrupt 1: Enable / 0: Disable.

STATUS 1: Event occurred / 0: Disable. 1 Write Status clear

3 - 11 - 2 2nd Level Interrupt setting

Enabling INT1_EN to INT7_EN on the 1st Level of 0x68 [7:1] enables the configuration of 2nd Level INT1_SET to INT7_SET interrupts on 0x69, 0x6A, 0x6B, 0x6C, 0x6D, 0x6E, and 0x6F.

Table 3-14. 2nd Level Interrupt Enable Setting Register

0x68	INT0_SET	0x70	INT0_STATUS	
bit	Bit name	bit	Bit name	Description
7	INT7_EN	7	INT7_STATUS	2nd Level Interrupt 7 (SAR-ADC) Enable.
6	INT6_EN	6	INT6_STATUS	2nd Level Interrupt 6 (Charger)
5	INT5_EN	5	INT5_STATUS	2nd Level Interrupt 5 (Charger)
4	INT4_EN	4	INT4_STATUS	2nd Level Interrupt 4 (VSYS)
3	INT3_EN	3	INT3_STATUS	2nd Level Interrupt 3 (Battery)
2	INT2_EN	2	INT2_STATUS	2nd Level Interrupt 2 (VCC)
1	INT1_EN	1	INT1_STATUS	2nd Level Interrupt 1 (VBUS)

Interrupt 1: Enable / 0: Disable.

STATUS 1: Event occurred / 0: Disable. 1 Write Status clear

3 - 12 Setting and checking the status of 2nd level Interrupts related to charging

The threshold value can be set by IBATP_TH_SET 0x46 for charge current, IBATM_TH_SET 0x47 for discharge current, and VBAT_TH_SET 0x48 for charge voltage. By enabling the INT3_SET and INT7_SET registers, the INT_STATUS register is set to 1 when the ADC measurement value exceeds these thresholds. The STATUS register can be set to 0 by writing 1 to it. There are no restrictions on when to read the STATUS register.

Table 3-15. Interrupt configuration register related to charging

Address	Address name	bit	Bit name	Description
0x46	IBATP_TH_SET	[14:0]	IBATP_TH_SET	Battery Current (Charge) Interrupt Threshold.
0x47	IBATM_TH_SET	[14:0]	IBATM_TH_SET	Battery Current (Dis-Charge) Interrupt Threshold.
0x48	VBAT_TH_SET	[14:0]	VBAT_TH_SET	Battery Voltage Interrupt Threshold.
0x6B	INT3_SET	9	VBAT_TH_DET	Interrupt VBAT Voltage > VBAT_TH_SET.
0x6B	INT3_SET	8	VBAT_TH_RES	Interrupt VBAT Voltage <= VBAT_TH_SET.
0x6F	INT7_SET	3	IBATM_TH_DET	Interrupt Battery Current (Dis-charge) > IBATM_TH_SET.
0x6F	INT7_SET	2	IBATM_TH_RES	Interrupt Battery Current (Dis-charge) <= IBATM_TH_SET.
0x6F	INT7_SET	1	IBATP_TH_DET	Interrupt Battery Current (Charge) > IBATP_TH_SET.
0x6F	INT7_SET	0	IBATP_TH_RES	Interrupt Battery Current (Charge) <= IBATP_TH_SET.

Table 3-16. Interrupt configuration register related to STATUS

Address	Address name	bit	Bit name	Description
0x73	INT3_STATUS	9	VBAT_TH_DET	Interrupt status VBAT Voltage > VBAT_TH_SET.
0x73	INT3_STATUS	8	VBAT_TH_RES	Interrupt status VBAT Voltage <= VBAT_TH_SET.
0x77	INT7_STATUS	3	IBATM_TH_DET	Interrupt status Battery Current (Dis-charge) > IBATM_TH_SET.
0x77	INT7_STATUS	2	IBATM_TH_RES	Interrupt status Battery Current (Dis-charge) <= IBATM_TH_SET.
0x77	INT7_STATUS	1	IBATP_TH_DET	Interrupt status Battery Current (Charge) > IBATP_TH_SET.
0x77	INT7_STATUS	0	IBATP_TH_RES	Interrupt status Battery Current (Charge) <= IBATP_TH_SET.

3 - 13 JEITA Temperature Profile

To meet the JEITA standard, the charging profile is automatically adjusted based on the temperature detected by the thermistor in the battery pack.

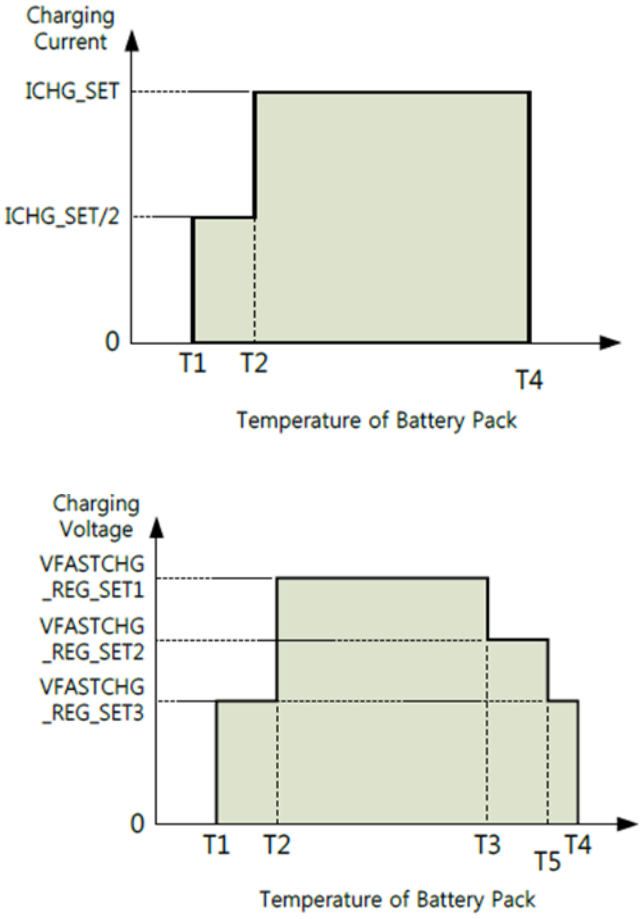


Figure 3-6. Temperature profile of charge current and charge voltage

0x40 VM_CTRL_SET 3bit THERMENB must be set to Enable and TSENSE voltage must be measured by ADC.
The T1-T5 JEITA temperature threshold window can be set via registers 0x41 to 0x45.

Table 3-17. JEITA temperature threshold window register

Code	Command	Protocols	Byte Size	Description
41h	THERM_WINDOW_SET1	Read/Write Word	2	JEITA Temperature Window Setting 1
42h	THERM_WINDOW_SET2	Read/Write Word	2	JEITA Temperature Window Setting 2
43h	THERM_WINDOW_SET3	Read/Write Word	2	JEITA Temperature Window Setting 3
44h	THERM_WINDOW_SET4	Read/Write Word	2	JEITA Temperature Window Setting 4
45h	THERM_WINDOW_SET5	Read/Write Word	2	JEITA Temperature Window Setting 5

The default values for the lower and upper thresholds for T1 to T5 are as follows

Table 3-18. JEITA Temperature Threshold Wind Register Initial Value

Register Name	Description	Default Value	Note
TMPTHR1A[7:0]	Lower threshold of T1	C6h (2 deg.)	T1 in JEITA profile
TMPTHR1B[7:0]	Upper threshold of T1	C3h (5 deg.)	T1 in JEITA profile
TMPTHR2A[7:0]	Lower threshold of T2	BEh (10 deg.)	T2 in JEITA profile
TMPTHR2B[7:0]	Upper threshold of T2	BBh (13 deg.)	T2 in JEITA profile
TMPTHR3A[7:0]	Lower threshold of T3	9Eh (42 deg.)	T3 in JEITA profile
TMPTHR3B[7:0]	Upper threshold of T3	9Bh (45 deg.)	T3 in JEITA profile
TMPTHR4A[7:0]	Lower threshold of T4	91h (55 deg.)	T4 in JEITA profile
TMPTHR4B[7:0]	Upper threshold of T4	8Eh (58 deg.)	T4 in JEITA profile
TMPTHR5A[7:0]	Lower threshold of T5	9Dh (47 deg.)	Between T3 and T4
TMPTHR5B[7:0]	Upper threshold of T5	96h (50 deg.)	Between T3 and T4

The status of the battery temperature without interrupt can be checked by reading register 0x03 bits[10:8].

Table 3-19. Battery temperature STATUS

8.5.4. CHGOP_STATUS

Charger Operation Status

Command Code: 03h
Bus Protocol: Read Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	BATTEMP[2]	Battery temperature range and the thermistor status. Please see next table.
9	BATTEMP[1]	
8	BATTEMP[0]	
7	reserved	
6	VRECHG_DET	Re-charge voltage detection status. "1": VBAT < VRECHG_SET / "0": VBAT keeps enough voltage.
5	reserved	
4	reserved	
3	reserved	
2	reserved	
1	RBOOST_UV	Reverse Buck Boost UVLO detection status. "1": Normal voltage. / "0": Low voltage.
0	RBOOSTS	Reverse Buck Boost status. "1": Boosting / "0": Not boosting.

BAT_TEMP	Temperature Range	Description
0h	Room Temp	T2 < Tbat < T3
1h	HOT1	T3 < Tbat < T5
2h	HOT2	T5 < Tbat < T4
3h	HOT3	T4 < Tbat
4h	COLD1	T1 < Tbat < T2
5h	COLD2	Tbat < T1
6h	Temp. Disable	Disable thermal control (No Thermistor)
7h	Battery Open	TSENSE_BAT port is open.

Thermistor temperature measurement

The readout of the thermistor temperature measurement converted to the detected temperature is in register 0x56.

Table 3-20. Battery temperature readings

8.5.81. THERM_VAL

Thermistor Temperature Measurement Value

Command Code: 56h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	THERM_VAL[7]	Temperature Measurement Value (200-THERM_VAL[7:0]) deg-C. -55 to 200 deg-C, 1 deg-C steps. Write Word access is available when VM_CTRL_SET.THERMENB bit = 0.
6	THERM_VAL[6]	
5	THERM_VAL[5]	
4	THERM_VAL[4]	
3	THERM_VAL[3]	
2	THERM_VAL[2]	
1	THERM_VAL[1]	
0	THERM_VAL[0]	

The interrupt threshold can be set in register 0x49, and interrupts are generated when the thermistor temperature measurement value °C in register 0x56 reaches the threshold value in register 0x49, with interrupts enabled by setting bits[5:4] to 0x6F.

Temperature setpoint interrupt setting

0x49 THERM_TH_SET can be used to set the thermistor temperature at which interrupt detection is desired.

Table 3-21. Battery temperature threshold setting for interrupt detection

8.5.68. THERM_TH_SET

Battery Temperature Interrupt Threshold Setting

Command Code: 49h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	reserved	
8	reserved	
7	THERM_TH_SET[7]	Battery Temperature Interrupt Threshold Setting (200-THERM_TH_SET[7:0]) deg-C. -55 to 200 deg-C range, 1 deg-C steps.
6	THERM_TH_SET[6]	
5	THERM_TH_SET[5]	
4	THERM_TH_SET[4]	
3	THERM_TH_SET[3]	
2	THERM_TH_SET[2]	
1	THERM_TH_SET[1]	
0	THERM_TH_SET[0]	

To enable interrupt register 0x68 bit[7] of INT7_SET: Set bit INT7_EN bit[0] of the 1st -level interrupt setting register 0x68 as described in Chapter 3-12 to Enable.

Table 3-22. Battery temperature detection interrupt configuration register

8.5.103. INT7_SET

2nd Level Interrupt Setting 7 (SAR-ADC)

Command Code: 6Fh
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	PROCHOT_DET	Interrupt of PROCHOT# asserted. "1": Enable / "0": Disable.
14	PROCHOT_RES	Interrupt of PROCHOT# de-asserted. "1": Enable / "0": Disable.
13	reserved	
12	reserved	
11	VACP_DET	Interrupt of VACP detect. "1": Enable / "0": Disable.
10	VACP_RES	Interrupt of VACP removal. "1": Enable / "0": Disable.
9	VACP_TH_DET	Interrupt Input Voltage (ACP) Voltage > VACP_TH_SET. "1": Enable / "0": Disable.
8	VACP_TH_RES	Interrupt Input Voltage (ACP) Voltage <= VACP_TH_SET. "1": Enable / "0": Disable.
7	IACP_TH_DET	Interrupt Input Current (between ACP-ACN) > IACP_TH_SET. "1": Enable / "0": Disable.
6	IACP_THE_RES	Interrupt Input Current (between ACP-ACN) <= IACP_TH_SET. "1": Enable / "0": Disable.
5	THERM_TH_DET	Interrupt TSENSE Voltage > THERM_TH_SET. "1": Enable / "0": Disable.
4	THERM_TH_RES	Interrupt TSENSE Voltage <= THERM_TH_SET. "1": Enable / "0": Disable.
3	IBATM_TH_DET	Interrupt Battery Current (Dis-charge) > IBATM_TH_SET. "1": Enable / "0": Disable.
2	IBATM_TH_RES	Interrupt Battery Current (Dis-charge) <= IBATM_TH_SET. "1": Enable / "0": Disable.
1	IBATP_TH_DET	Interrupt Battery Current (Charge) > IBATP_TH_SET. "1": Enable / "0": Disable.
0	IBATP_TH_RES	Interrupt Battery Current (Charge) <= IBATP_TH_SET. "1": Enable / "0": Disable.

TSENSE Resistance setting

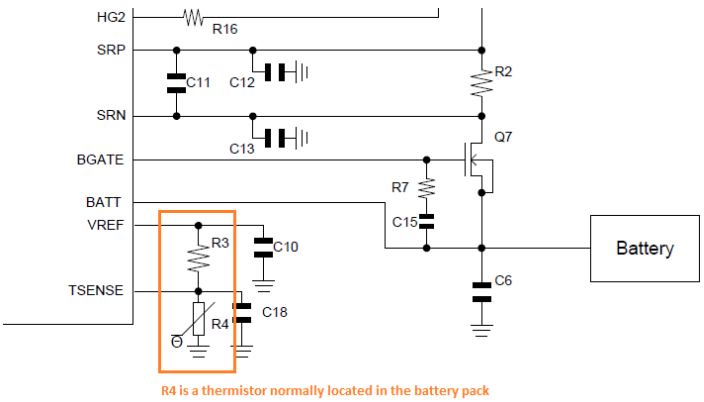


Figure 3-7. TSENSE external circuit

To set the JEITA temperature profile, connect a voltage divider resistor between VREF and TSENSE, and a thermistor between TSENSE and GND. The upper resistor should be 5.6kΩ and the thermistor should be 10kΩ with B25/85 constant = 3435K. For designs that require the use of a different thermistor, refer to the following formula.

The effective range of the TSENSE voltage is 0.1V to 1.4V. TSENSE pin voltages below 0.1V or above 1.4V cannot be used for JEITA thermal profiles.

B25 / 85 constant = 3435K When using a thermistor other than 10kΩ

Based on the resistance value of the thermistor to be used, the external resistance value of TSENSE can be calculated using the following formula.

IC internal reference voltage: Vth = 1.225V - 0.01212 x (Ta - 2°C)
RNTC_T1: Temperature of T1 of the thermistor to be used
RNTC_T5: Temperature of T5 of the thermistor to be used
RT1: TSENSE upper side resistance
RT2: TSENSE down side resistance

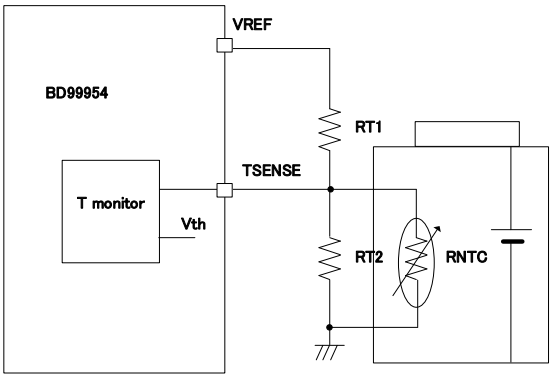


Figure 3-8. External components when connecting thermistors

$$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T5} \times \left(\frac{1}{V_{T5}} - \frac{1}{V_{T1}} \right)}{R_{NTC,T1} \times \left(\frac{1}{V_{T1}} - 1 \right) - R_{NTC,T5} \times \left(\frac{1}{V_{T5}} - 1 \right)}$$

$$RT1 = \frac{\frac{1}{V_{T1}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}}$$

4 protection function

4 - 1 Input undervoltage protection (VBUSUVLO, VCCUVLO)

Low voltage protection is detected when the voltage of VBUS and VCC voltage drops and the detection conditions are met.

4 - 1 - 1 Input undervoltage protection (VBUSVLO)

Detection condition: VBUS < 3.67V

Turn off the DCDC converter. Charging operation stops; ACGATE1 is turned off.

Release condition: VBUS > 3.8V

ACGATE1 turns on; DCDC converter turns on; if CHG_EN=1, charging operation starts.

4 - 1 - 2 Input undervoltage protection (VCCUVLO)

Detection condition: VCC < 3.67V

Turn off the DCDC converter. Charging operation stops; ACGATE2 is turned off.

Release condition: VCC > 3.8V

ACGATE2 is turned on, DCDC converter is turned on, if CHG_EN=1, charging operation is started。

4 - 2 Input overvoltage protection

Detection voltage: 25.5V±0.5V

AC_OK outputs Low.

DCDC turns off.

When the system voltage falls below the battery voltage, the BATFET is turned on.

Release voltage: 25.35V±0.5V

It returns when the input voltage falls below the release voltage.

AC_OK outputs High.

DCDC is automatically started when the input voltage falls below the release voltage.

4 - 3 System overvoltage protection (VSYS_OV)

VSYS_OV is detected when the VSYS voltage becomes high and the following detection conditions are met.

Detection conditions：

VSYS voltage is 1.1 times VSYSREG_SET

VSYS voltage is 1.1 times BATT x 1.15

When VSYS_OV occurs, the DCDC converter is turned off.

release conditions：

VSYS voltage is 1.05 times VSYSREG_SET

VSYS voltage is 1.05 times BATT x 1.15

When the VSYS voltage falls below the release voltage, the DCDC converter is automatically turned on.

4 - 4 Battery Overvoltage protection (BATOVP)

Protects the battery from overvoltage when the wrong battery is connected or when the battery is disconnected during charging.

Detection Condition: Sets the BATT OVP threshold. BATOVP_SET（0x1E）.

Charging operation is stopped and DCDC operates normally. The Battery Error of 0x00 is changed to 1.

Release condition: Complies with state machine state transition (13). There is no hysteresis voltage.

4 - 5 Battery short circuit protection

It can detect the current flowing from the battery to the system and provide status notification. 0x1F IBATSHORT_SET can set the battery short-circuit threshold from 0 to 25,000mA, with 1mA steps. When IBATM_AVE_VAL (0x53) is greater than the battery short circuit detection status: IBATM_SHORT_SET (0x1F), the watchdog timer BATTWDT_SET (0x10) WDT_IBAT_SHORT [15:8] starts counting down. When the watchdog timer time is exceeded, the VBAT / VSYS_STATUS (0x01) IBAT_SHORT bit is changed to "1".

4 - 6 System short protection (VSYS_SCP)

Detection conditions：

The timer starts when the VSYS voltage falls below VSYSVAL_THL_SET and stops with a latch after 20ms. If VSYSVAL_THH_SET or more is reached during the count, the timer will stop and reset.

Operation: All four MOSFETs are off. Charging operation also stops.

Release condition: Reinsert VBUS / VCC and return

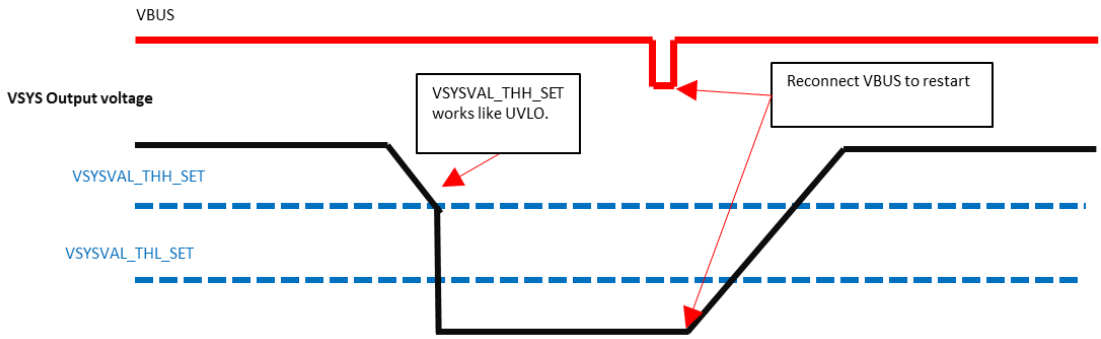


Figure 4-1. VSYSVAL_THH_SET and VSYS voltage diagram.

4 - 7 Thermal Shutdown (TSD)

When the internal chip temperature Tj of the BD99954 rises, the thermal shutdown protection function is activated under the following conditions.

Detection conditions： Tj > 175℃

release conditions：Tj < 150℃

DCDC maintains operation. Charge operation is stopped.

4 - 8 Summary of protective function operation

The DCDC and charge operation status when the protection function is activated is shown in Table 4-1. For the registers to detect the state in which the protective function has been activated, check "Detection result STATUS register" and "Judgment condition of STATUS register".

Table 4-1. Summary of protection features

protection function	Detection conditions	Release conditions	DCDC	charging operation	Input FET	Detection result STATUS register	Judgment condition of STATUS register
Input undervoltage protection VCCUVLO	VCC < 3.67V	VCC > 3.8V	OFF	OFF	OFF	0x02 8bit VCC_DET=0	VCC < 3.67V It is only a voltage judgment. Does not determine if it is in the UVLO detection state.
VBUSUVLO	VBUS < 3.67V	VCC > 3.8V	OFF	OFF	OFF	0x02 0bit VBUS_DET=0	VBUS < 3.67V It is only a voltage judgment. Does not determine if it is in the UVLO detection state.
Input overvoltage protection	VCC > 25.5V	VCC < 25.35V	OFF	OFF	OFF	0x02 11bit VCC_OVP = 1	VCC > 25.5V
						Interrupt setting 0x6A 5bit VCC_OVP_DET=1 Status bit 0x72 5bit VCC_OVP_DET=1	
	VBUS > 25.5V	VBUS < 25.35V	OFF	OFF	OFF	0x02 3bit VBUS_OVP =1	VBUS > 25.5V
						Interrupt setting 0x69 5bit VBUS_OV_DET=1 Status bit 0x71 5bit VBUS_OV_DET=1	
System overvoltage protection VSYS_OV	There are the following two patterns of VSYS voltage depending on the conditions. (1) VSYSREG_SET (2) BATT x 1.15 OVP is detected when the VSYS voltage becomes 1.1 times (1) or 1.1 times or more of (2). OVP detection conditions (1) VSYSREG_SET x 1.1 (2) BATT x 1.15 x 1.1	The OVP is released when the VSYS voltage becomes less than 1.05 times the OVP detection condition (1) or 1.05 times the OVP detection condition (2).	OFF	OFF		0x01 14bit VSYS_OV=1 Interrupt setting 0x6C 5bit VSYS_OV_DET=1 status read 0x74 5bit VSYS_OV_DET=1	VSYS_OV is 1 for all commands that stop DCDC. VBUS and VCC are not connected, VSYS_SCP detected, USUS = 1 and ALLRST = 1. VSYS over-voltage status. Two VSYS OVP detection condition. Either detected. (1) VSYS x 1.1 (2) BATT x 1.15 x 1.1 "1": VSYS > VSYS_OVP / "0": VSYS < VSYS_OVP
Battery overvoltage protection VBATOVP	0x1E [14:4] Set VBATOVP_SET. VBAT >= VBATOVP_SET	VBAT < VBATOVP_SET		OFF		0x01 3bit VBAT_OV=1	VBAT >= VBATOVP_SET
						Interrupt set 0x6B 5bit VBAT_OV_DET=1 Status bit 0x73 5bit VBAT_OV_DET	VBAT >= VBATOVP_SET
						CHGSTATE 0x00 [14:8]= 40h or 0x00 [0:6] =40h	Charger WDT finished Thermal WDT finished VBAT> = Battery Overvoltage detected
Battery short protection	0x1F [14: 0] Set IBATM_SHORT_SET. IBATM_AVE_VAL> IBATM_SHORT_SET Watchdog timer WDT_IBAT_SHORT [15: 8] has completed the countdown.	IBATM_AVE_VAL＜IBATM_SHORT_SET				0x01 6bit IBAT_SHORT=1	IBATM_SHORT_SET is larger than IBATM_AVE_VAL Count down of watch dog time BATTWDT_SET WDT_IBAT_SHORT[15:8] is completed. "1": Battery Short Current Detected / "0": Normal operation
						Interrupt setting 0x6B 7bit IBAT_SHORT_DET=1 Status bit 0x73 7bit IBAT_SHORT_DET=1	IBATM_SHORT_SET(0x1Fh) is larger than IBATM_AVE_VAL(0x53h)
System short protection VSYS_SCP	20ms have passed since the VSYS voltage became smaller than the set value of VSYSVAL_THL_SET.	The VSYS voltage becomes higher than VSYSVAL_THH_SET, shut off VBUS or VCC, and then reconnect.	OFF	OFF	OFF	0x01 13bit VSYS_SCP=1	"1": 20ms VSYS SCP timer expired. / "0": Normal operation.
						Interrupt setting 0x6C 1bit VSYS_UV_DET=1 Status bit 0x74 1bit VSYS_UV_DET=1	Interrupt function VSYS voltage <VSYSVAL_THL_SET After that, Interrupt is possible without the latch stopped for 20ms.
						Interrupt setting 0x6C 3bit VSYS_SHT_DET=1 Status bit 0x74 3bit VSYS_SHT_DET=1	Interrupt function VSYS voltage < VSYSVAL_THL_SET Interrupt is possible after 20ms of latch stop.
Thermal shutdown TSD	Junction temperature Tj > 175℃	Junction temperature Tj ＜ 175℃		OFF		0x6D INT5_SET 5bit TSD_DET 0x68 INT0_SETの5bit INT5_EN=1 0x75 INT5_STATUSの TSD_DET=1	Set 0x6D INT5_SET 5bit TSD_DET = 1 with the interrupt function of Interrupt. Set to 5bit INT5_EN = 1 of 0x68 INT0_SET. When TSD is detected, TSD_DET = 1 of 0x75 INT5_STATUS.

5 Power save mode

5 - 1 Power save mode and how to set it

The BD99954 has four power save modes, and the power save mode can be set by 0x7C POWER SAVE MODE[2:1] listed in Table 5-2. The power save mode is enabled when the battery is connected and the VBUS/VCC input is not connected. As shown in the transition diagrams in Figure 5-4 and Figure 5-5, when the input is connected and plugged in, the mode is automatically changed from power save mode to normal operation mode (0x7C=0h). When the input is connected and plugged in, the mode is automatically changed from Power save mode to Normal operation mode with 0x7C=0h. Since the register is not changed, the mode is automatically changed back to Power save mode according to the register setting when the input is plugged off. Please refer to P110-113 of the datasheet. The circuit current in power save mode in Table 5-1 does not include the current flowing to external components. In addition to the current of the IC itself, the current flows through the external resistors of the IADP/RESET, TSENE, SDA, and SCL pins as shown in Figure 5-6.

Table 5-1. Power save mode

Symbol	IBATT5	IBATT4	IBATT3	IBATT2	IBATT1
0x7C Data	0h	1h	2h	6h	5h
BGATE Charge pump	ON	ON	ON	OFF	ON
AD converter measurement	PROCHOT VSYS ISYS	PROCHOT VSYS (250μs/S)	PROCHOT VSYS (1ms/S)	-	-
Battery stand-by current	700μA	150μA	125μA	25μA	50μA

Table 5-2. Register for power save mode

Power Save Mode Setting.

Command Code: 7Ch
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	SMBREG[15]	Reserved SMBus Clock Domain Register (for future use)
14	SMBREG[14]	
13	SMBREG[13]	
12	SMBREG[12]	
11	SMBREG[11]	
10	SMBREG[10]	
9	SMBREG[9]	
8	SMBREG[8]	
7	SMBREG[7]	
6	SMBREG[6]	
5	SMBREG[5]	
4	SMBREG[4]	
3	SMBREG[3]	
2	POWER_SAVE_MODE[2]	Power Save Mode Setting. 0h: Normal Operation 1h: BGATE ON with PROCHOT# Monitored only System voltage/ 2h: BGATE ON with PROCHOT# Monitored only System voltage (1ms)/ 5h: BGATE ON without PROCHOT#// 6h: BGATE OFF/ Other: reserved.
1	POWER_SAVE_MODE[1]	
0	POWER_SAVE_MODE[0]	

When setting the power save mode, be sure to set the Normal Operation mode (0x7C=0h) first, and then set the other power save modes.

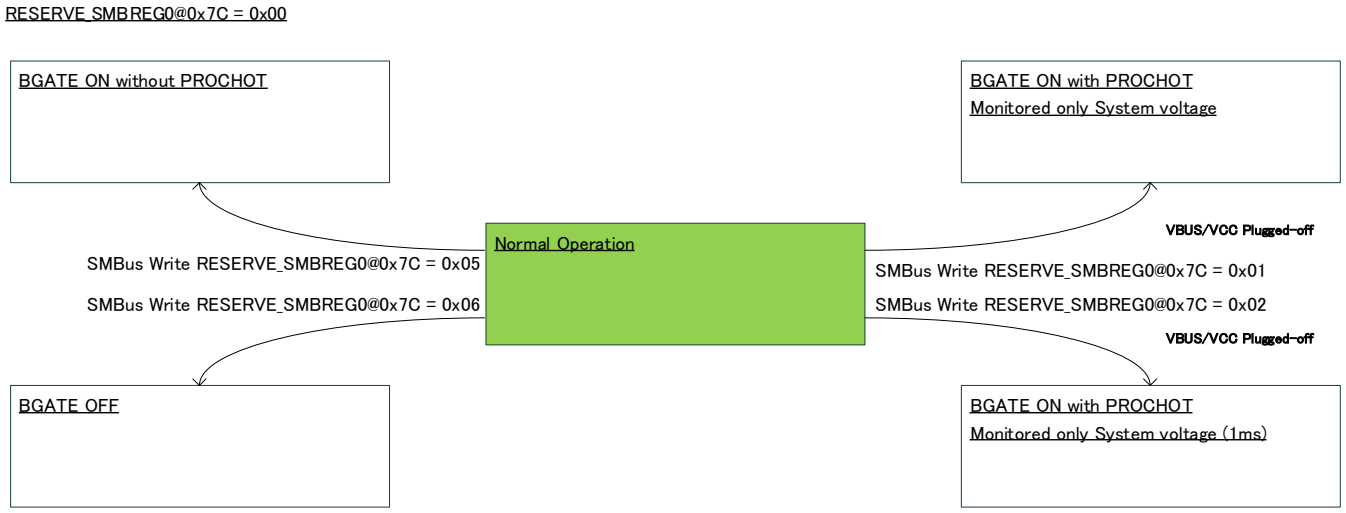


Figure 5-1. How to set Power save mode from Normal Operation

After setting to power save mode, be sure to set to another power save mode from the normal operation mode setting when setting to another mode.

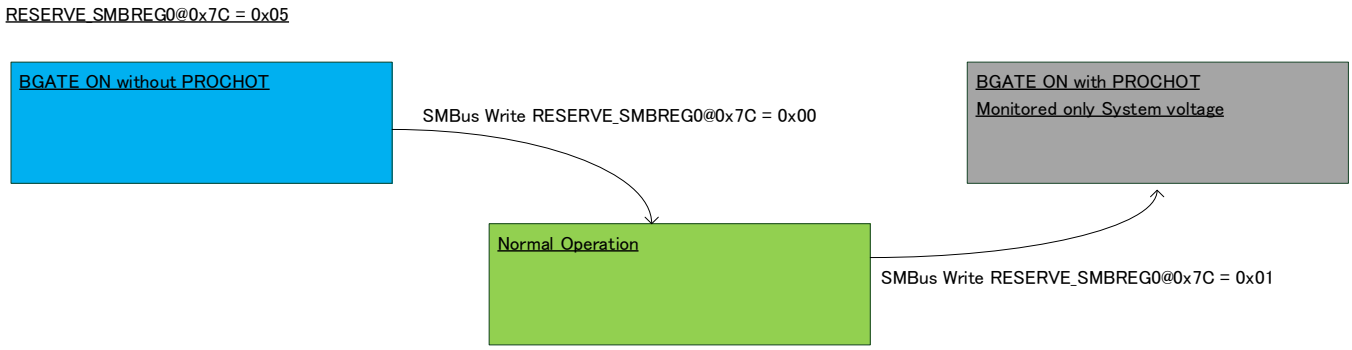


Figure 5-2. How to change Power save mode settings

It is not possible to set another mode without going through Normal mode. For example, it may not be set when transitioning from 0x7C = 5h to 0x7C = 1h. Set from 0x7C = 5h to 0x7C = 0h and then set to 0x7C = 1h.

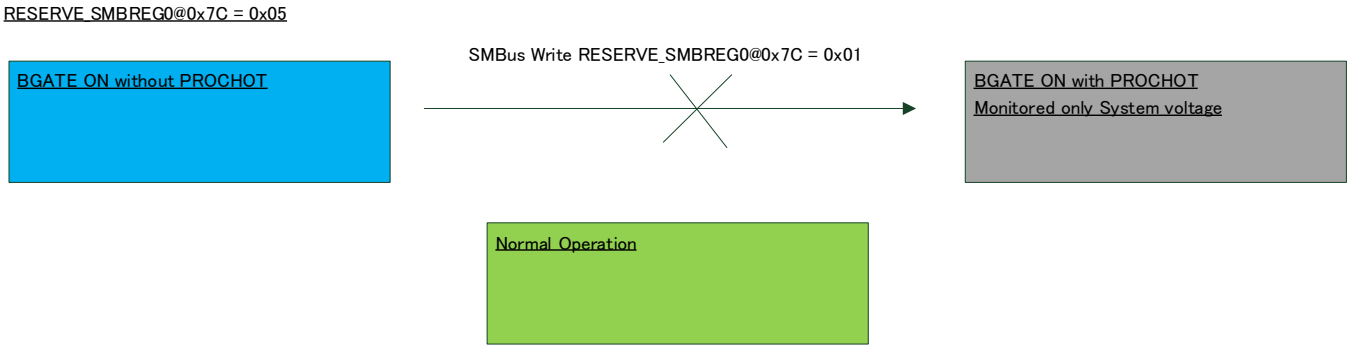


Figure 5-3. Example of Power save mode setting change failure

5 - 2 VBUS/VCC plug connection status and power save mode

When VBUS/VCC is plugged in during power save mode, it automatically transitions to Normal Operation (0x7C=0h). Since the register is held, it automatically transitions to the original Power save mode when it is plugged off again. For example, when VBUS/VCC is plugged in at 0x7C=5h as shown in the dotted line, it transitions to Normal Operation. Since 0x7C =5h is retained, it will automatically transition to power save mode with 0x7C=5h when plugged off.

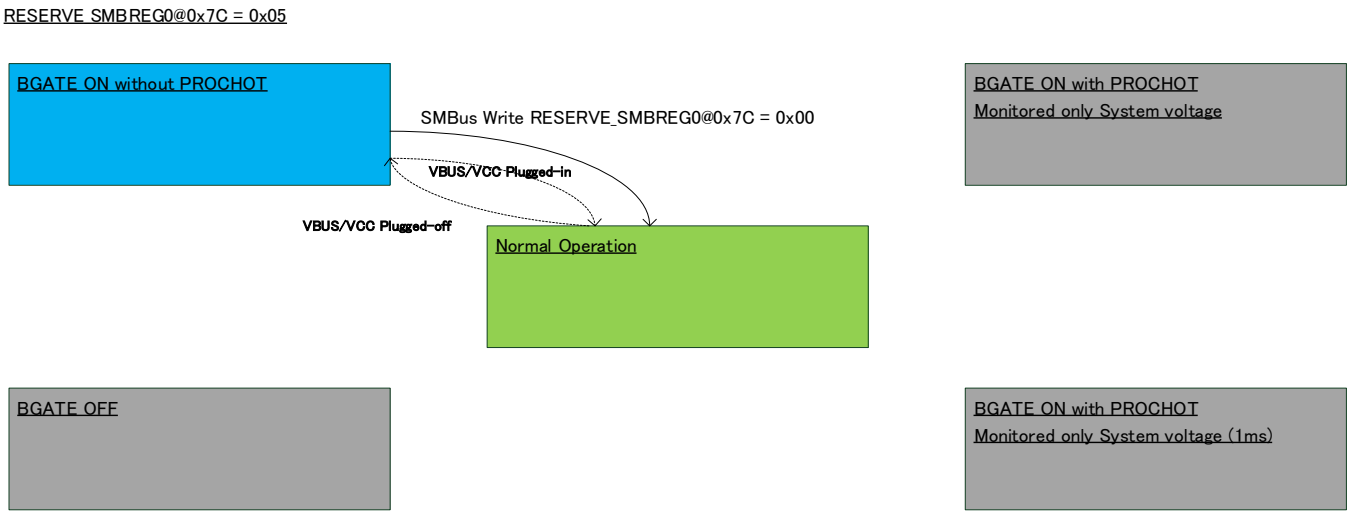


Figure 5-4. Power save mode transition when plugged in/off

Figure 5-5 on page 110 of the data sheet shows the transition diagram for the entire Power save mode. When setting to another Power save mode, it is necessary to set via 0x7C = 0h.

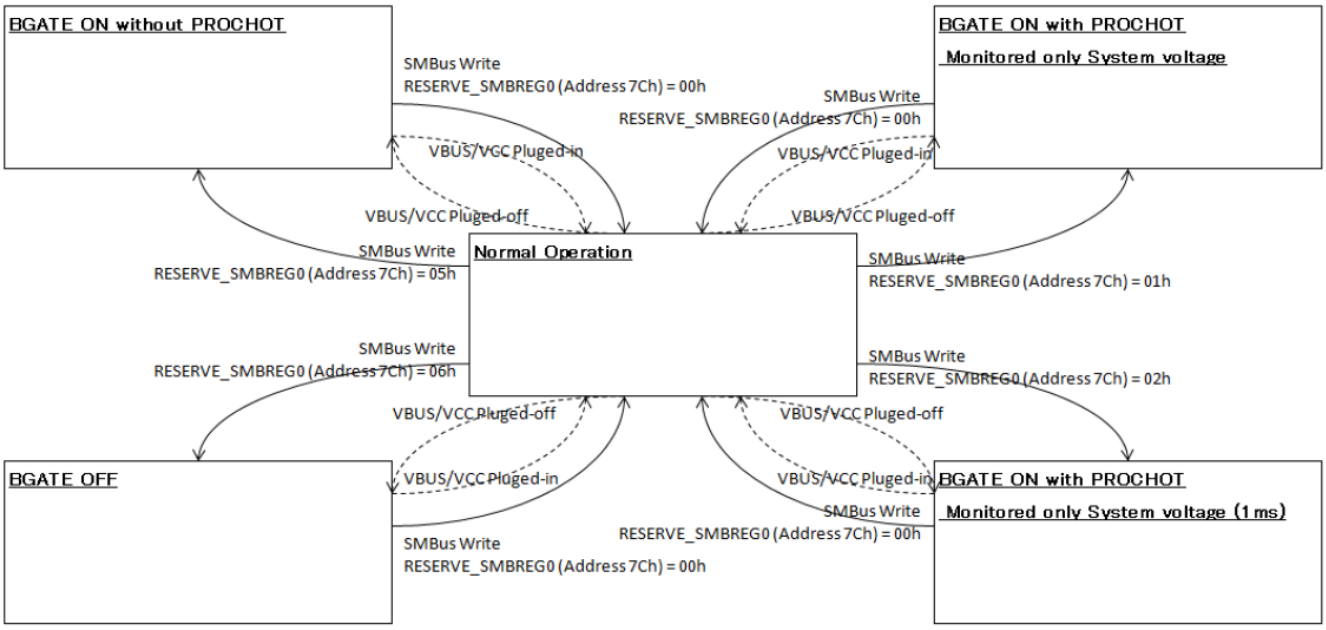


Figure 5-5. Power Save Mode Transition Diagram

5 - 3 Current path to external resistor in power save mode

During power save mode, current flows through the internal circuit to the external components. Since this can cause an increase in current, it is necessary to select the component constants according to the application. In Figure 5-6 (1), the current flows through the VREF pin to the external resistors of the IADP/RESET and TSENE pins. In Figure 5-6 (2), the current consumption of the 3.3V external power supply also flows through the pull-up resistors of SCL and SDA. In Figure 5-6 (3), when VCC_ID and VBUS_ID are connected to GND, the current flows from the battery via the internal circuit. If VCC_ID and VBUS_ID are not used, leave the pins open.

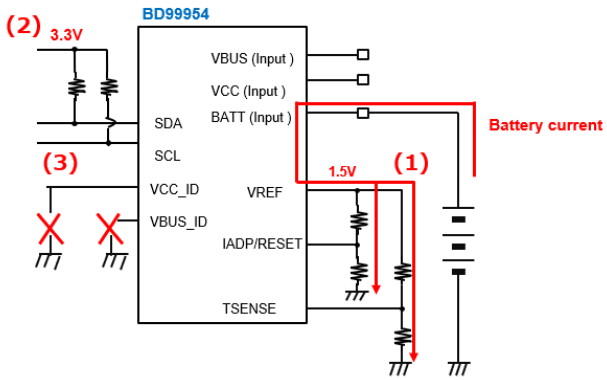


Figure 5-6. Current path to external resistor in power save mode

6 USB On-The-Go (OTG)

6 - 1 USB On-The-Go (OTG) settings

If OTG is required, the OTG output current limit, VBUS or VCC output port setting, and OTG output voltage setting must be configured. The registers that need to be set are as follows. For details, refer to the respective pages of the datasheet.

Table 6-1. OTG mode register

Address	Code name	bit	Bit name	Description
0x09	IOTG_LIM_SET	[13:5]	IOTG_LIM_SET	VBUS/VCC output current limit when OTG 0 to 16,352mA, 32mA steps.
0x0A	VIN_CTRL_SET	15	OTG_BOTH_EN	Enabling OTG reverse buck boost output to VBUS and VCC both. 1: Enable / 0: Disable When OTG_BOTH_EN=1 and VBUS_EN=VCC_EN=1, OTG reverse buck boost output same voltage at VBUS and VCC, VBUS=VCC=VRBOOST_SEL[14:6].
0x0A	VIN_CTRL_SET	14	VRBOOST_TRIG	Reverse buck Boost operation Trigger. 1: Trigger/ 0: No trigger
0x0A	VIN_CTRL_SET	13	VRBOOST_EN[1]	Enabling VCC Reverse buck Boost operation. 1: Enable / 0: Disable
0x0A	VIN_CTRL_SET	12	VRBOOST_EN[0]	Enabling VBUS Reverse buck Boost operation. 1: Enable / 0: Disable
0x19	VRBOOST_SET	[14:6]	VRBOOST_SET	Reverse buck boost voltage setting. 4,032 to 22,016mV, 64mV steps.

6 - 2 OTG start and stop

Figure 6-1 shows the timing of the start time T_{VBUS_ON} and stop time T_{VBUS_OFF} of the OTG mode described in Page10 of the datasheet. T_{VBUS_ON} and T_{VBUS_OFF} are the times when the ACP voltage starts and stops after the OTG command is input. When starting up, ACGATE1 or ACGATE2 turns on 12.8ms after the ACP voltage starts up. When off, ACP and ACGATE1 or ACGATE2 turn off after T_{VBUS_OFF} time elapses after the OTG off command is input. The rise and fall times of ACGATE1 and ACGATE2 for Trise and Tfall1 vary depending on the gate capacitance of ACGATE1 and ACGATE2. Tfall2 is the discharge time of the capacitor between VBUS and VCC.

Table 6-2. OTG mode start and stop time

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
VBUS Reverse Output turn-on Time	T_{VBUS_ON}	-	5	10	msec	
Voltage Output down-off Time	T_{VBUS_OFF}	-	1	5	µsec	

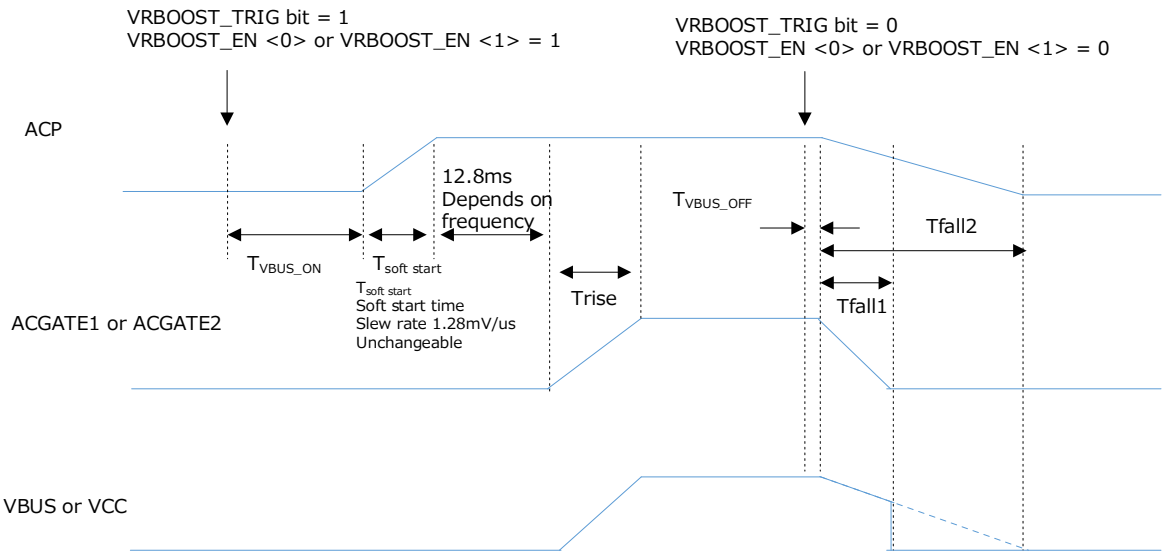


Figure 6-1. OTG mode start/stop sequence

Table 6-3 shows an example of OTG mode setting in which the output current limit is set to 5.5A and 5.056V is output to VBUS. Step 1 and 2 in Table 6-3. show the hardware reset state where the IADP/RESET pin voltage is set to less than 0.44V. For the 20ms wait time in Step2, please set 10ms or more; for the 20ms wait time in Step9, Step16, and Step19, this setting example is an example system and should be changed as necessary.

Table 6-3. Example of OTG mode register settings

Step	Step Description	SMBus command
1	Hold the reset state for 5ms.	
2	Release the reset state and wait for 20ms.	
3	Set PROTECT_SET to 0000h	write 0x3E = 0x0000
4	Set MAP_SET to 0001h.	write 0x3F = 0x0001
5	Set IOTG_LIM_SET to 5.5A	write 0x09 = 0x1580
6	Set IBUS_LIM_SET to 5.5A	write 0x07 = 0x1580
7	Set the output voltage to VRBOOST_SET.	write 0x19 = 0xXXXX
8	Set VIN_CTRL_SET to VIN_ORD.	write 0x0A = 0x0080
9	20ms Standby	
10	Set PROTECT_SET to 0032h	write 0x3E = 0x003C
11	Set MAP_SET to 0002h.	write 0x3F = 0x0002
12	Set CHARGING_CURRENT to 020Fh	write 0x14 = 0x020F
13	Set PROTECT_SET to 0000h	write 0x3E = 0x0000
14	Set MAP_SET to 0001h.	write 0x3F = 0x0001
15	Set VIN_CTRL_SET to VIN_ORD, VBUS_EN, and VRBOOST_TRIG.	write 0x0A = 0x40C0
16	20ms standby	
17	Set VIN_CTRL_SET to VIN_ORD, VBUS_EN, VRBOOST_TRIG, and VRBOOST_EN[0]	write 0x0A = 0x50C0
18	Set VIN_CTRL_SET to VIN_ORD, VBUS_EN, and VRBOOST_TRIG.	write 0x0A = 0x40C0
19	20ms standby	
20	Set VIN_CTRL_SET to VIN_ORD, VBUS_EN, VRBOOST_TRIG, and VRBOOST_EN[0]	write 0x0A = 0x50C0

If the output voltage needs to be changed, set it in the register below.

Step	Step Description	SMBus command
1	Set output voltage to VRBOOST_SET	write 0x19 = 0xXXXX

6 - 3 OTG protection function

OTG has output current limit, short circuit protection (SCP) and output over-voltage protection.

Table 6-4. Electrical characteristics of OTG mode

7.7.2. Electrical Characteristics

Table 7-6 Electrical Characteristics for Reverse Buck/Boost

Adapter=18.0V, Battery=7.4V, LX1=LX2=0.0V, GND=0V, Ta=25℃ (unless otherwise noted.)

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
<OUTPUT CURRENT Limit>						
Output Current Limit Setting Range	$I_{RADPRNG}$	0	4096	8128	mA	REG0x09h
Output Current Limit Setting LSB	$I_{RADPLSB}$	-	32	-	mA	
Output Current Limit Accuracy (10mΩ current sense resistor)	I_{RADP1}	-2%	4096	+2%	mA	REG0x09h=1000h
	I_{RADP2}	-3%	2048	+3%	mA	REG0x09h=0800h
	I_{RADP3}	-5%	1024	+5%	mA	REG0x09h=0400h
	I_{RADP4}	-10%	512	+10%	mA	REG0x09h=0200h
<Output VOLTAGE>						
Output Voltage Setting 1	V_{ROUT1}	4.95	5.0	5.05	V	REG0x19h=1380h
Output Voltage Setting 2	V_{ROUT2}	5.15	5.2	5.25	V	REG0x19h=1440h
Output Voltage Setting 3	V_{ROUT3}	8.91	9.0	9.09	V	REG0x19h=2340h
Output Voltage Setting 4	V_{ROUT4}	11.88	12.0	12.12	V	REG0x19h=2F00h
Output Voltage Setting 5	V_{ROUT5}	19.8	20.0	20.2	V	REG0x19h=4E40h
Output Voltage Setting Range	$V_{ROUTRNG}$	4.032	-	22.016	V	REG0x19h
Output Voltage Setting LSB	$V_{ROUTLSB}$	-	64	-	mV	
VBUS Buck/Boost Output Short Circuit Protection.	$V_{R}scp$	-	VBUS_UVLO VCC_UVLO	-	V	
VBUS Buck/Boost OVP Voltage	$V_{R}ovp$	-	V_{ROUT} x 1.1	-	V	
VBUS Buck/Boost OVP Detection Hysteresis Range	$V_{R}ovp\_hys$	-	V_{ROUT} x 1.05	-	mV	

Note: Resister address refer to extended commands

6 - 4 OTG mode Output current limit

When the output current exceeds the threshold of IOTG_LIM_SET at 0x09, the device works to keep the output current constant. As the output current increases further, the output voltage will decrease.

6 - 5 OTG mode Output short-circuit protection (SCP)

When the voltage drops below the voltage of VBUS Buck/Boost Output Short Circuit Protection (same as VBUS and VCC_UVLO), the 20ms counter starts as in the case of VSYS output short circuit, and after the count is completed, the latch stops. To release the latch stop state, input the input voltage, BATT, again.

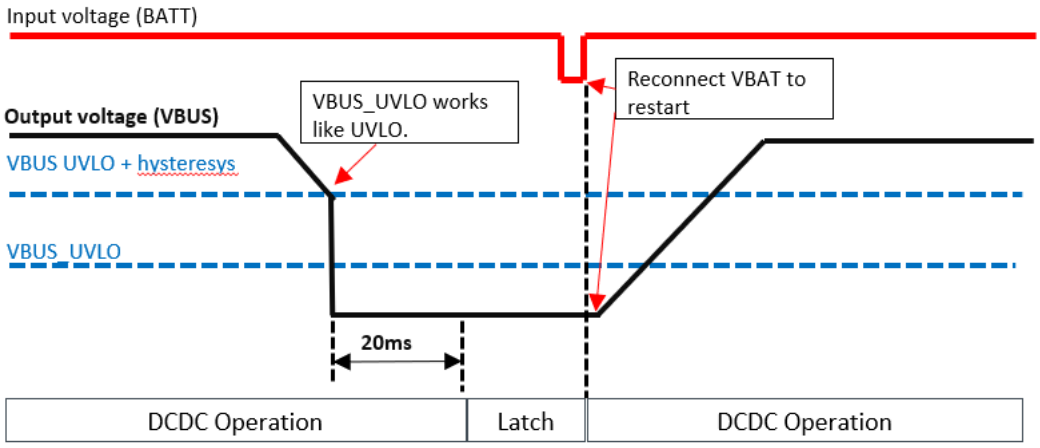


Figure 6-2. OTG mode Output short-circuit protection

6 - 6 OTG mode Output overvoltage protection

When the output voltage drops to 1.05 times of VRBOOST_SET, the overvoltage protection is released and the DCDC resumes operation.

6 - 7 DCDC behavior when OTG mode anti-collapse is detected

When the output voltage becomes lower than the anti-collapse detection voltage set by VBUSCLPS_TH_SET (0x0D) and VCCCLPS_TH_SET (0x0E), the DCDC operation stops. When the output voltage becomes higher than the anti-collapse detection voltage, DCDC operation is restored by changing VRBOOST_TRIG=0Ah from Disable to Enable.

7 Check the status

7 - 1 Charge status

You can check the charging status in Table 7-1.

Table 7-1. CHGSTM_STATUS register

0x00 CHGSTM_STATUS

bit	Bit name	Description
[14:8]	PREV_CHGSTM_STATE	The previous charging state can be confirmed.
[6:0]	CHGSTM_STATE	The current charging state can be confirmed.

7 - 2 Charge status

Table 7-2 shows the status of the battery and VSYS.

Table 7-2. VBAT/VSYS_STATUS registers

0x01 VBAT/VSYS_STATUS

bit	Bit name	Description
15	VSYS_OV	VSYS voltage is 1.05 times VSYSREG_SET When the VSYS voltage drops to 1.05 times BATT x 1.15, the DCDC restarts and releases. When DCDC is stopped by VSYS_SCP, VSYS_SCP is released by plugging and unplugging VBUS/VCC, and DCDC is started and released. DCDC starts when USB_SUS = 0 and ALLRST = 0. 1: Condition to be Detected by one of the following. (1) VSYS voltage x 1.1 (2) BATT x 1.15 x 1.1 VSYS > VSYS_OVP, VBUS, and VCC are not connected. VSYS_SCP is detected. USB_SUS=1、ALLRST=1
14	VSYS_SSD	This is not a register for detecting protection operation, but a register for detecting whether DCDC has completed soft start or not. 1: Soft-Start finished / 0: Not finished.
13	VSYS_SCP	When DCDC is stopped by VSYS_SCP, VSYS_SCP is released by plugging and unplugging VBUS/VCC, and DCDC is started and released. 1: VSYS SCP timer expired. / 0: Normal operation. It detects when the value is below the VSYS_UVLO setting (0x12 VSYSVAL_THH_SET / 0x13 VSYSVAL_THL_SET) for 20ms. Latch stop
12	VSYS_UVN	It detects when the value is below the VSYS_UVLO setting (0x12 VSYSVAL_THH_SET / 0x13 VSYSVAL_THL_SET). It returns when the value is above. 1: Low voltage. / 0: Normal voltage.
6	IBAT_SHORT	If the value of IBATM_AVE_VAL is larger than that of IBATM_SHORT_SET and exceeds the set value of Watch Dog timer WDT_IBAT_SHORT [15: 8], bit becomes 1. DCDC and charging operation do not stop. BATTWDT_SET(0x10) WDT_IBAT_SHORT[15:8] are finished. 1: Battery Short Current Detected / 0: Normal operation
3	VBAT_OV	When the BATT voltage is above the setting of 0x1E VBATOVP_SET, DCDC stops and charging operation also stops; when the BATT voltage is below 0x1E VBATOVP_SET, DCDC and charging operation are restored. 1: VBAT > VBAT_OVP / 0: VBAT < VBAT_OVP with Hysteresis
0	DEAD_BAT	This is not a detection register for protective operations. DCDC and charging operations are not stopped. 1: Dead Battery, VBAT < VSYSREG_SET, Detected / 0: Normal operation, VBAT >= VSYSREG_SET.

7 - 3 VBUS and VCC status

Table 7-3 shows the status of VBUS and VCC.

Table 7-3. VBUS/VCC_STATUS registers

0x02 VBUS/VCC_STATUS

bit	Bit name	Description
12	VACP_DET	This is not a detection register for protection operation; it detects whether VACP exceeds UVLO value or not. 1: VACP detected (over UVLO level) / 0: not detected or low level.
11	VCC_OVP	DCDC and charging operations stop while VCC_OVP is detected; DCDC operations resume when the voltage drops below VCC_OVP. 1:VCC > VCC_OVP / 0:Normal voltage. (When VCC_EN = 1) 1:VACP > VCC_OVP / 0:Normal voltage. (When VCC_EN = VBUS_EN = 0)
10	ILIM_VCC_MOD	When the input current limit value is changed by Anti-collapse, this bit is set to 1. It becomes 1 when the input current limit value is changed by Anti-collapse. 1: Limit controlled. / 0: No.
9	VCC_CLPS	This is not a register for detecting protective actions; it is set to 1 when an anti-collapse is detected. 1: VCC Anti-collapse / 0: normal operation. (When VCC_EN = 1) 1: VACP Anti-collapse / 0: normal operation. (When VCC_EN = VBUS_EN = 0)
8	VCC_DET	This is not a protection operation detection register; it detects whether the VCC voltage exceeds the UVLO value or not. 1: VCC detected (over UVLO level) / 0: not detected or low level.
3	VBUS_OVP	DCDC and charging operations stop while VBUS_OVP is detected; DCDC operations resume when the voltage drops below VBUS_OVP. 1: VBUS > VBUS_OVP / 0: Normal voltage.
2	ILIM_VBUS_MOD	When the input current limit value is changed by Anti-collapse, this bit is set to 1. 1: Limit controlled. / 0: No.
1	VBUS_CLPS	This is not a register for detecting protective actions; it is set to 1 when an anti-collapse is detected. 1: Anti-collapse / 0: normal operation.
0	VBUS_DET	This is not a protection operation detection register; It detects whether the VBUS voltage exceeds the UVLO value or not. 1: VBUS detected (over UVLO level) / 0: not detected or low level.

7 - 4 Status of charging operation, watchdog timer, OTG

Table 7-4 shows the charging operation, watch dog timer, and OTG status.

Table 7-4. CHGOP_STATUS registers

0x03 CHGOP_STATUS

bit	Bit name	Description
6	MONRST_STATE	The ADC monitor-related register values can be reset. 1: Reset asserted / 0: Reset released.
5	ALMRST_STATE	ALARM monitor-related register values can be reset. 1: Reset asserted / 0: Reset released.
4	CHGRST_STATE	The CHG state of 0x00 can be reset. 1: Reset asserted / 0: Reset released.
1	OTPLD_STATE	You can check if the OTP load is completed. 1 shows the OTPROM loading is finished./ 0: not finished.
0	ALLRST_STATE	You can check if the ALLRST at 0x3D is in Reset Status. 1: Reset asserted / 0: Reset released.

7 - 5 ADC Status

By reading the 0x3C register in Table 7-5, it is confirmed whether the 0x3D reset state is valid.

Table 7-5 . SYSTEM_STATUS registers

0x3C SYSTEM_STATUS

Bit	Bit name	Description
6	MONRST_STATE	The ADC monitor-related register values can be reset. 1: Reset asserted / 0: Reset released.
5	ALMRST_STATE	ALARM monitor-related register values can be reset. 1: Reset asserted / 0: Reset released.
4	CHGRST_STATE	The CHG state of 0x00 can be reset. 1: Reset asserted / 0: Reset released.
1	OTPLD_STATE	You can check if the OTP load is completed. 1 shows the OTPROM loading is finished./ 0: not finished.
0	ALLRST_STATE	You can check if the ALLRST in 3Dh is in Reset Status. 1: Reset asserted / 0: Reset released.

7 - 6 Resetting the status of the ADC

For ADC and ALARM monitor-related registers, writing 1 to the 0x3D register in Table 7-6 resets the status register in Table 7-5.

Table 7-6. Registers for SYSTEM_CTRL_SET

0x3D SYSTEM_CTRL_SET

Bit	Bit name	Description
6	MONRST	Resets the Status register of the ADC voltage measurement; the Setting register is not reset. 1 Reset、 0 Reset release
5	ALMRST	This function resets the Interrupt Status register, but does not reset the Setting register. 1 Reset、 0 Reset release
4	CHGRST	Reset the Battery Charge and USB Detection registers; the Setting register is not reset. 1 Reset、 0 Reset release
1	OTPLD	OTP can be loaded. 1 starts to load the OTPROM data into the internal registers.
0	ALLRST	Resets all registers for ADC voltage measurement, Interrupt, Battery charging and USB detection. 1 Reset、 0 Reset release

8 Application data

8 - 1 Input current limit IBUS_LIM_SET=1024mA, VSYS=5.8V

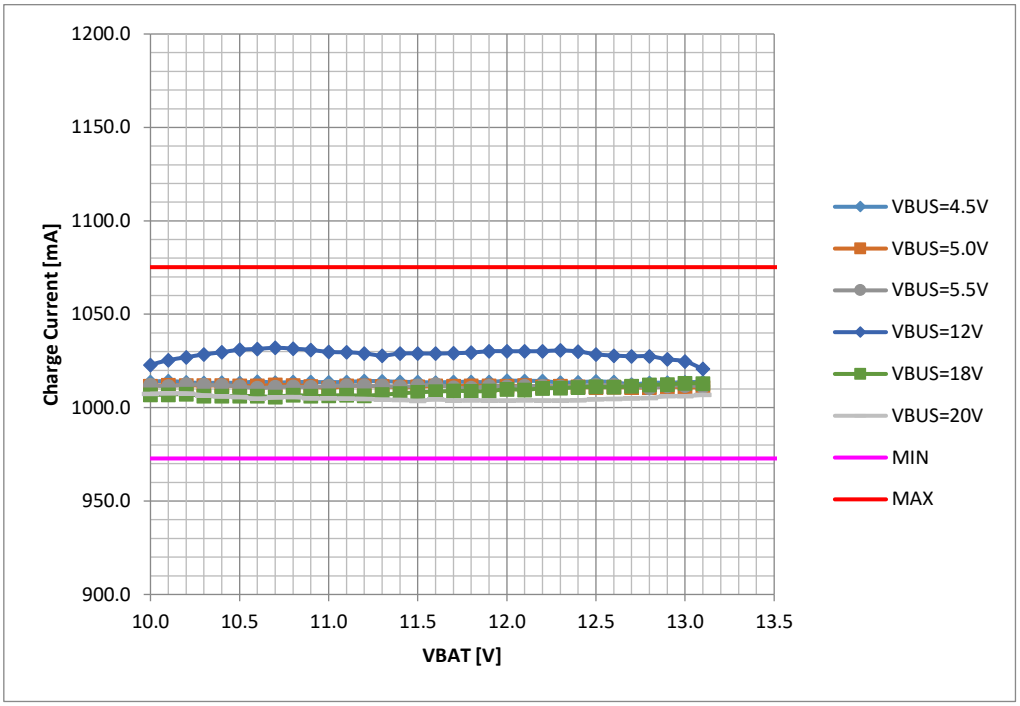


Figure 8-1. VBAT vs Input Current Limit Data

8 - 2 Charge current ICHG_SET＝1024mA、VSYS=5.8V

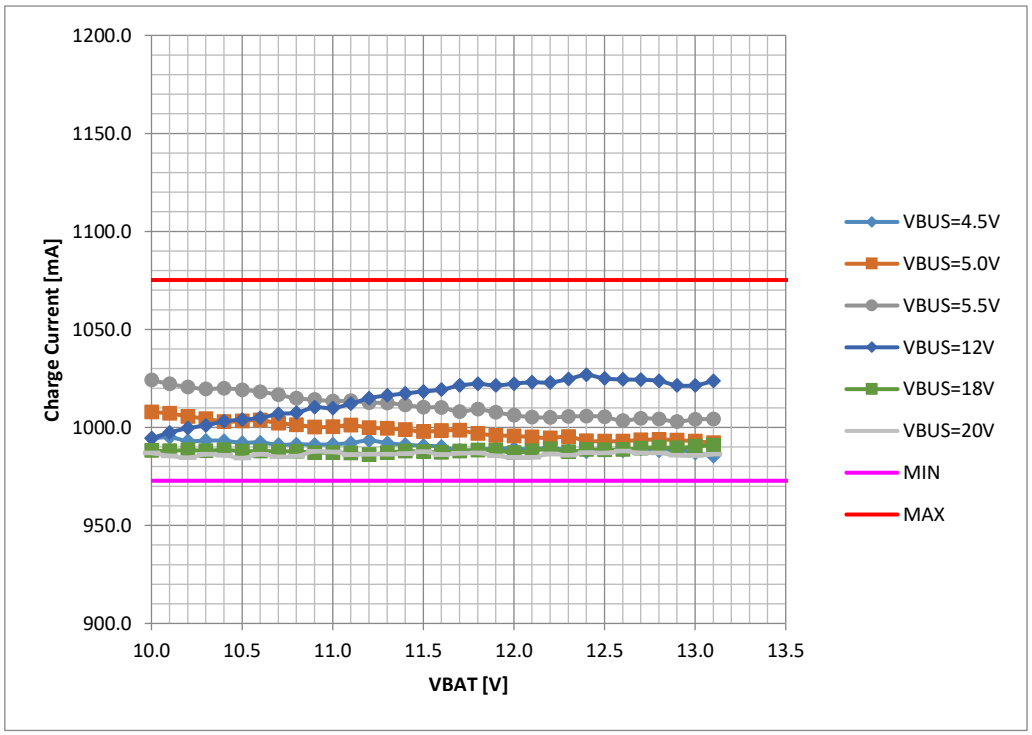


Figure 8-2. VBAT vs charge current data

8 - 3 Charge voltage VFASTCHG_REG_SET1＝13.2V、VSYS=9.2V

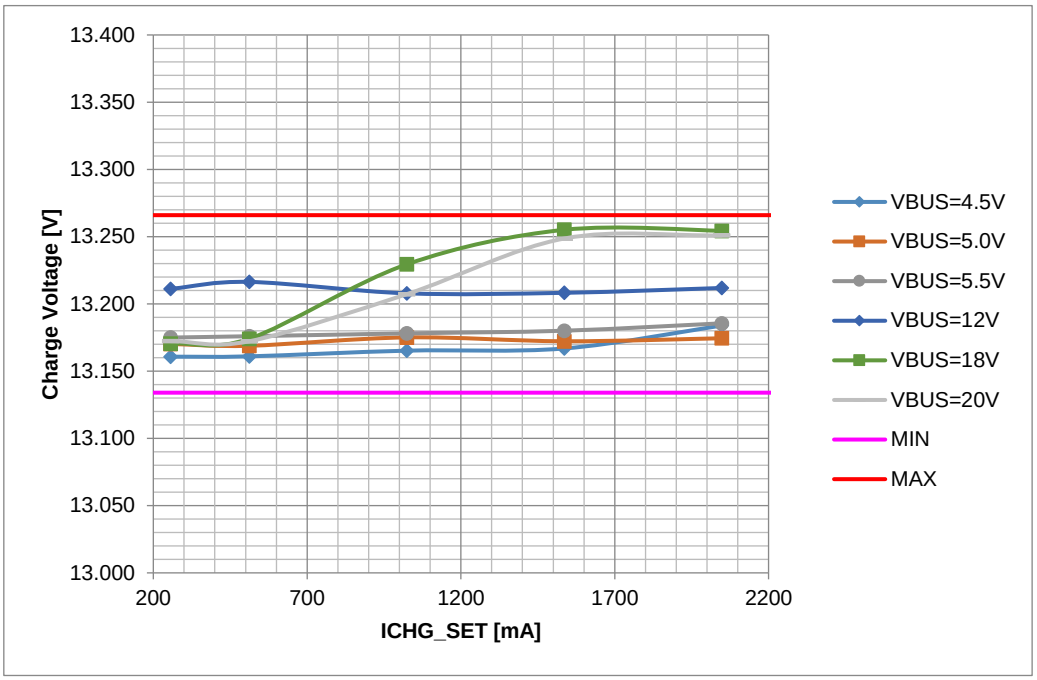


Figure 8-3. Charge current vs. charge voltage data

8 - 4 Step-up/step-down DCDC efficiency

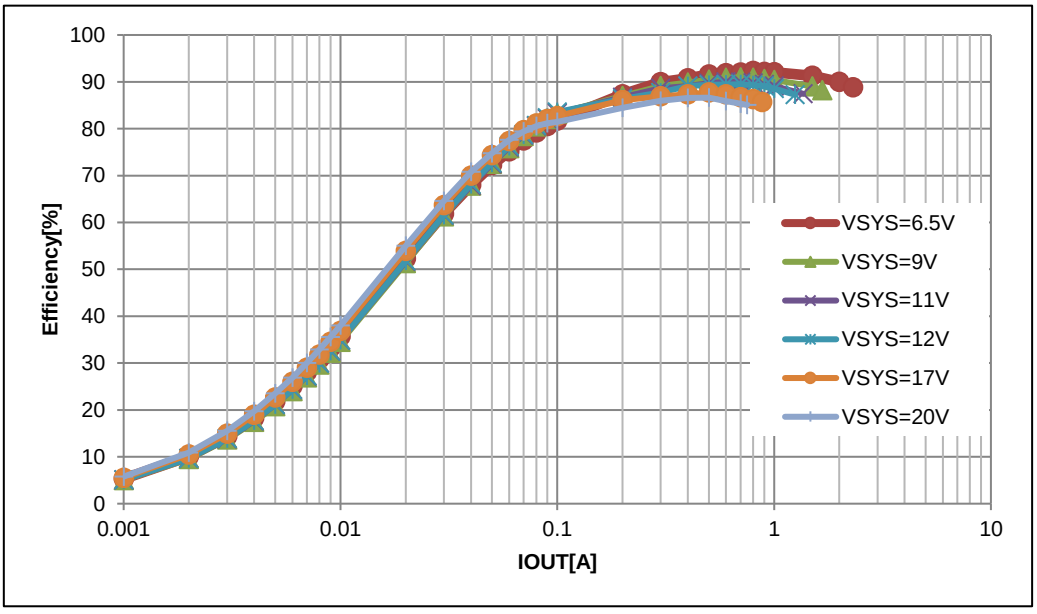


Figure 8-4. VBUS = 5V Efficiency data

Efficiency data (continued)

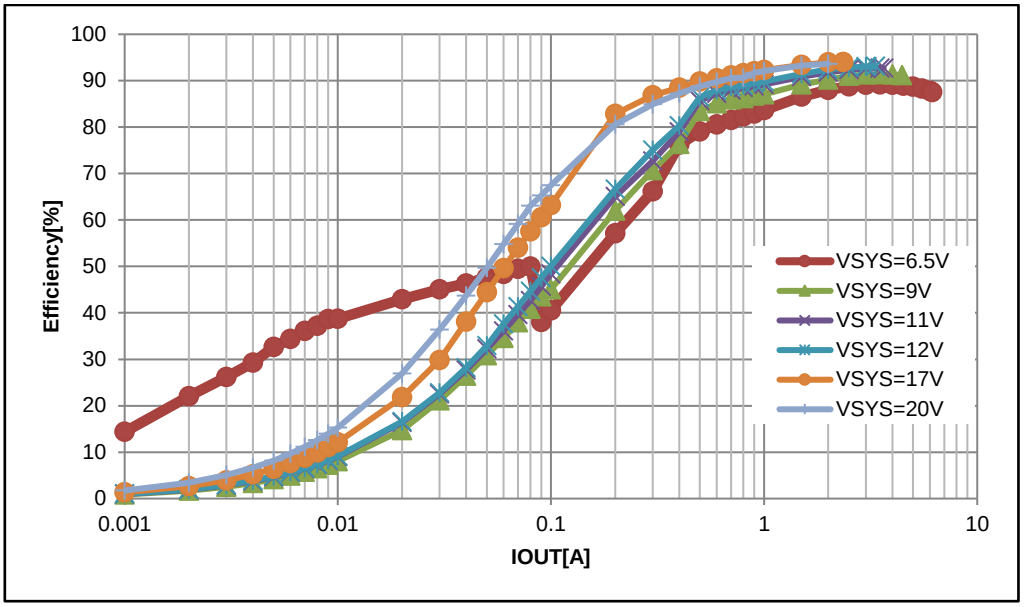


Figure 8-5. VBUS = 20V Efficiency data

8 - 5 Step-up/step-down DCDC load transient response

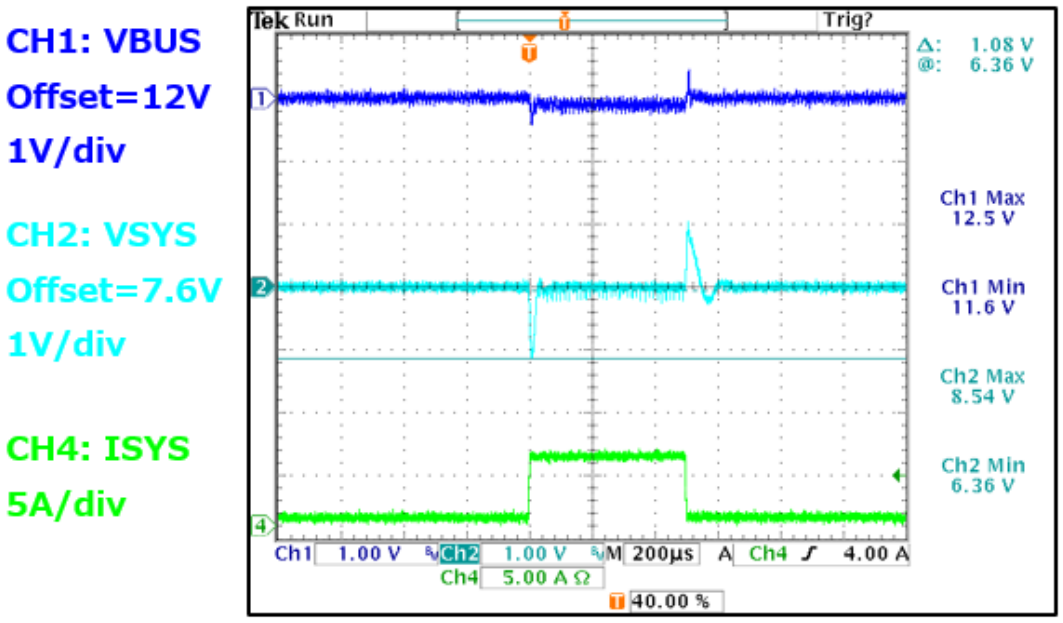


Figure 8-6. VBUS = 12V、VSYS=7.6V Iout = 0.5A ⇔ 5.3A

9 Parts selection

9 - 1 ACP-ACN Input current sensing resistor

・RAC = 10mΩ

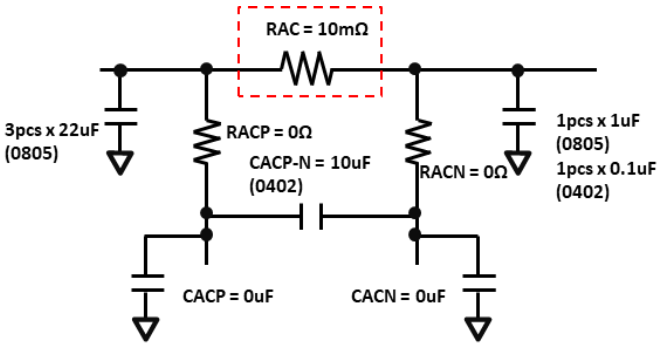


Figure 9-1. ACP-ACN circuit: Input current sensing resistor

9 - 2 ACP-ACN Input filter

・Input capacitor= 22μF（25V）×3pcs

If a ceramic capacitor is used and audible noise is generated, use a tantalum polymer capacitor.

・ACN Resistance（RACN）=0Ω

Internal circuit current is flowing. The input current limit becomes smaller due to voltage drop.

・ACP Resistance（RACP）=0Ω

・Capacitors between ACP and CAN（CACP-N）= 10μF

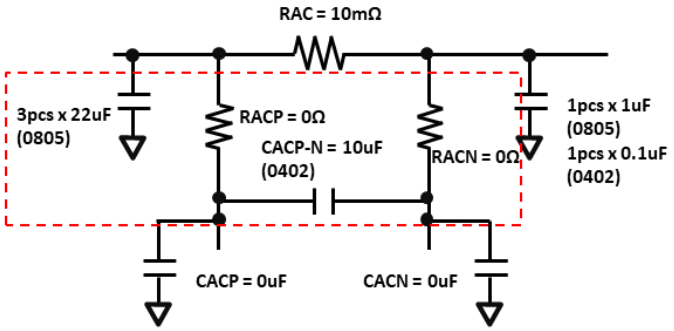


Figure 9-2. ACP-ACN circuit: Input current filter

9 - 3 Inductors

The BD99954 has four selectable fixed switching frequencies.

The recommended inductance is 2.2μH. The inductor saturation current should be higher than the input current (I_{IN}) plus half of the ripple current (I_{RIPPLE}) during boost operation. It should be higher than the load current Iout during step-down operation plus half the ripple current. The following formula is the formula for calculating the I_{SAT} current during boost operation. When stepping down, replace I_{IN} with Iout for calculation.

$$I_{SAT} = I_{IN} + \frac{1}{2}(I_{RIPPLE})$$

The inductor ripple current in step-down operation depends on the input voltage (V_{IN}), duty cycle ($D_{BUCK} = V_{OUT}/V_{IN}$), switching frequency ($f_S$), and inductance (L).

$$I_{RIPPLE\_BUCK} = \frac{V_{IN} \times D_{BUCK} \times (1 - D)}{f_S \times L}$$

The duty cycle during voltage multiplier operation is (D_{BOOST} = 1 - (V_{IN}/VBAT)).
The ripple current is as follows

$$I_{RIPPLE\_BOOST} = \frac{V_{IN} \times D_{BOOST}}{f_S \times L}$$

9 - 4 Input capacitor

The input capacitor should be selected with a ripple current rating greater than the input switching ripple current. The RMS ripple current is half of the input current IIN when the duty cycle is 50% in buck mode. The RMS current of the capacitor occurs where the duty cycle is closest to 50% and can be estimated as follows

$$I_{CIN} = I_{IN} \times \sqrt{D \times (1 - D)}$$

Low ESR ceramic capacitors, such as X7R and X5R, are suitable for input decoupling capacitors and should be placed as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. The voltage rating of the capacitor should be higher than the normal input voltage level. Select a capacitor with a 25V rating or higher.
Ceramic capacitors have a DC bias effect Due to this effect, when a DC bias voltage is applied to both ends of a ceramic capacitor, the effective capacitance is reduced. Particularly when the input voltage is high and the capacitor package is small, the capacitance may be significantly reduced. Please refer to the manufacturer's information.
It may be necessary to select a higher voltage rating or nominal capacitance value, assuming a DC bias voltage is applied.

9 - 5 VBUS, VCC input capacitor

For an input voltage of 19V to 20V, it is recommended to use at least one capacitor of 4.7μF 0805 size.

9 - 6 ACP input capacitor

For an input voltage of 19V to 20V, it is recommended to use three or more 22μF 0805 size capacitors.

In addition, audible noise is generated when ceramic capacitors are used. If audible noise is unacceptable, use a 22μF tantalum polymer capacitor.

For example: T521B226M025ATE100：22μF、25V、1411 size

9 - 7 ACN input capacitor

Connect a 1μF capacitor; note that connecting more than 1μF will cause instability in the VSYS output.

9 - 8 Output capacitor（VSYS）

The output capacitor must also have a ripple current rating that is sufficient to absorb the output switching ripple current. The RMS current of the output capacitor is given by
Audible noise is generated when using ceramic capacitors. If audible noise is unacceptable, use a 22μF tantalum polymer capacitor.

For example: T521B226M025ATE100：22μF、25V、1411 size

9 - 9 BATT Capacitor

Audible noise is generated when using ceramic capacitors. If audible noise is unacceptable, use a 22μF tantalum polymer capacitor.

For example: T521B226M025ATE100：22μF、25V、1411 size

In OTG mode, the device operates in Reverse Buck-Boost mode, which means that it outputs from the battery to VBUS and VCC. It may be necessary to select a higher voltage rating or nominal capacitance value, assuming that a DC bias voltage is applied as described in the input capacitor section.

9 - 10 Power MOSFETs

9 - 10 - 1 How to select Power MOSFETs

Four external N-channel MOSFETs are used in the synchronous rectification switching battery charger IC. The gate driver outputs a gate drive voltage of 5.2V from the IC's internal power supply. For an input voltage of 19V to 20V, a MOSFET with a voltage rating of 30V or higher is recommended.

The gate charge Qg of each MOSFET should be selected so that it is less than 20nC.

MOSFET losses include conduction losses and switching losses. Duty cycle ($D = V_{OUT} / V_{IN}$), input current (I_{IN}), on-resistance of MOSFET ($R_{DS(ON)}$), input voltage (V_{IN}), switching frequency (f_S), turn-on time (t_{on}) off-time (t_{off})

$$P_{top} = D \times {I_{IN}}^2 \times R_{DS(ON)} + \frac{1}{2} \times V_{IN} \times I_{IN} \times \left(t_{on} + t_{off}\right) \times f_S$$

The first item represents the conduction loss. Typically, the MOSFET $R_{DS(ON)}$ increases by 50% as the junction temperature increases by 100°C. The second term represents the switching loss. These are the turn-on and turn-off times of the MOSFET.

The conduction loss of a low-side MOSFET, when operating in synchronous rectification continuous conduction mode, can be calculated by the following equation

$$P_{bottom} = (1 - D) \times {I_{IN}}^2 \times R_{DS(ON)}$$

When the BD99954 is operating in asynchronous mode, the low-side MOSFET during buck operation and the high-side MOSFET during boost operation are turned off. As a result, the freewheeling current passes through the MOSFET body diodes. The power dissipation of a body diode depends on its forward voltage drop (V_F), its current in asynchronous mode ($I_{NONSYNC}$), and its duty cycle (D).

$$P_D = V_F \times I_{NONSYNC} \times (1 - D)$$

9 - 10 - 2 Precautions for using Power MOSFETs

For applications with large load currents, MOSFETs with high power dissipation should be selected and a single FET should be used instead of in parallel.

The use of MOSFETs in parallel is not recommended for the following reasons

- ・The danger of high-side and low-side through-current
- ・Heat is not evenly distributed.

9 - 11 DCDC FET Gate Resistance

Each gate resistance must be less than 10Ω. 0Ω is also possible.

9 - 12 BATFET

During trickle charge and pre-charge, current flows from the VSYS voltage to the battery. Since it works like an LDO, loss FET_{loss} is generated by the voltage difference ΔV between VSYS and the battery and the charging current. If the potential difference is large and the charge current is large, the heat generated by the FET will be large. As a countermeasure, select a FET with high power dissipation and pay attention to the thermal design.

$$FET_{loss} = \Delta V \times ITRICH\_SET$$
$$\Delta V = VSYSREG\_SET - VBAT_{minimum}$$

9 - 13 BATFET Gate resistor and capacitor

The resistance between BGATE and BATT is 470Ω, and a 0.1μF capacitor is connected. BGATE outputs a constant current of 6μA to turn on the gate of BATFET. If a FET with Vgs of 2.5V is used, the delay time with a 0.1μF capacitor is 42ms. 470Ω and 0.1μF is also a phase compensation circuit. When CBGATE is 3300pF, use a resistance of 1kΩ for RBGATE (see 11-1 Phenomena Caused by Long Time Until BGATE Turns ON and Workarounds).

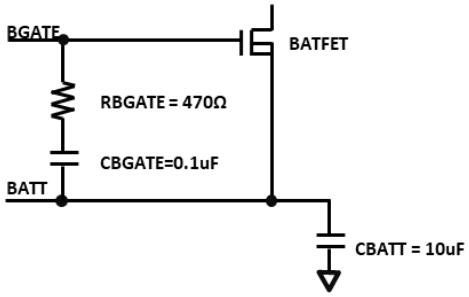


Figure 9-3. BATFET Gate resistor and capacitor circuit

9 - 14 Charge current detection resistor and filter

We recommend 10mΩ for the charge current detection resistor. If you want to set it smaller than 300mA termination current, you can set it to 20mΩ as described in 3-5 Termination current. Connect a 0.1μF capacitor to the SRN and SRP pins as a filter for detecting the charge current, as shown in Figure 9-4.

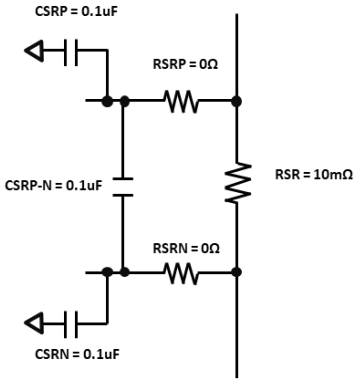


Figure 9-4. Charge current filter circuit

9 - 15 VREF Capacitor

VREF is the 1.5V output of the internal reference circuit. The recommended capacitor is 1μF.（10μF is connected to EVK, but use 1μF.）

9 - 16 REGN Capacitor

REGN is the 5.2V output of the internal reference circuit. The recommended capacitor is 10μF.

9 - 17 BOOT1, BOOT2 Capacitor

The recommended BOOT1 and BOOT2 capacitors are 0.1μF / 50V.

9 - 18 ACGATE1, ACGATE2 Capacitor

It is recommended to connect 0.1μF as a countermeasure against rush current.

9 - 19 TSENSE Resistors, Thermistors and Capacitors

When using a thermistor, use RTS2 and thermistor 10kΩ, B: 3435K.

(Example.)

Thermistor = NTCG063JF103FTB

(B constant [25/85°C])

When using a thermistor, the pull-up resistor RTS1 is 5.6kΩ.

It is recommended to connect a filter capacitor of 0.1μF between TSENSE and GND.

If the thermistor is not used, remove RTS1 and pull down RTS2 to GND with 10kΩ.

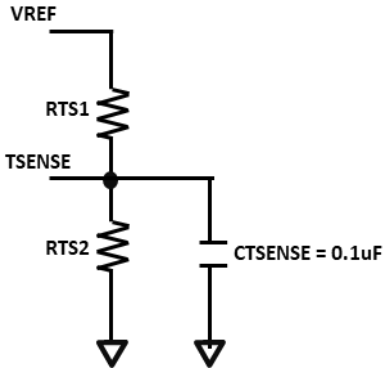


Figure 9-5. TSENSE resistor circuit

9 - 20 SCL, SDA pull-up resistor

The BD99954 is SMBus2.0 compliant. However, it is not fully compliant. It operates at an operating frequency of 400 kHz. If this is the case, please change the pull-up resistor. EVK is 47kΩ pulled up to 3.3V external power supply.

9 - 21 IADP/RESET resistance

The initial value of the input current limit is set by IADP / RESET. When DCDC is operating, the initial value of the input current limit continues until the input current limit is set from the host.

The resistance from VREF to GND becomes the current consumption. When using only a battery, set the resistor value large enough so that the sum of RIADP1 and RIADP2 is less than 200kΩ, because the current consumption may increase in the power save mode.

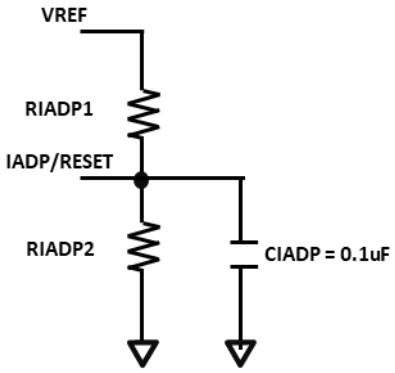


Figure 9-6. IADP/RESET resistor circuit

10 Layout pattern

10 - 1 Layout pattern notes

・Lower the impedance between the input current sensing resistor and the ACN pin.

・The ACN and ACP terminals of the input current sensing resistor should be wired independently so that there is no common impedance.

・The charge current detection resistor and the STN and SRP pins should be wired independently so that there is no common impedance between them.

・ The drain of the MOSFET of the DCDC and the SRP pin side of the charge current detection resistor are connected with low impedance.

・GND is connected to the two layers with low impedance.

・The path through which the switching current flows should be wired in the shortest possible length. (CIN-FET-COUT).

・LG1, HG1, LG2, HG2, LX1, and LX2 do not parallel or cross VREF, REGN, or SRP.

・IADP/RESET, SRN, ACN, ACP, IADP/RESET, TSENSE, VBUS_DPI, VBUS_DMI, VCC_DMI, VCC_DPI and switching signals are not parallel or crossed.

・The GND pin is connected to the thermal pad of the QFN package.

・To improve the thermal design, place many vias and connect them to GND.

・Place more vias on the GND side of the REGN capacitor.

10 - 2 Layout pattern example

The circuit diagram in Figure 10-1 shows the components where the current flows during switching operation. An example layout pattern is shown in Figure 10-2.

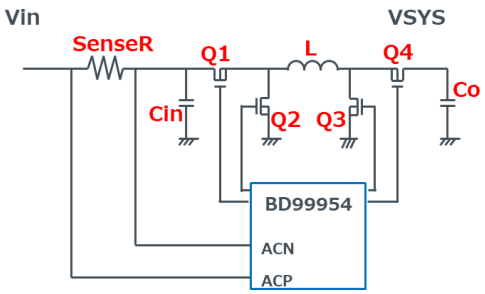


Figure 10-1. BD99954 Schematic Circuit

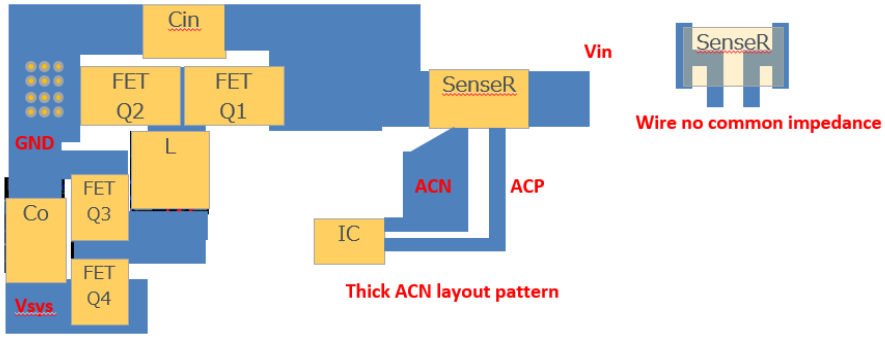


Figure 10-2. BD99954 Layout Pattern

11 Phenomena that are easy to face and their workarounds

11 - 1 Phenomena caused by the long time before BGATE turns on and workarounds

Figure 11-1 (excerpted from Figure 1-1 of the datasheet) shows the BGATE peripheral application circuit, where R7 and C15 are filters for phase compensation of Q7, the BGATE charge path switch. Due to the time constant of this filter, it takes some time before Q7 is turned on. During this time, the system voltage will be the BATT voltage minus the Vf of the body diode of Q7. At this time, if the battery level is low and the current supply capability of the adapter is low, the system may shut down. As a workaround, change the phase compensation constant according to the following formula: C15 can be set up to 3300pF; use 1kΩ for R7 when C15 is 3300pF.

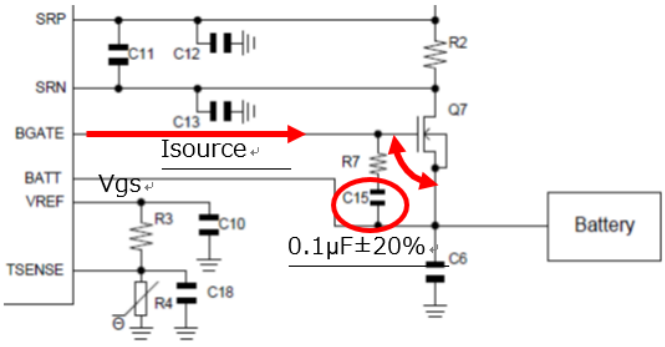


Figure 11-1. Factors that determine the time until BGATE turns on

The phase compensation constant and the time to turn on Q7, Ton, are calculated by the following formula and are 42ms.

Ton = C15 x Vgs/Isource

BGATE capacitor C15 : 0.1μF ±20% (Ignore gate capacitance of Q7 as it is small compared to C15)
Charge MOSFET Q7 threshold max : 2.5V (when using ROHM MOSFET RQ3E120GN)
BGATE current Isource : 6μA ±50%

Table 11-1. Ton time at the current phase compensation constant

	Min	Typ	Max
Ton(ms)	22	42	100

11 - 2 Reverse current from battery to input during DCDC startup and how to avoid it

With VBUS/VCC connected and bit7: CHG_EN = 1 (charge enable) of 0x0C: CHGOP_SET2, when bit6: USB_SUS = 1 (DCDC = OFF) -> 0 (DCDC = ON) of 0x0C: CHGOP_SET2, current flows from BATT to VBUS/VCC (reverse current).

This mechanism is illustrated in Figure 11-2a (added to Figure 1-1 on page 4 of the datasheet).

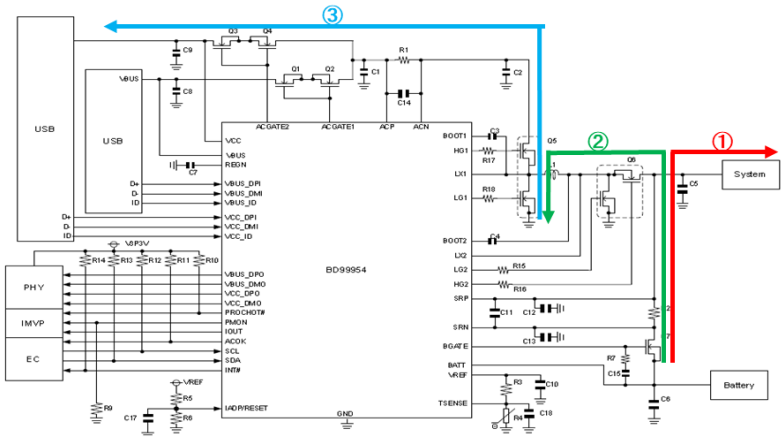


Figure 11-2a. Mechanism of reverse current generation

(1) Input current limit is so small that system voltage does not start and current is supplied from VBATT

(2) Since the step-up/step-down DCDC for system voltage generation is operating and the current supply from VBUS is small, the operation of the step-up DCDC with VBATT as the power supply
Low side FET of LG1 turns on and current flows from VBATT to inductor to low side FET.

(3) When Low side FET turns off, current to VBUS side is supplied and reverse current to VBUS is generated.

When 0x0C: bit 0 of CHGOP_SET2: CHOP_ALL = 1, the asynchronous rectification mode is set, so the FETs of LG1 and HG2 are turned off during switching operation. This means that even if the system voltage becomes lower than the VBATT voltage and current is supplied from VBATT, the FET body diode of the FET will block the reverse flow.

However, CHOP_ALL is reset when VBUS/VCC is inserted, so please set it to 1 during the timing chart shown in Figure 11-2b (added to the upper figure of datasheet P18).

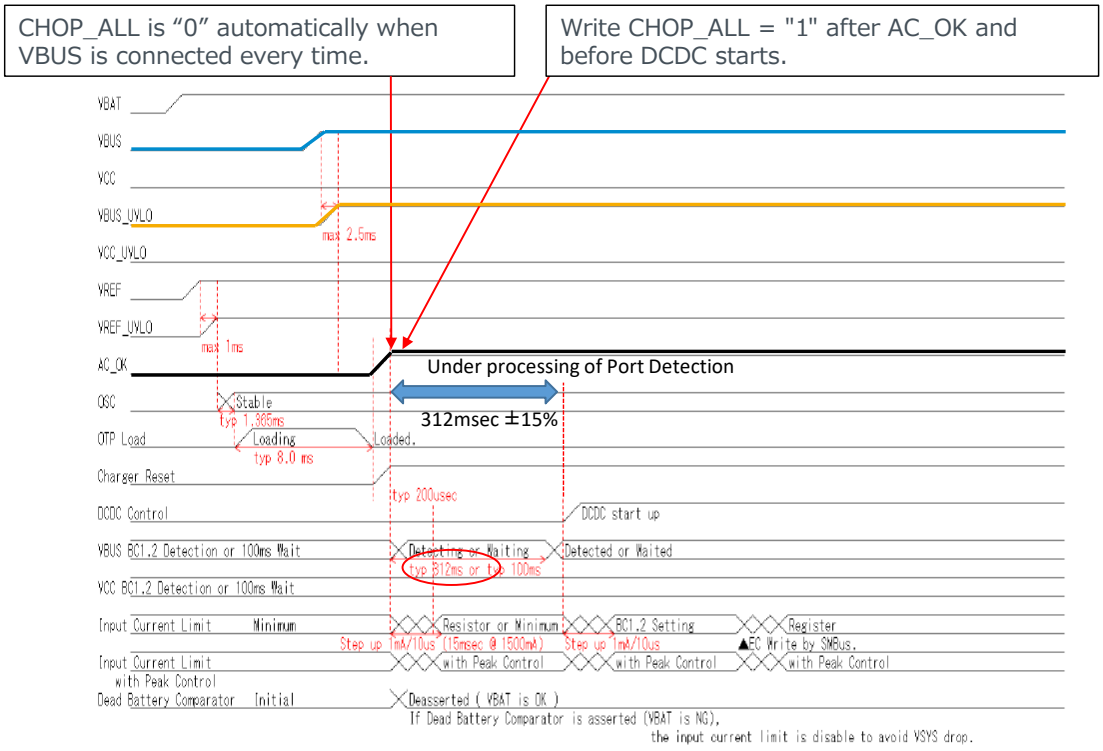


Figure 11-2b. Timing to write CHOP_ALL = 1

11 - 3 DCDC Input/Output capacitor noise and workaround

The buck-boost DCDC of BD99954 has intermittent switching operation, when improving efficiency at light loads, preventing backflow current from the battery to the input, and switching between boost, step-down, and buck-boost operation modes. Since the intermittent cycle is in the audible band, the ceramic capacitors in the input and output generate the intermittent cycle sound.

As for the adverse effects of noise on the set, check the effects in the EVK evaluation and determine whether or not countermeasures are necessary for the actual set.

There are two ways as this countermeasure.

Changed to a capacitor type that does not generate noise due to physical distortion due to the piezoelectric effect
-- > ①.

Control the switching cycle so that it does not fall into the audible band-->②, ③.

The explanations are given below in order.
①Input/output capacitor is changed to POSCAP (dielectric polymer capacitor).

Figure 3-3a shows the corresponding capacitor in a circle. The following priorities apply to these measures, which should be implemented after evaluation and confirmation on the actual set board.

(Priority 1) Capacitors close to DCDC and large capacitance = = > C5

(Priority 2) Capacitors close to DCDC = = > C2

(Priority 3) Others ＝=> C1,C6,C8,C9

Measures will be taken with the above priority.
In addition, C8 and C9 need only the capacity required for the port used in the actual set specifications.

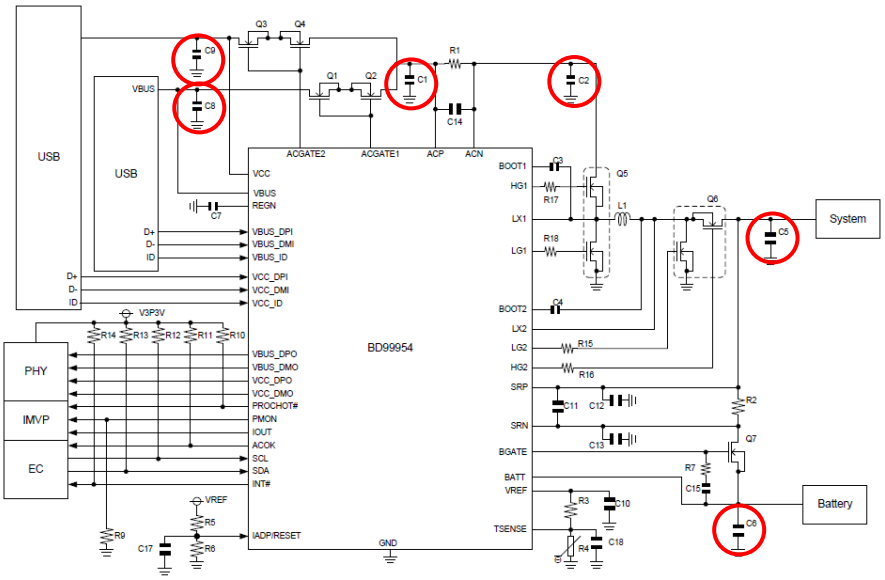


Figure 11-3a. Capacitors that may require noise reduction

②A switch is provided between the battery and the CV mode operation at all times.

The BD9954 is equipped with a DCDC converter that changes its operation mode from buck, buck-boost, to boost, depending on the input and output voltages. Figure 11-3b shows how this works.

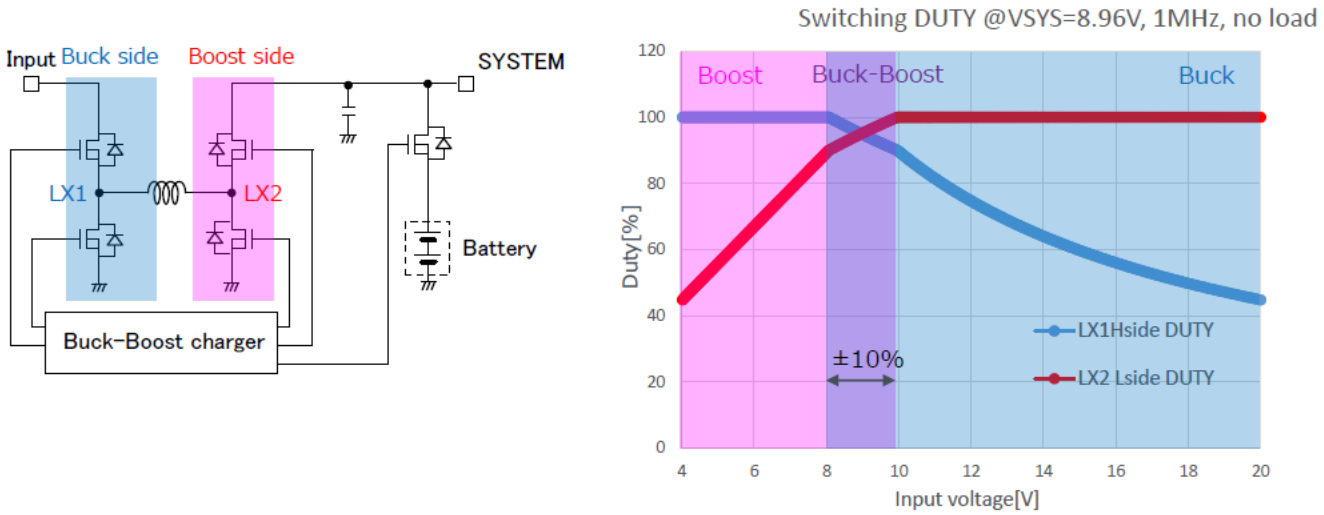


Figure 11-3b. About step-up/step-down control

When switching the operation mode (the edge of the dark part on the right of Figure 11-3b), the minimum ON pulse is output, but this pulse becomes intermittent due to changes in the output voltage. For example, at the left edge, there is a pulse output ⇒ output voltage rise ⇒ no pulse output ⇒ output voltage falls repeatedly. At this time, since the pulse becomes intermittent, the pulse frequency drops and the frequency enters the audible band, so that the distortion of the ceramic capacitor can be heard as sound.

As a countermeasure, add a switch FET (circled in red) as shown in Figure 11-3c to prevent the DCDC switching pulse from being intermittent. Table 11-3 shows the control table of the additional FET and the countermeasures. The gate of the FET for the switch is controlled by GPIO of the host CPU.

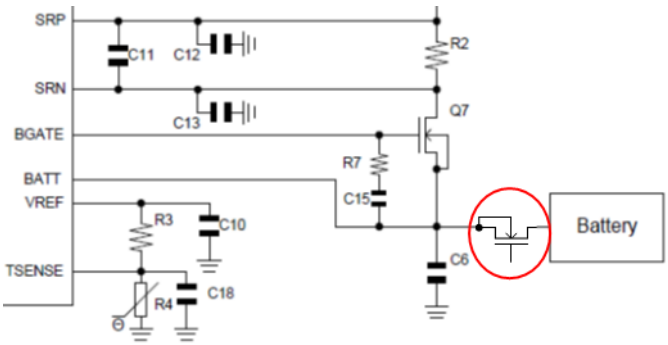


Figure 11-3c. Additional position of FET for countermeasures

Table 11-3. Control and countermeasure scheme of FETs for switches

Operation mode	System output voltage	Additional FET control	Countermeasures for noise
Power supply mode	Value of VFAST_CHG_SET	OFF	DCDC becomes CV control.
FAST-Charge mode (CV)	Value of VFAST_CHG_SET	ON	Due to CV control, the effect of sounding is small. Explained in Fig. 3-3d
FAST-Charge mode (CC)	BATT ＋ICHG x R2	ON	Due to CV control, the effect of sounding is small. Explained in Fig. 3-3e
TRICKLE, PRE Charge mode	Value of VSYSREG_SET	ON	Since the output is constant at 8.96V, the effect of sounding is small.

This section describes the mechanism for reducing noise during CV / CC control. Figure 11-3d shows an explanatory diagram of noise reduction during CV control.

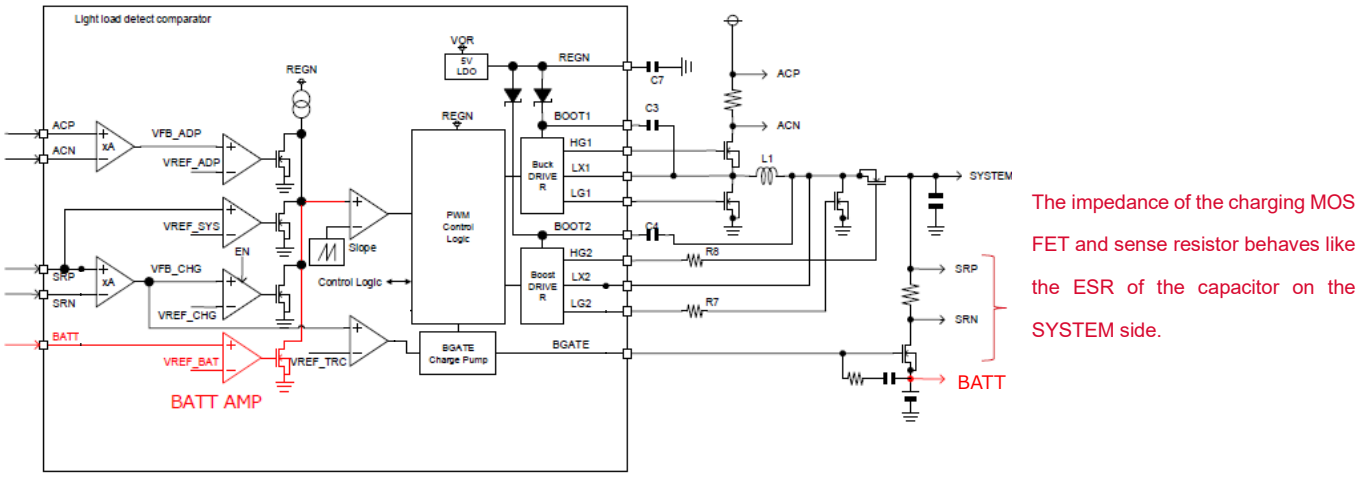


Figure 11-3d. Illustration of noise reduction during CV control

During CV charging, the unit is operated by a BATT AMP loop with the BATT pin as input, which keeps the BATT pin voltage constant. The loop characteristic of BATT AMP is that the MOSFETs for charging and the current sensing resistors are visible as ESR to the output capacitor on the SYSTEM side, and the DCDC bandwidth shifts to a higher range due to the creation of a zero point. This reduces the ripple at light loads.

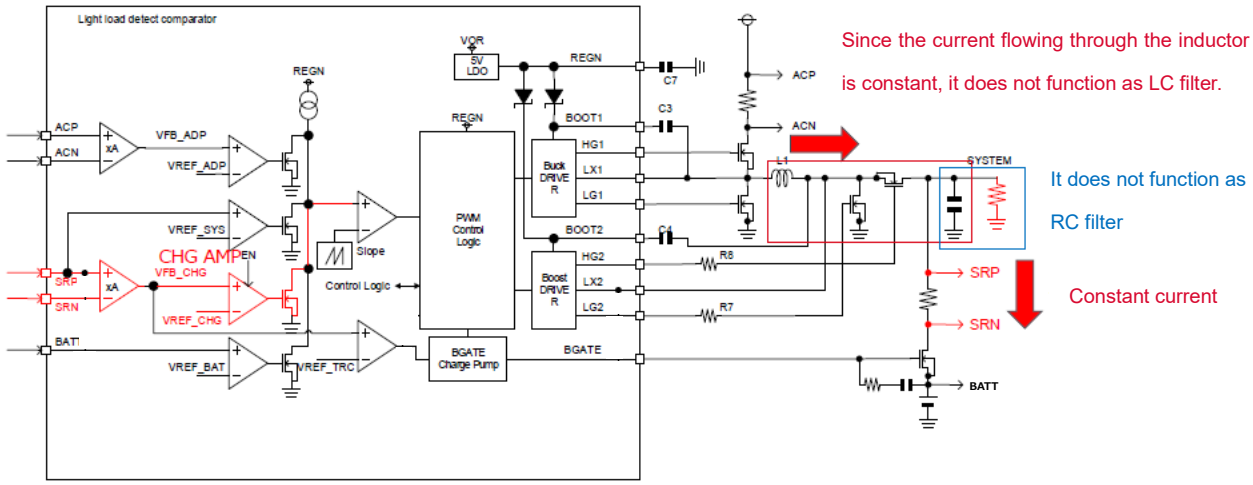


Figure 11-3e. Explanation diagram of sound reduction during CC control

During CC charge current control, the DCDC voltage is controlled so that the voltage between SRP and SRN is constant. Unlike the CV charging voltage control, the control is such that the current flowing through the inductor is constant, and no feedback is applied to the load from the SYSTEM side. Therefore, the inductor, output capacitor, and load resistance filter cannot be seen during current control. As a result, the output capacitor does not reduce the bandwidth, and the response characteristics remain in the high frequency range, eliminating ripples in the audible range.

12 Misleading specifications

12 - 1 Adapter/USB input source is not automatically switched.

As shown in Table 12-1 (added to VIN_CTRL_SET on page 41 of the datasheet), the two power ports of the BD99954 are designed to be able to automatically switch to the port with the higher priority setting by setting the priority. (Determined by the logic of bit7: VIN_ORD in the red box.)

Table 12-1. VBUS/VCC Priority Port Setting Register

8.5.11. VIN_CTRL_SET

VBUS and VCC Control Setting

Command Code: 0Ah
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	OTG_BOTH_EN	"Enabling OTG reverse buck boost output to VBUS and VCC both. "1": Enable / "0": Disable." When OTG_BOTH_EN=1 and VBUS_EN=VCC_EN=1, OTG reverse buck boost output same voltage at VBUS and VCC, VBUS=VCC=VRBOOST_SEL[14:6].
14	VRBOOST_TRIG	Reverse buck Boost operation Trigger. "1": Trigger/ "0": No trigger
13	VRBOOST_EN[1]	Enabling VCC Reverse buck Boost operation. "1": Enable / "0": Disable.
12	VRBOOST_EN[0]	Enabling VBUS Reverse buck Boost operation. "1": Enable / "0": Disable.
11	PP_BOTH_THRU	"Enabling output to VBUS and VCC both. "1": Enable / "0": Disable." When PP_BOTH_THRU=1 and VBUS_EN=VCC_EN=1, VIN_ORD=0 : Power path output same voltage from VCC to VBUS, VIN_ORD=1 : Power path output same voltage from VBUS to VCC.
10	reserved	
9	reserved	
8	reserved	
7	VIN_ORD	VBUS / VCC input priority. "1": VBUS prior / "0": VCC prior.
6	VBUS_EN	Enabling VBUS input. "1": Enable / "0": Disable.
5	VCC_EN	Enabling VCC input. "1": Enable / "0": Disable.
4	VSYS_PRIORITY	Disabling the input current limit for avoiding VSYS drop when VBAT is the dead-battery, VBAT is < VSYSREG_SET. "1": Disable the input current limit / "0": Enable the input current limit.
3	PPC_SUB_CAP[1]	Power source peak current sub-capability
2	PPC_SUB_CAP[0]	
1	PPC_CAP[1]	Power source peak current capability
0	PPC_CAP[0]	

However, when VSYSREG_SET > VBATT voltage, such as Dead Battery, automatic switching is not performed to avoid system shutdown. For example, even if 15V is input to VBUS while VBUS is given priority and VCC=5V is input in a situation where the battery voltage is low (2.5V or less), it will not switch to VBUS. Unplug all the connected inputs, and then connect the desired inputs.

12 - 2 Not compatible with USB1.1 and other 100mA input current standards

Due to the configuration of the step-up/step-down DCDC that drives the four external MOSFETs, the self-consumption current is so large that it cannot supply power to the system or charge the battery at an input current of 100mA, so operation of the USB1.1 standard or the USB1.2 standard SDP 100mA is not guaranteed.

12 - 3 VSYS voltage drop when charging is stopped

In order to prevent the rush current to the battery when charging is stopped, Enable (EN) of the charging current control amplifier is delayed by 3-4ms as shown in the timing chart in Figure 12-1, so VFB_CHG = VREF_CHG = 0 of the amplifier during that time. Due to the offset state of the amplifier, the FB is pulled out, so the DCDC stops and the VSYS voltage drops.

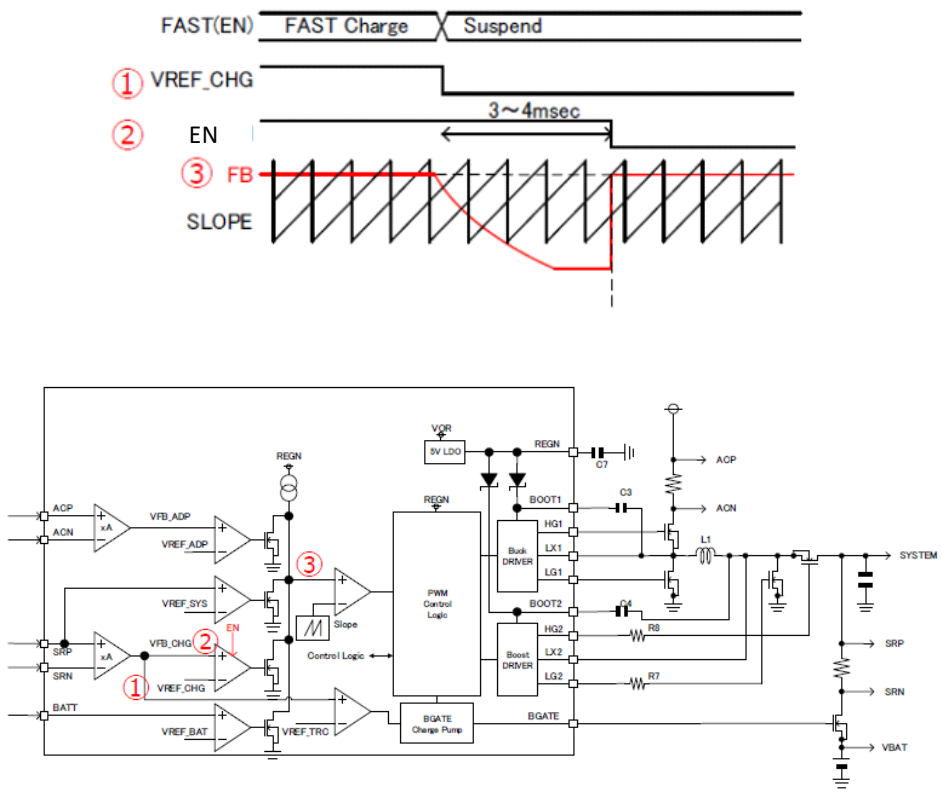


Figure 12-1. VSYS voltage drop mechanism (FAST charge termination timing chart and charge block diagram)

The cause of the VSYS voltage drop is that there is a time lag in the switching of the operating mode of the amplifier that controls the DCDC output during the state transition from FAST charging to suspend charging (temp_error, suspend).

When the transition from FAST charging to charging stop (red arrow) in the state transition table shown in Figure 12-2 occurs, the control of VSYS_AMP is switched from CHG_AMP. On the other hand, when the transition from TRICLE and PRE charging to charge stop (blue arrow), TRI_AMP is only stopped, and the amplifier that controls the output of DCDC is not switched. Therefore, if charging is stopped from the PRE charging state by setting the VSYSREG_SET register, VSYS voltage drop will not occur.

AMP	Use	TRICLE, PRE	Stop charging	FAST
①BATT_AMP	For CV control	Operation	Operation	Operation
②VSYS_AMP	For VSYS control	Operation	Operation	Stop
③CHG_AMP	For FAST charge control	Stop	Stop	Operation
④TRI_AMP	Tricle, Pre for charge control	Operation	Stop	Operation as OCP

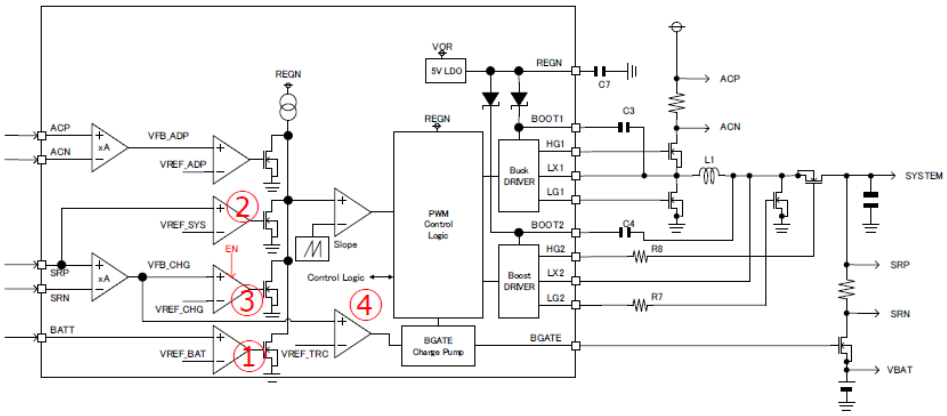


Figure 12-2. VSYS voltage drop avoidance control
(state transition table of charge-related amplifiers and its block diagram)

Finally, the avoidance sequence (control procedure) is described below.

1. Detection of battery disconnection
   This phenomenon becomes a fatal problem such as a system stop only when the battery voltage such as a dead battery is extremely low or when the battery is removed.
   → FAST charge state. BGATE ON,VSYS=BATT=12.40V

2. 0x11: VSYSREG_SET is set to 14.016V.
   → After 28.8ms (max) from completion of setting, transition to PRE charging. BGATE ON, VSYS=BATT=12.40V

3. 0x0C: Set CHG_EN to disenable
   → Transition to SUSPEND. BGATE OFF、VSYS=14.016V, BATT=OPEN

4. 0x11: VSYSREG_SET is set to 8.960V.
   → SUSPEND state. BGATE OFF, VSYS=8.960V, BATT=OPEN

12 - 4 Caution when using BC1.2 with VBUS port

Noise from VBUS_DPI and VBUS_DMI propagates to the IADP/RESET signal inside the IC, causing IADP/RESET to be reset, and there is an input current limit value. When signals are input to VBUS_DPI and VBUS_DMI, set 9bit EXTIADPEN of 0x40 VM_CTRL_SET to 0, and make the ADC measurement of IADP/RESET Disenable.

13 PROCHOT

13 - 1 PMON setting

The power monitoring result in compliance with IMPV8 can be output to the PMON pin.

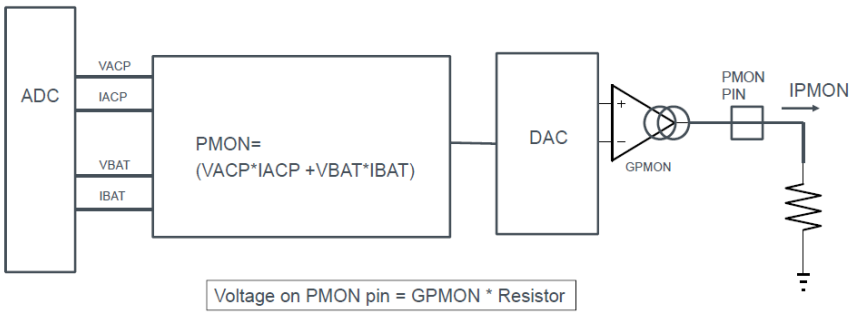


Figure 13-1. PMON pin internal circuit block diagram

Output the power value as current from the PMON pin and measure the voltage of the external resistor.

The conversion between power and current is given below in the datasheet.

Table 13-1. PMON Electrical Characteristics

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
<PMON>						
Power Monitor Amplifier Gain (IPMON)/(VACP×IACP + VBAT×IBAT)	G_{PMON}	-	16	-	µA/W	REG0x25h[2:0]=6h 6.25W Setting
		-	8	-	µA/W	REG0x25h[2:0]=5h 12.5W Setting
		-	4	-	µA/W	REG0x25h[2:0]=4h 25W Setting
		-	2	-	µA/W	REG0x25h[2:0]=3h 50W Setting
		-	1	-	µA/W	REG0x25h[2:0]=2h 100W Setting
		-	0.5	-	µA/W	REG0x25h[2:0]=1h 200W Setting
		-	0.25	-	µA/W	REG0x25h[2:0]=0h 400W Setting
	I_{PMON}	-5	-	+5	%	IPMON=50uA
PMON Maximum Current	$I_{PMONMAX}$	-	-	200	µA	

0x25 Set bit 8 and bits [3:0] of PMON_IOUT_CTRL_SET to set the PMON.

Table 13-2. PMON Setting Register

8.5.38. PMON_IOUT_CTRL_SET

PMON and IOUT Output Control Setting

Command Code: 25h
Bus Protocol: Read/Write Word

Bit	Symbol	Description
15	reserved	
14	reserved	
13	reserved	
12	reserved	
11	reserved	
10	reserved	
9	IMON_INSEL	IOUT Input source select. 0b: Measurement Average Value/ 1b: Measurement Value
8	PMON_INSEL	PMON Input source select. 0b: Measurement Average Value/ 1b: Measurement Value
7	IOUT_OUT_EN	IOUT enable. "1": Enable / "0": Disable.
6	IOUT_SOURCE_SEL	IOUT source select. "1": Input Current / "0": Battery Dis-charge Current.
5	IOUT_GAIN_SET[1]	IOUT gain select. 00b: 5V/V / 01b: 10V/V / 10b: 20V/V/ 11b: 40V/V
4	IOUT_GAIN_SET[0]	
3	PMON_OUT_EN	PMON Enable. "1": Enable / "0": Disable.
2	PMON_GAIN_SET[2]	PMON gain select. 0h: x1/ 1h: x2/ 2h: x4/ 3h: x8/ 4h: x16/ 5h: x32/ 6h: x64
1	PMON_GAIN_SET[1]	
0	PMON_GAIN_SET[0]	

13 - 2 Peak Power Control

Peak Power Control can be set in accordance with IMPV8. When using Peak Power Control, peak input current control can be set by VIN_CTRL_SET.PPC_CAP [1:0] and PPC_SUB_CAP [1:0].

Table 13-3. Peak Power Control Setting Register

● **VIN_CTRL_SET**

VBUS and VCC Control Setting

Command Code: 0Ah
Bus Protocol: Read/Write Word

Bit	Symbol	Description
3	PPC_SUB_CAP[1]	Power source peak current sub-capability
2	PPC_SUB_CAP[0]	
1	PPC_CAP[1]	Power source peak current capability
0	PPC_CAP[0]	

PPC_CAP	PPC_SUB_CAP	Overload Capabilities Description
00b	*b	Peak current equals (IBUS_LIM_SET or ICC_LIM_SET) .
01b	00b	Peak current equals 150.0% (IBUS_LIM_SET or ICC_LIM_SET) for 1ms. Low current equals 97.0% (IBUS_LIM_SET or ICC_LIM_SET) for 19ms.
	01b	Peak current equals 125.0% (IBUS_LIM_SET or ICC_LIM_SET) for 2ms. Low current equals 97.0% (IBUS_LIM_SET or ICC_LIM_SET) for 18ms.
	10b	Peak current equals 110.0% (IBUS_LIM_SET or ICC_LIM_SET) for 10ms. Low current equals 90.0% (IBUS_LIM_SET or ICC_LIM_SET) for 10ms.
10b	00b	Peak current equals 200.0% (IBUS_LIM_SET or ICC_LIM_SET) for 1ms. Low current equals 95.0% (IBUS_LIM_SET or ICC_LIM_SET) for 19ms.
	01b	Peak current equals 150.0% (IBUS_LIM_SET or ICC_LIM_SET) for 2ms. Low current equals 94.0% (IBUS_LIM_SET or ICC_LIM_SET) for 18ms.
	10b	Peak current equals 125.0% (IBUS_LIM_SET or ICC_LIM_SET) for 10ms. Low current equals 75.0% (IBUS_LIM_SET or ICC_LIM_SET) for 10ms.
11b	00b	Peak current equals 200.0% (IBUS_LIM_SET or ICC_LIM_SET) for 1ms. Low current equals 95.0% (IBUS_LIM_SET or ICC_LIM_SET) for 19ms.
	01b	Peak current equals 175.0% (IBUS_LIM_SET or ICC_LIM_SET) for 2ms. Low current equals 92.0% (IBUS_LIM_SET or ICC_LIM_SET) for 18ms.
	10b	Peak current equals 150.0% (IBUS_LIM_SET or ICC_LIM_SET) for 10ms. Low current equals 50.0% (IBUS_LIM_SET or ICC_LIM_SET) for 10ms.

For the input current limit value CUR_ILIM_VAL set by IADP/RESET, IBUS_LIM_SET, IVCC_LIM_SET, or BC1.2, several patterns with different ratios of time and input current limit settings can be set as shown below.

Figure 13-2. Input current limit when Peak Power Control is set

When the input current limit is set at 3000mA, Peak Power Control of 125%/10ms and 75%/10ms is set as shown below.

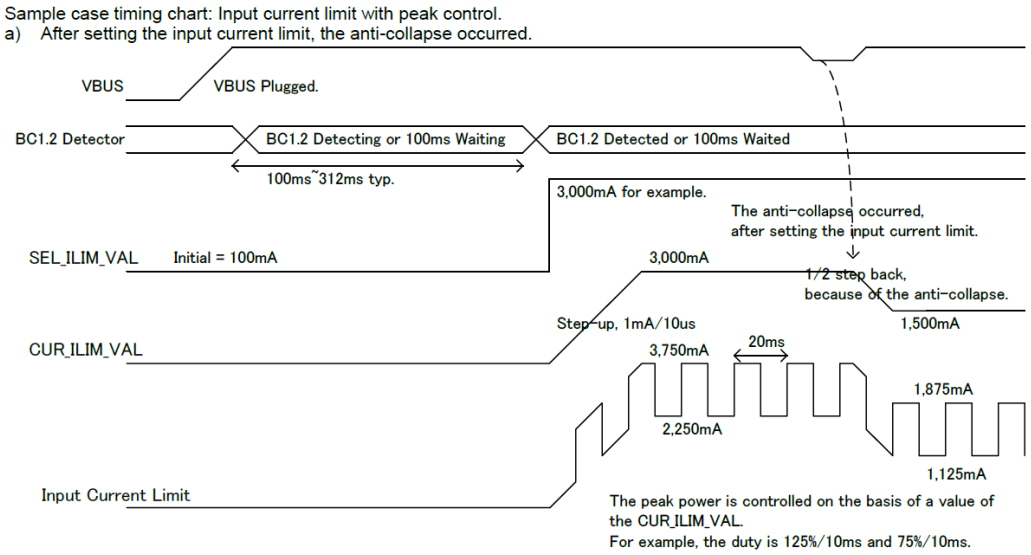


Figure 13-3. Input current limit when Peak Power Control is set

14 Flowchart of the process from battery and input connection to charge completion

The flowchart below shows how to connect inputs, set input current limit, set charging, and detect protection operation. The flow chart shows the process up to the completion of charging. Clicking on the underlined blue text in the flowchart will take you to the link. The waiting time shown in the flowchart is an example. They need to be set according to the application.

14 - 1 Flowchart of the process from battery and input connection to charge completion

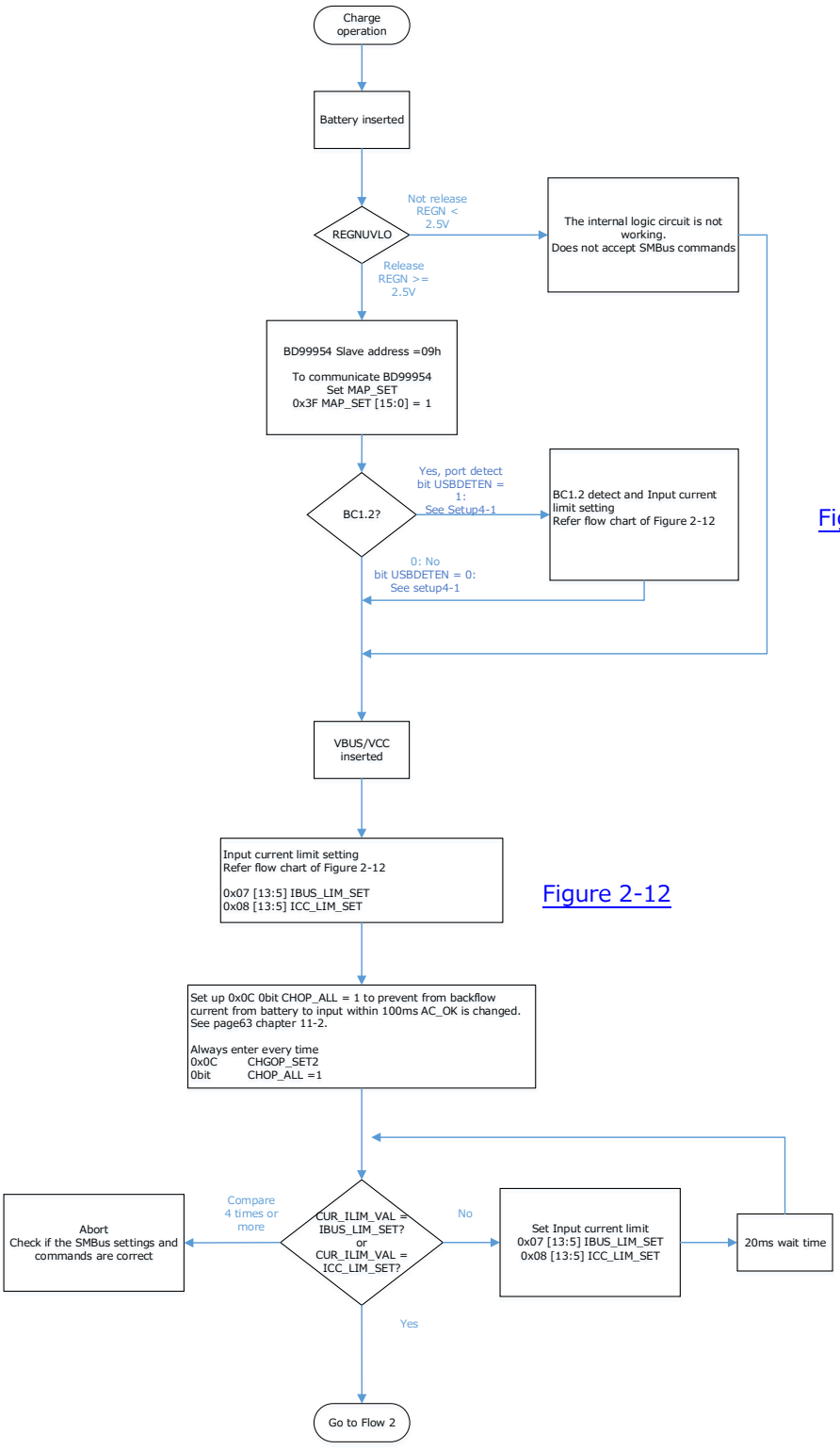


Figure 2-12

Figure 2-12

Figure 14-1. Flowchart for input connection

14 - 2 Flowchart of battery and input connection to complete charging Continued 2

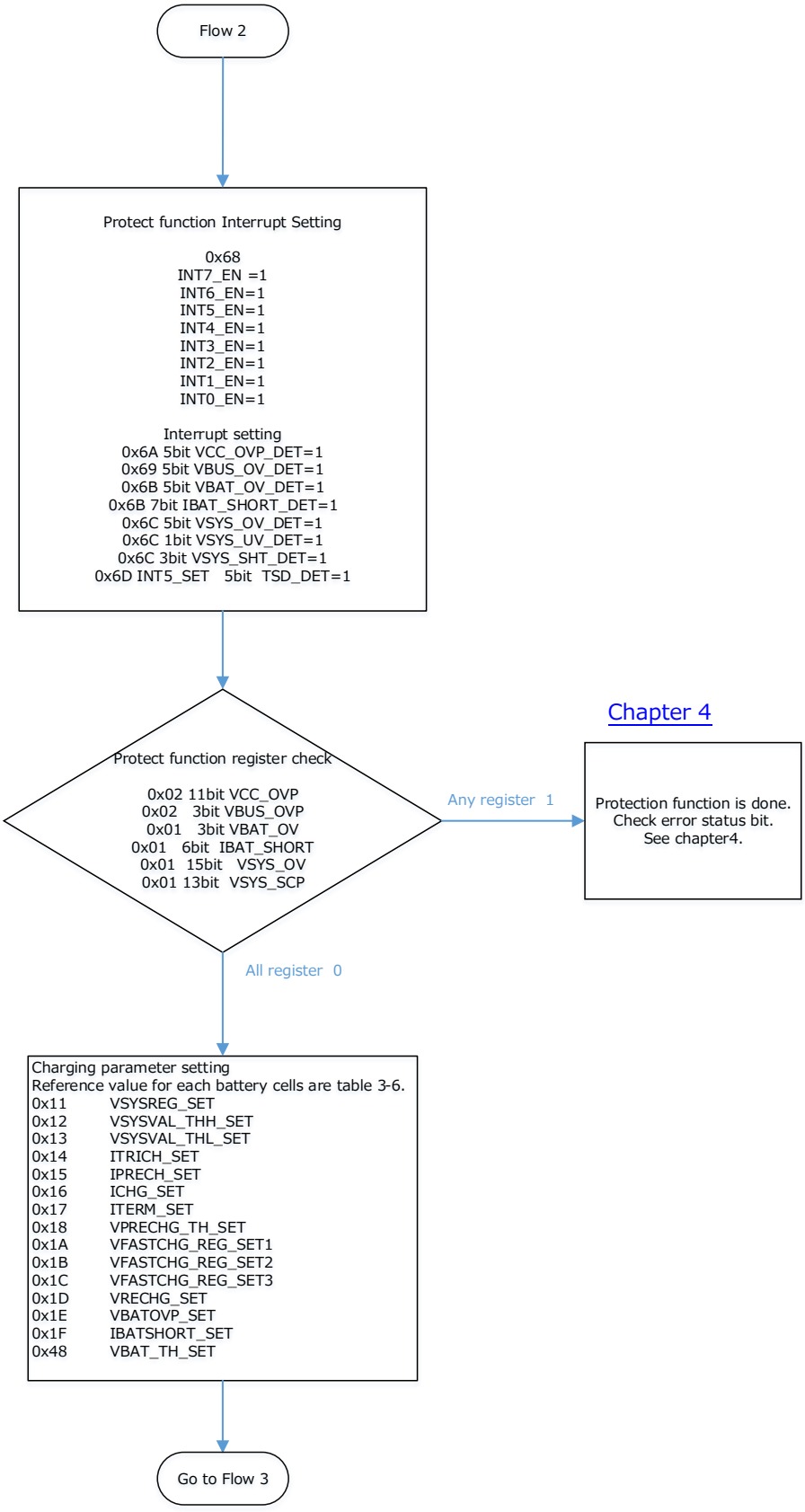


Figure 14-2. Flowchart for setting charging conditions

14 - 3 Flowchart of battery and input connection to complete charging Continued 3

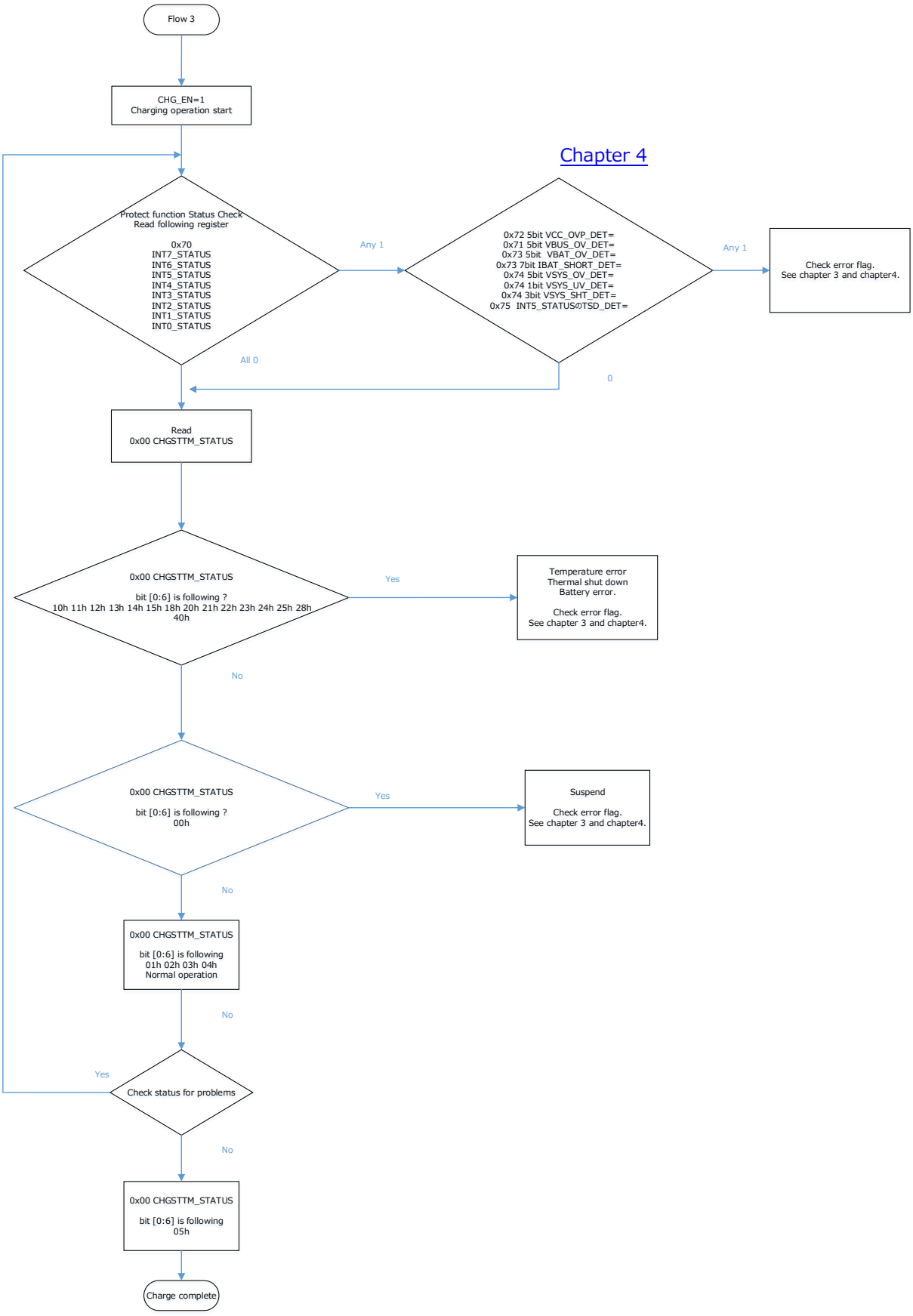


Figure 14-3. Flowchart of charging from start to completion

Revision History

Date	Revision	Changes
27. Dec. 2021	001	Initial Release

Notes

1) The information contained herein is subject to change without notice.

2) Before you use our Products, please contact our sales representative and verify the latest specifications :

3) Although ROHM is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors.
Therefore, in order to prevent personal injury or fire arising from failure, please take safety measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. ROHM shall have no responsibility for any damages arising out of the use of our Poducts beyond the rating specified by ROHM.

4) Examples of application circuits, circuit constants and any other information contained herein are provided only to illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

5) The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM or any other parties. ROHM shall have no responsibility whatsoever for any dispute arising out of the use of such technical information.

6) The Products specified in this document are not designed to be radiation tolerant.

7) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a ROHM representative : transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.

8) Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters.

9) ROHM shall have no responsibility for any damages or injury arising from non-compliance with the recommended usage conditions and specifications contained herein.

10) ROHM has used reasonable care to ensure the accuracy of the information contained in this document. However, ROHM does not warrants that such information is error-free, and ROHM shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.

11) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. For more details, including RoHS compatibility, please contact a ROHM sales office. ROHM shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

12) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.

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ROHM SEMICONDUCTOR

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