

SPICE Modeling Report

Isolation voltage 3750Vrms 1ch Gate Driver Providing Galvanic Isolation BM61S41RFV-C

General Description

This is a report of the BM61S41RFV-C SPICE Model.

The correlation between actual measurement and simulation result were summarized.

Simulation Environment

- Circuit Simulator : PSpice / Cadence Design System, Inc.
- Version Information : 17.2-2016
- OS Information : Windows 10 64-bit Edition

File Information

- Library File Name : BM61S41RFV.lib
- Symbol File Name : BM61S41RFV.olb
- Subcircuit and Symbol

Table 1. Correspondence Table

Product Name	Subcircuit	Symbol
BM61S41RFV-C	BM61S41RFV (Rev:1.00)	BM61S41RFV

Caution

- These model characteristics are specifically at Ta=25°C. Thus, the simulation result with temperature variances may significantly differ from the result with the one done at actual application board (actual measurement).
- The simulation result and characteristics described in this report may differ depending on the board design. It is recommended to perform the measurement on the actual board to verify the result.
- The values from the simulation results are not guaranteed. Please use these results as a guide for your design.
- Actual measurement was done using a specific sample, thus the measured data is just as a reference.

BM61S41RFV-C SPICE MODEL

■ Terminal Information

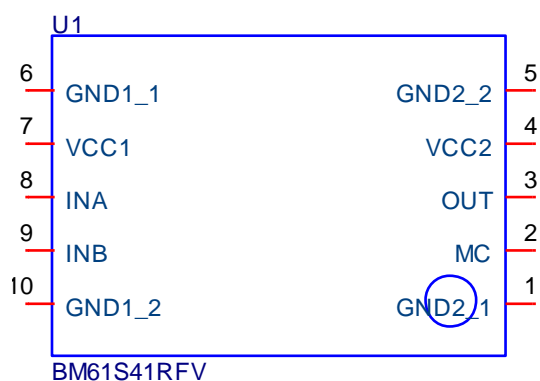


Figure 1. Symbol of BM61S41RFV

Table 2. Pin Table

Terminal No.	Terminal Name
1	GND2_1
2	MC
3	OUT
4	VCC2
5	GND2_2
6	GND1_1
7	VCC1
8	INA
9	INB
10	GND1_2

Verifiable Characteristics

- Electrical Characteristics (vs. Datasheet)..... 3-4
- Characteristics in SPICE (vs. Measured Waveform)
 - ✓ Input-side Circuit Current 1 vs Input-side Supply Voltage..... 5
 - ✓ Input-side Circuit Current 2 vs Input-side Supply Voltage..... 6
 - ✓ Output-side Circuit Current 1 vs Output-side Supply Voltage..... 7
 - ✓ Output-side Circuit Current 2 vs Output-side Supply Voltage..... 8
 - ✓ Logic High/Low Level Input Voltage vs Input-side Supply Voltage..... 9
 - ✓ Output Voltage vs Logic Level Input Voltage (INA)..... 10

Electrical Characteristics (vs. Datasheet)

Table 3. Electrical Characteristics Comparison

Unless otherwise specified, Ta=25°C, V_{CC1}=5V, V_{CC2}=18V

Parameter	Modeled <i>(Note 1)</i>	Value		Unit	Error	Condition
		Datasheet (Typ.)	SPICE			
General						
Input-side Circuit Current 1	Yes	0.4	0.40	mA	0.0%	INA=L, INB=H
Input-side Circuit Current 2	Yes	2.0	2.00	mA	0.0%	INA=100kHz, Duty=50%
Output-side Circuit Current 1	Yes	0.70	0.700	mA	0.0%	OUT=L
Output-side Circuit Current 2	Yes	0.52	0.520	mA	0.0%	OUT=H
Logic Block						
Logic High Level Input Voltage	Yes	-	1.53	V	-	INA, INB
Logic Low Level Input Voltage	Yes	-	1.33	V	-	INA, INB
Logic Pull-down Resistance	Yes	50	50.0	kΩ	0.0%	INA
Logic Pull-up Resistance	Yes	50	50.0	kΩ	0.0%	INB
Output						
OUT ON Resistance (Source)	Yes	0.67	0.671	Ω	0.1%	I _{OUT} =-40mA
OUT ON Resistance (Sink)	Yes	0.45	0.451	Ω	0.2%	I _{OUT} =40mA
Turn ON Time	Yes	55	55.0	ns	0.0%	INA=PWM, INB=L
	Yes	55	54.4	ns	1.1%	INA=H, INB=PWM
Turn OFF Time	Yes	55	56.9	ns	3.5%	INA=PWM, INB=L
	Yes	55	54.9	ns	0.2%	INA=H, INB=PWM
Propagation Distortion	Yes	0	1.9	ns	-	t _{POFFA} -t _{PONA}
	Yes	0	0.5	ns	-	t _{POFFB} -t _{PONB}
Rise Time	No	15	16.8	ns	12.0%	2nF between OUT-GND2
Fall Time	No	15	13.7	ns	8.7%	2nF between OUT-GND2
MC ON Resistance	Yes	0.45	0.452	Ω	0.4%	I _{MC} =40mA
MC ON Threshold Voltage	Yes	2	2.0	V	0.0%	

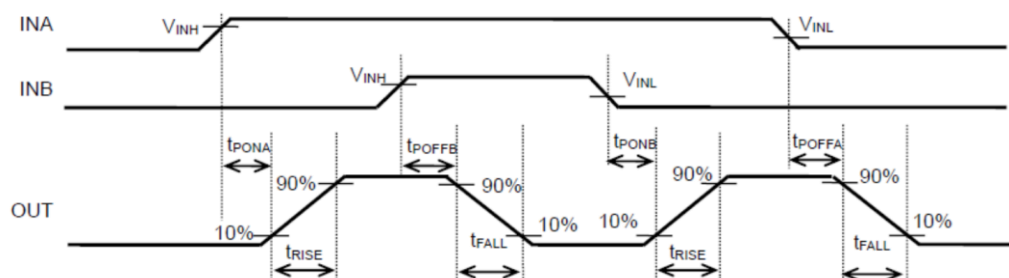


Figure 2. Timing Chart of IN-OUT (Note 2)

(Note 1) Yes : There is a good correlation between measurement result and simulation result.

No : No correlation between measurement result and simulation result.

(Note 2) t_{PONA} : Turn ON Time, t_{PONB} : Turn ON Time, t_{POFFA} : Turn OFF Time, t_{POFFB} : Turn OFF Time, t_{RISE} : Rise Time, t_{FALL} : Fall Time, V_{INH} : Logic High Level Input Voltage, V_{INL} : Logic Low Level Input Voltage.

Parameter	Modeled <i>(Note 1)</i>	Value		Unit	Error	Condition
		Datasheet (Typ.)	SPICE			
Protection Function						
V _{CC1} UVLO OFF Voltage	Yes	4.2	4.20	V	0.0%	
V _{CC1} UVLO ON Voltage	Yes	4.0	4.00	V	0.0%	
V _{CC1} UVLO Mask Time	Yes	1.5	1.63	μs	8.7%	
V _{CC2} UVLO OFF Voltage	Yes	15.0	15.00	V	0.0%	
V _{CC2} UVLO ON Voltage	Yes	14.5	14.50	V	0.0%	
V _{CC2} UVLO Mask Time	Yes	2.9	3.10	μs	6.9%	

(Note 1) Yes : There is a good correlation between measurement result and simulation result.

No : No correlation between measurement result and simulation result.

Characteristics in SPICE (vs. Measured Waveform)

1. Input-side Circuit Current 1 vs Input-side Supply Voltage

Simulation Setting

Type : DC

Voltage Source : VCC1

(4.5V to 5.5V, 100mV step)

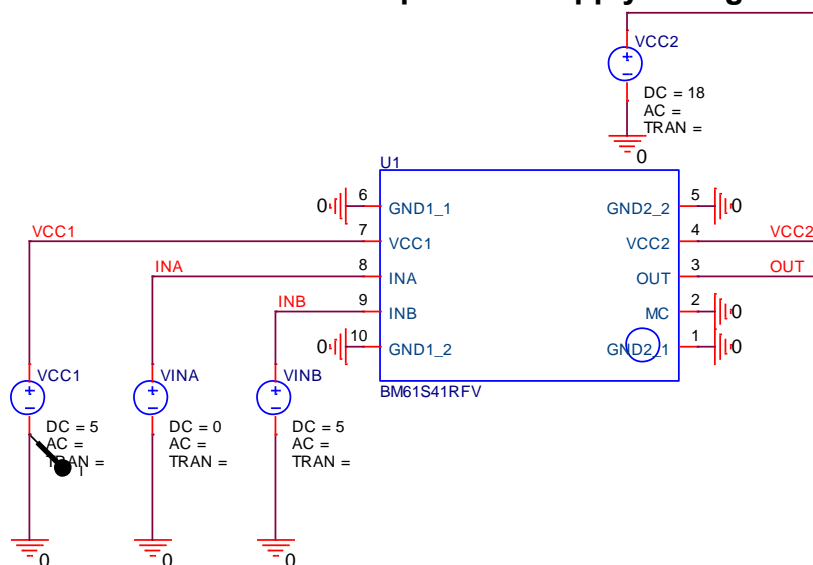
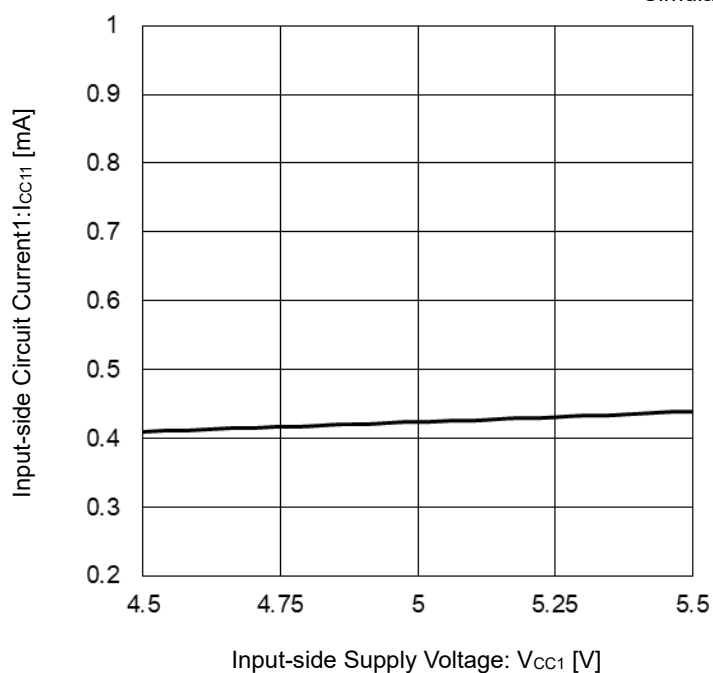
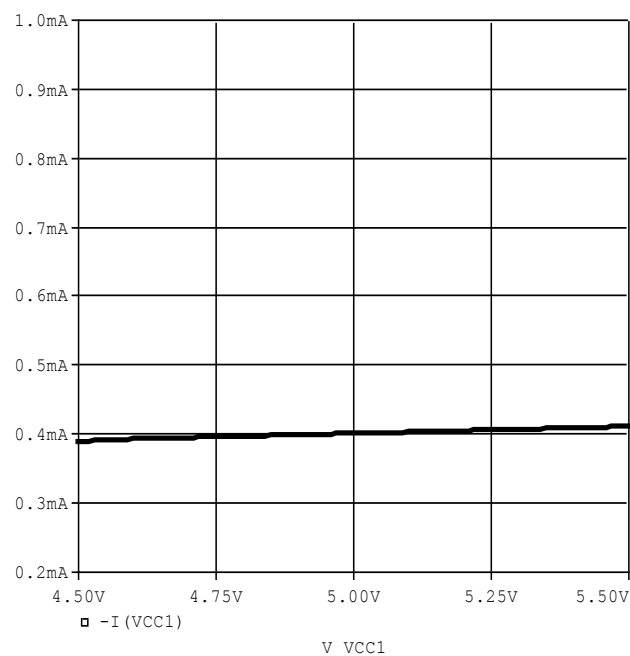
Figure 3.
Simulation Schematic 1Figure 4.
Input-side Circuit Current 1 vs Input-side Supply Voltage
(Measured Waveform)Figure 5.
Input-side Circuit Current 1 vs Input-side Supply Voltage
(SPICE Simulation)

Table 4. Comparison of Characteristics

Unless otherwise specified, Ta=25°C, V_{CC1}=5V, V_{CC2}=18V

Parameter	Measured Result	SPICE Simulation Result	Unit	Error	Condition
Input-side Circuit Current 1	0.42	0.40	mA	-4.8%	INA=L, INB=H

2. Input-side Circuit Current 2 vs Input-side Supply Voltage

Simulation Setting

Type : DC
Voltage Source : VCC1
(4.5V to 5.5V, 100mV step)

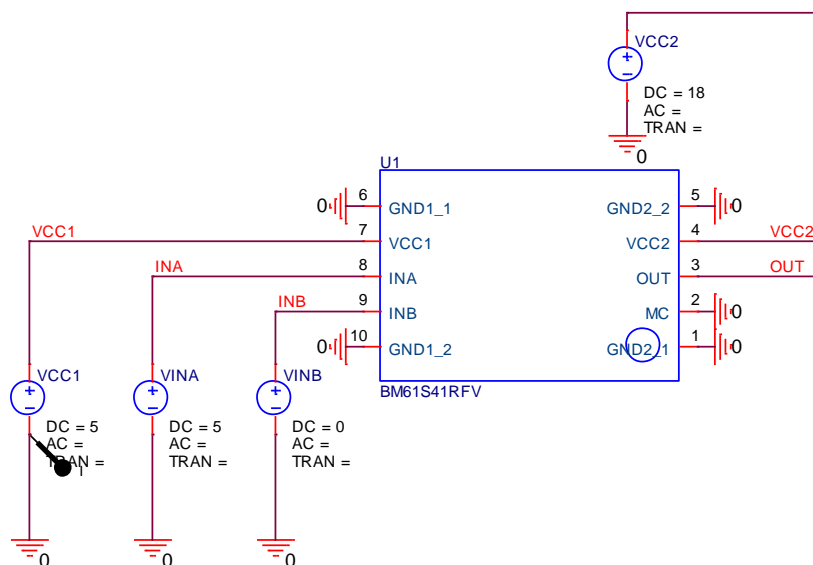


Figure 6.
Simulation Schematic 2

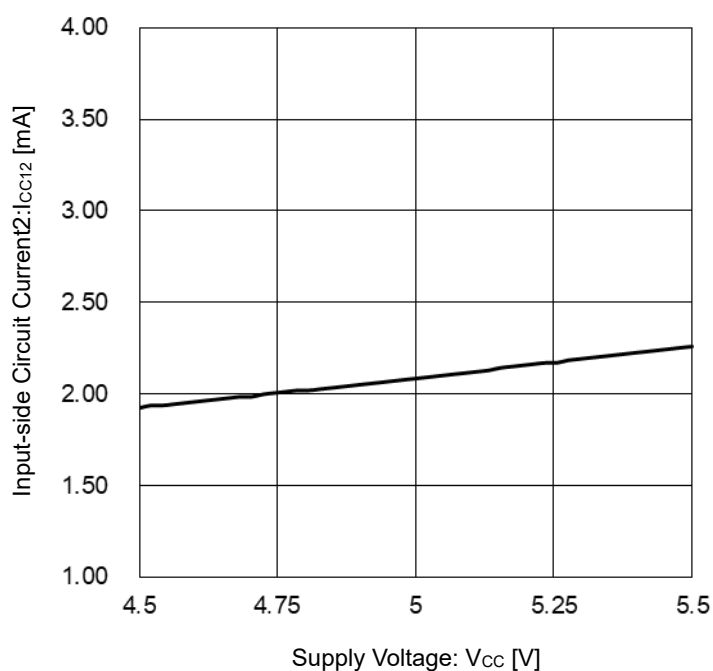


Figure 7.
Input-side Circuit Current 2 vs Input-side Supply Voltage
(Measured Waveform)

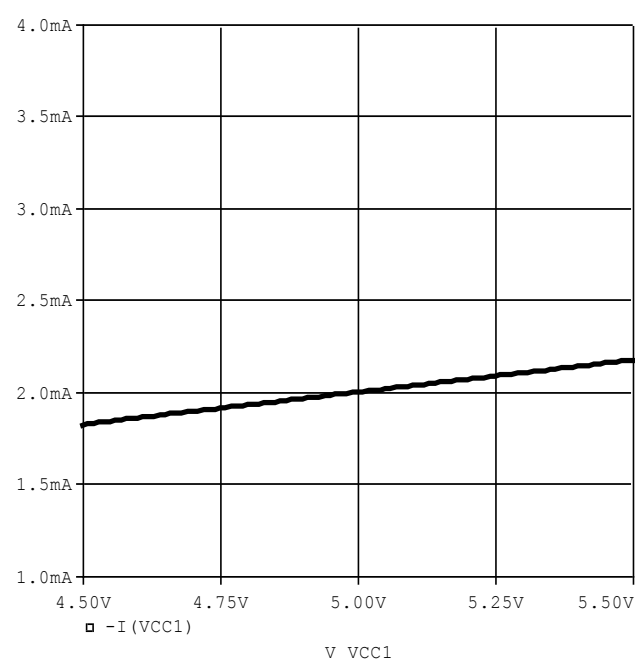


Figure 8.
Input-side Circuit Current 2 vs Input-side Supply Voltage
(SPICE Simulation)

Table 5. Comparison of Characteristics

Unless otherwise specified, Ta=25°C, VCC1=5V, VCC2=18V

Parameter	Measured Result	SPICE Simulation Result	Unit	Error	Condition
Input-side Circuit Current 2	2.09	2.00	mA	-4.3%	INA=H, INB=L

3. Output-side Circuit Current 1 vs Output-side Supply Voltage

Simulation Setting

Type : DC
Voltage Source : VCC2
(16V to 24V, 100mV step)

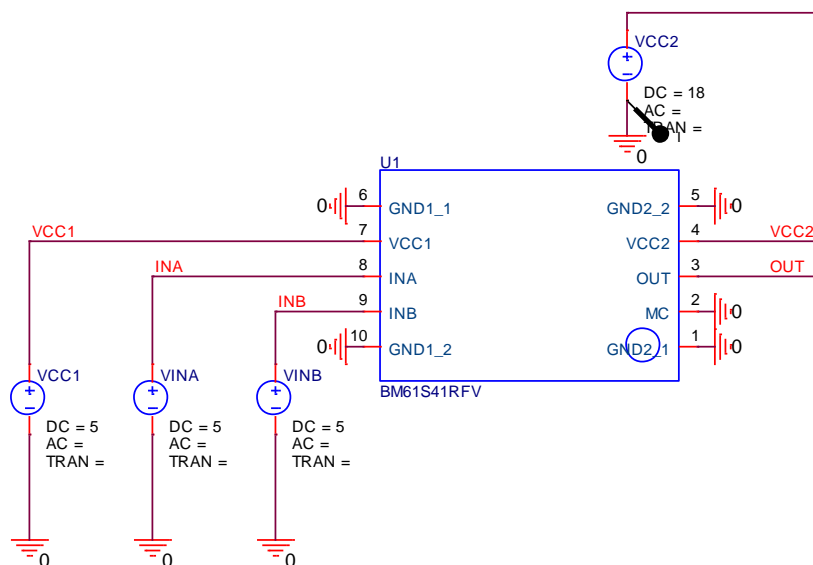


Figure 9.
Simulation Schematic 3

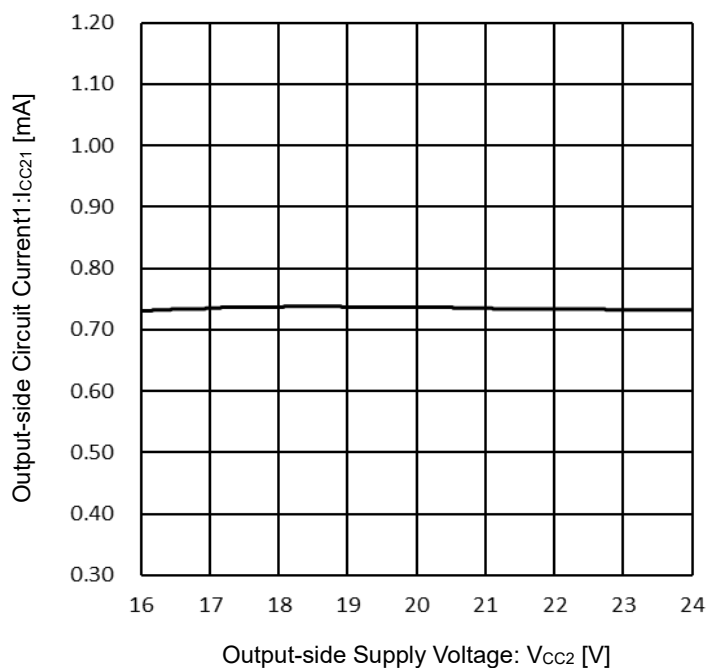


Figure 10.
Output-side Circuit Current 1 vs Output-side Supply Voltage
(Measured Waveform)

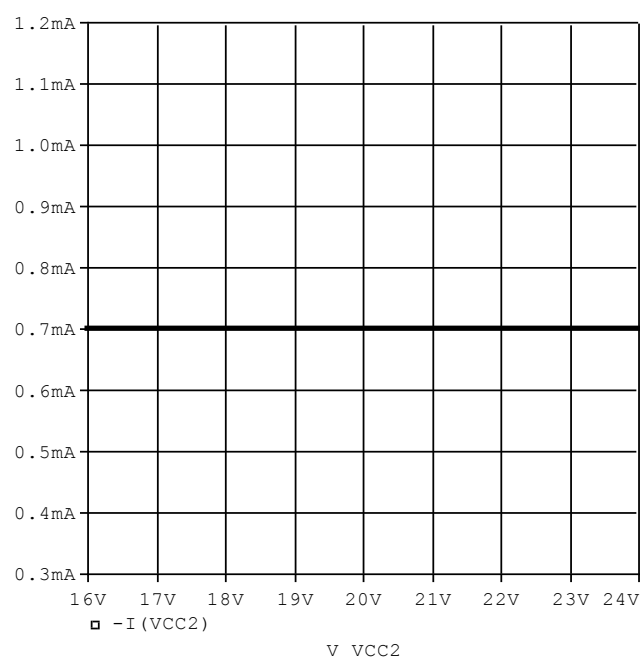


Figure 11.
Output-side Circuit Current 1 vs Output-side Supply Voltage
(SPICE Simulation)

Table 6. Comparison of Characteristics

Unless otherwise specified, Ta=25°C, VCC1=5V, VCC2=18V

Parameter	Measured Result	SPICE Simulation Result	Unit	Error	Condition
Output-side Circuit Current 1	0.73	0.70	mA	-4.1%	OUT=L

4. Output-side Circuit Current 2 vs Output-side Supply Voltage

Simulation Setting

Type : DC
 Voltage Source : VCC2
 (16V to 24V, 100mV step)

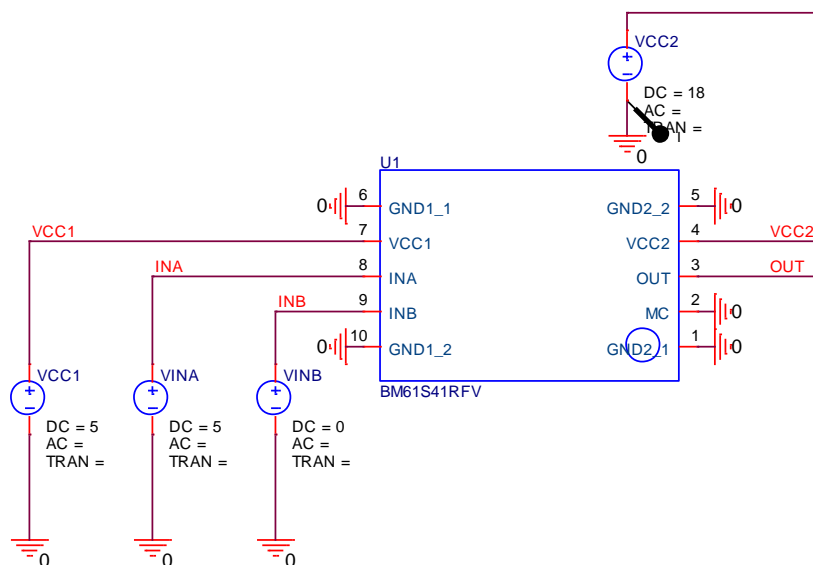


Figure 12.
Simulation Schematic 4

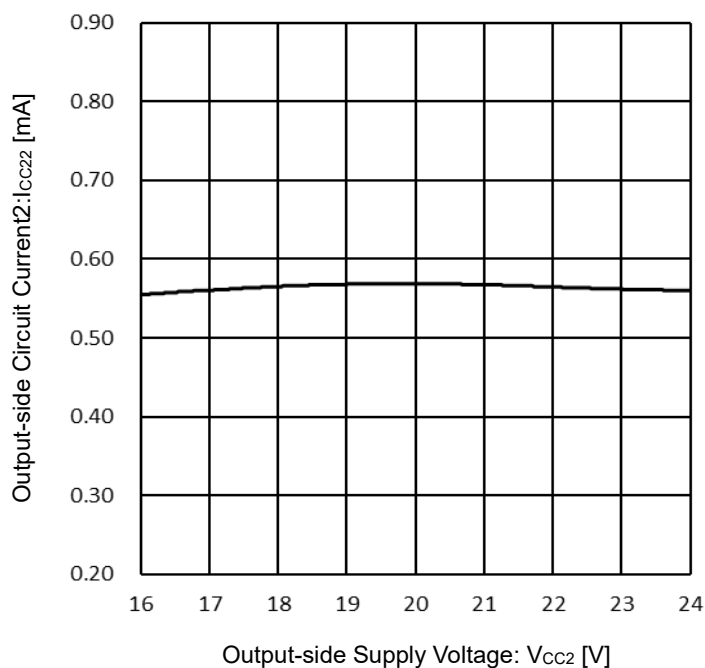


Figure 13.
Output-side Circuit Current 2 vs Output-side Supply Voltage
(Measured Waveform)

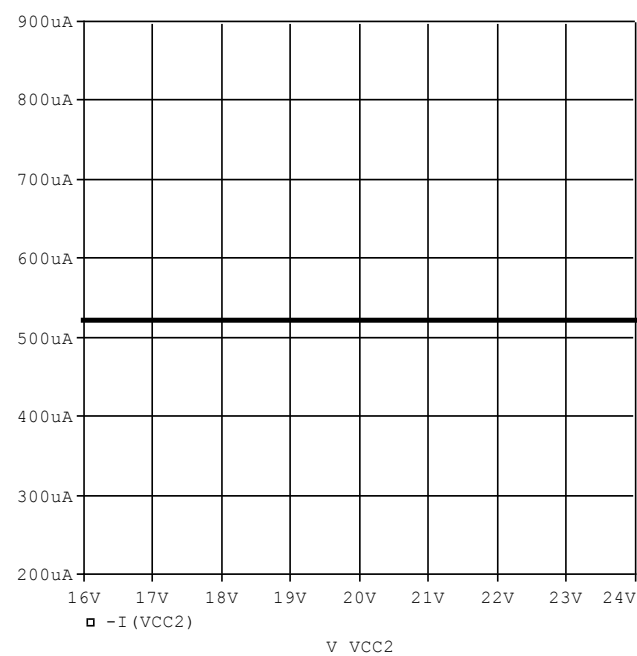


Figure 14.
Output-side Circuit Current 2 vs Output-side Supply Voltage
(SPICE Simulation)

Table 7. Comparison of Characteristics

Unless otherwise specified, Ta=25°C, VCC1=5V, VCC2=18V

Parameter	Measured Result	SPICE Simulation Result	Unit	Error	Condition
Output-side Circuit Current 2	0.56	0.52	mA	-7.1%	OUT=H

5. Logic H/L Level Input Voltage vs Input-side Supply Voltage

Simulation Setting

Type : Transient

Run Time : 2sec

(Maximum Step Size :100μsec)

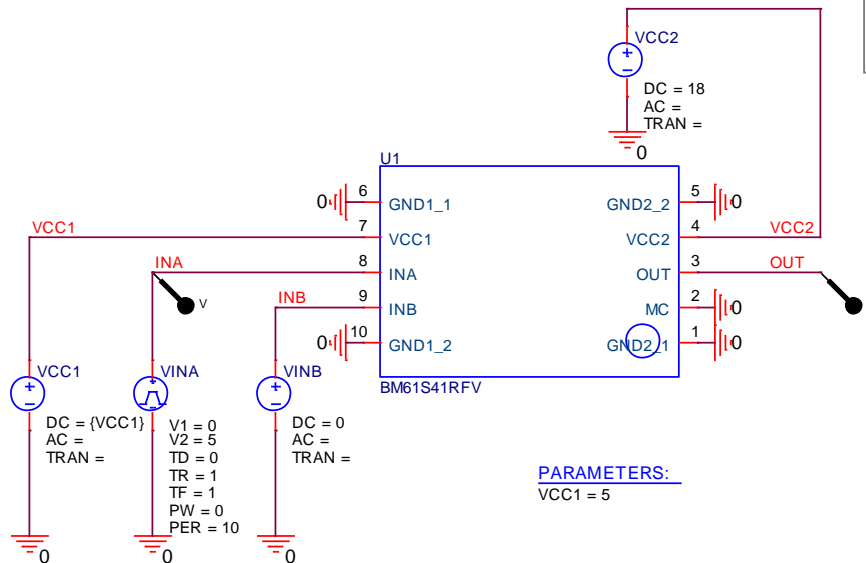


Figure 15.
Simulation Schematic 5

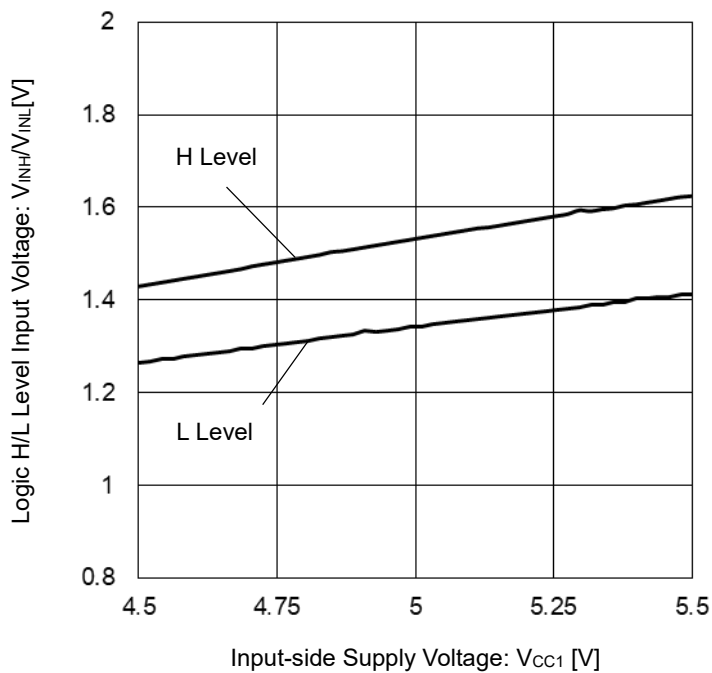


Figure 16.
Logic H/L Level Input Voltage vs Input-side Supply Voltage
(Measured Waveform)

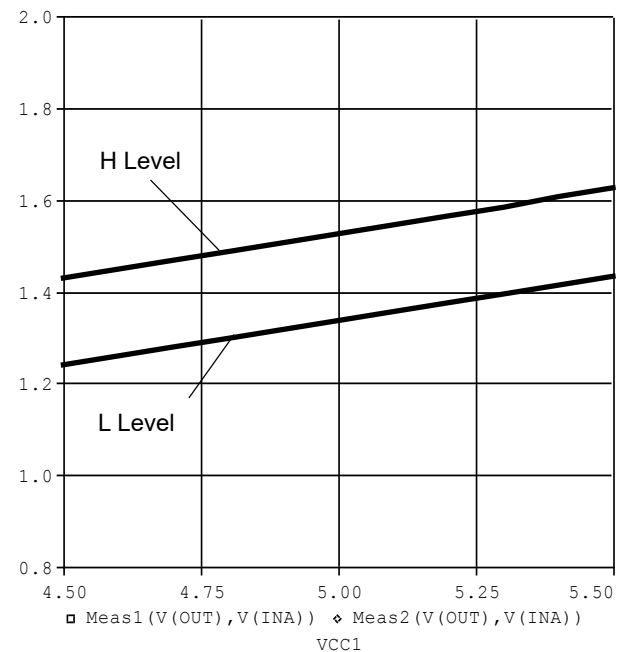


Figure 17.
Logic H/L Level Input Voltage vs Input-side Supply Voltage
(SPICE Simulation)^(Note 1)

Table 8. Comparison of Characteristics

Unless otherwise specified, Ta=25°C, VCC1=5V, VCC2=18V

Parameter	Measured Result	SPICE Simulation Result	Unit	Error	Condition
High Level Threshold	1.53	1.53	V	0.0%	Sweep up
Low Level Threshold	1.34	1.34	V	0.0%	Sweep down

(Note 1) Convert the horizontal axis of simulation result into V(VCC1)

6. Output Voltage vs. Logic Level Input Voltage (INA)

Simulation Setting
 Type : Transient
 Run Time : 2sec
 (Maximum Step Size :100μsec)

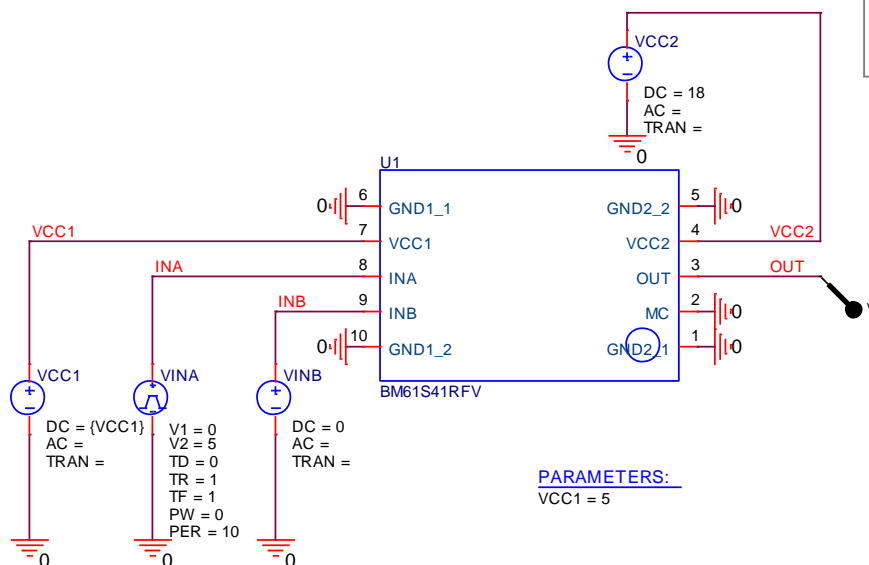


Figure 18.
Simulation Schematic 6

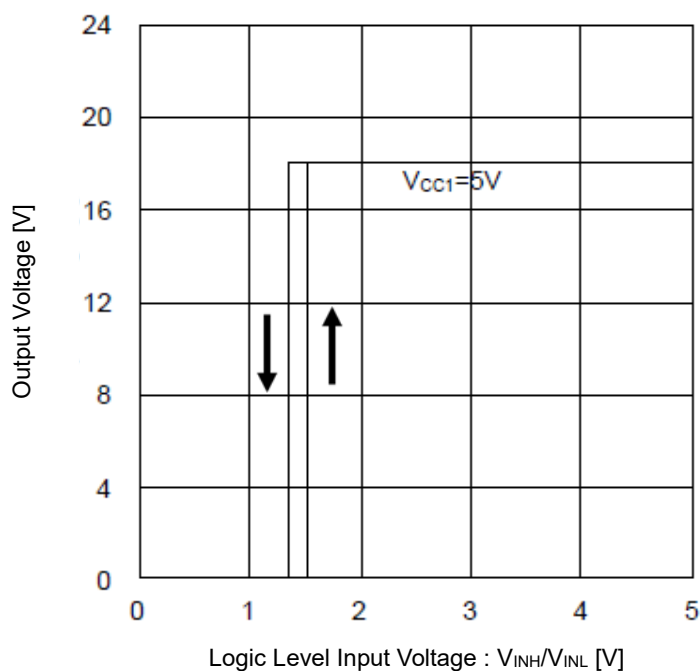


Figure 19.
Output Voltage vs. Logic Level Input Voltage (INA)
(Measured Waveform)

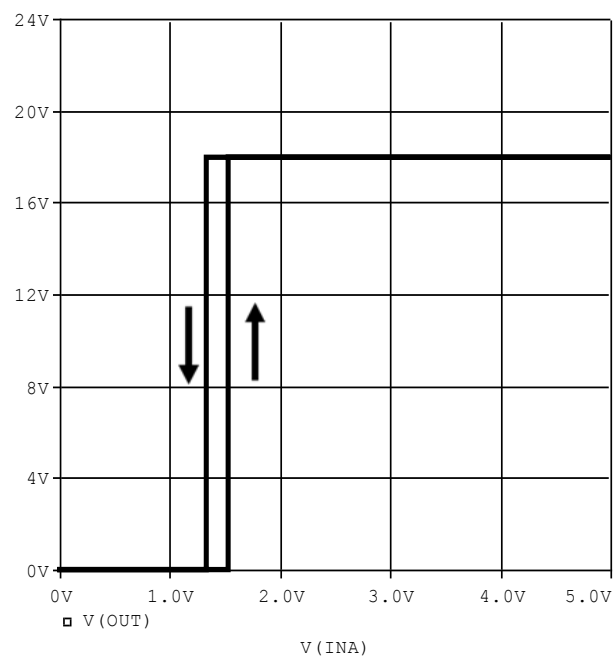


Figure 20.
Output Voltage vs. Logic Level Input Voltage (INA)
(SPICE Simulation) ^(Note 1)

Table 9. Comparison of Characteristics

Unless otherwise specified, $T_a=25^{\circ}\text{C}$, $V_{CC1}=5\text{V}$, $V_{CC2}=18\text{V}$

Parameter	Measured Result	SPICE Simulation Result	Unit	Error	Condition
High Level Threshold	1.53	1.53	V	0.0%	Sweep up
Low Level Threshold	1.34	1.34	V	0.0%	Sweep down

(Note 1) Convert the horizontal axis of simulation result into $V(V_{CC1})$

Revision History

Date	Revision	Changes
Nov.2019	001	New Release

Notes

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