Thermal Design

How to Use the Two-Resistor Model

The two-resistor model is one of the simplest thermal simulation models. The thermal simulations mentioned here cover three-dimensional model thermal conduction and thermal fluid analysis tools. By using the two-resistor model, it is possible to obtain the results of thermal simulation of circuits created on a board in a relatively short period of time. This application note explains how to use the two-resistor model.

Overview of the two-resistor model

The two-resistor model is one of the simplest thermal models for semiconductor devices where the arrangement can be represented as shown in Figure 1. To actually represent the two-resistor model in simulation software, two cuboids of the same shape are stacked together as shown in Figure 2. Since the two-resistor model has a simple structure in which the package is simply divided vertically at the junction, it is suitable for single function devices, such as discrete products. This model is also suitable for connection to multilayer boards or boards with high heat dissipation performance since it is based on a four-layer board in accordance with JEDEC. On the other hand, the two-resistor thermal model produces globally uniform temperature results in thermal simulation and is therefore unsuitable for use in operation modes or chip layouts with localized heat generation, or for connection to boards with low heat dissipation performance, since the simulation precision may be reduced. Because of its simplicity, the two-resistor model is less accurate than the detailed model, which is the most complex thermal model, but has a feature that it can significantly reduce the time required for analysis.
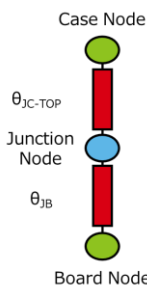

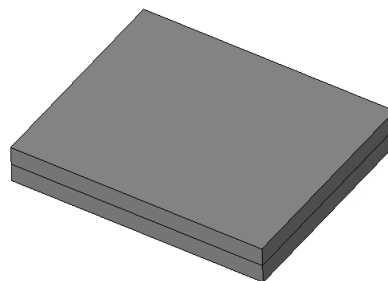Figure 1. Physical arrangement of the two-resistor model

Figure 2. Example of the two-resistor model

LDO regulator BD950M5EFJ-C

(Package name: HTSOP-J8)

In Figure 1, Junction Node is the heat source of the chip, where all the heat is generated while the device is operated. Case Node is the package surface that is in direct thermal contact with the environment immediately above it (normally, air or a thermal conducting material used together with the heat sink). The Board Node represents the board surface temperature at a position of 1 mm or less from the contact point between the edge of the device and the board, and is in direct thermal contact with the environment immediately below the footprint of the package (normally, the printed circuit board). The Case Node and the Board Node are connected to the Junction Node via two thermal resistors ($\theta_{JC\text{-}TOP}$ and θ_{JB}), respectively, which correspond to the two cuboids in Figure 2. In the two-resistor model, it is assumed that the heat generated in the Junction Node flows only in two directions, i.e., toward the Case Node and toward the Board Node, and the thermal flow from the side surfaces of the package to the surrounding fluid is not considered.

For more information on the two-resistor model, refer to Application Note "Two-Resistor Model for Thermal Simulation."

How to obtain the two-resistor model

Step 1

- Access the [ROHM website](#). Enter the product model name in the "Search ROHM" box on the upper right of the home page.
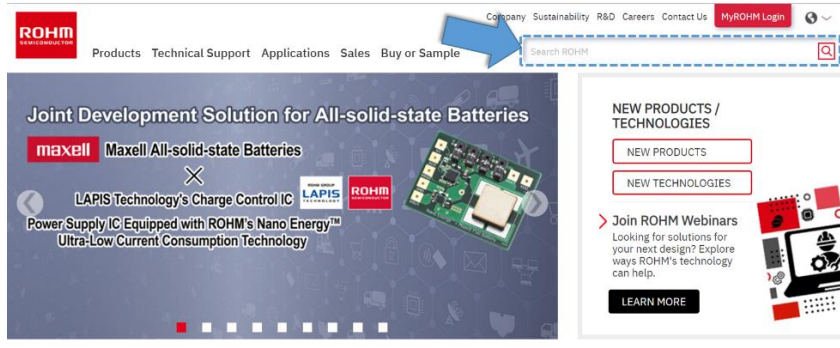

Figure 3. Search ROHM box on the home page

Step 2

- Click on the applicable model name in the search results to go to the individual product page.
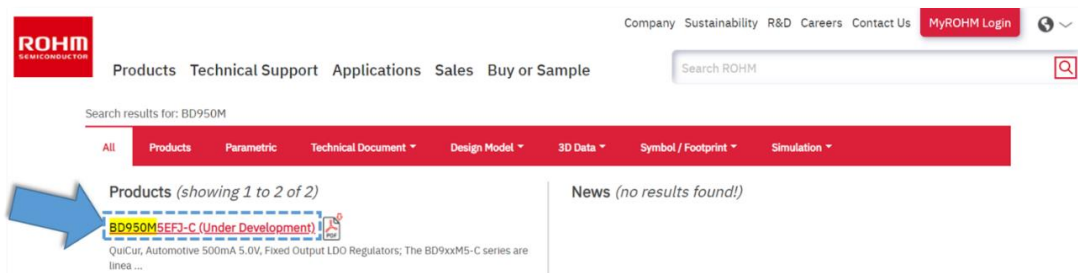

Figure 4. Example of searching for the applicable model name (BD950M5EFJ-C)

Step 3

- Click "Documents" on the product page.
- From "THERMAL DESIGN" in "Documents", download the two-resistor model application note. Note that the two-resistor model is not supported by some products.
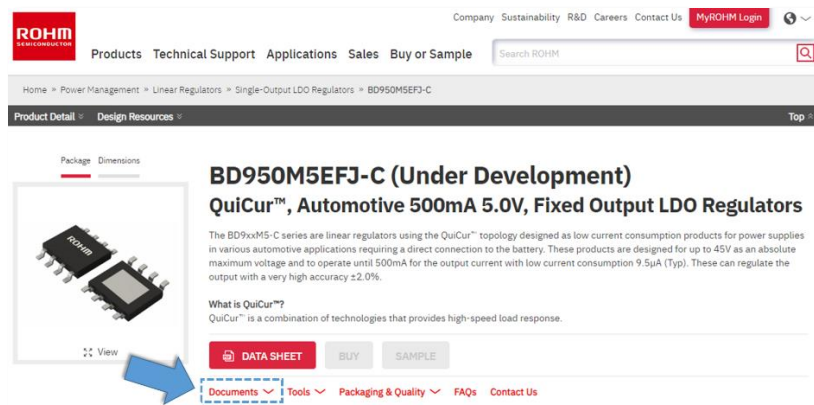

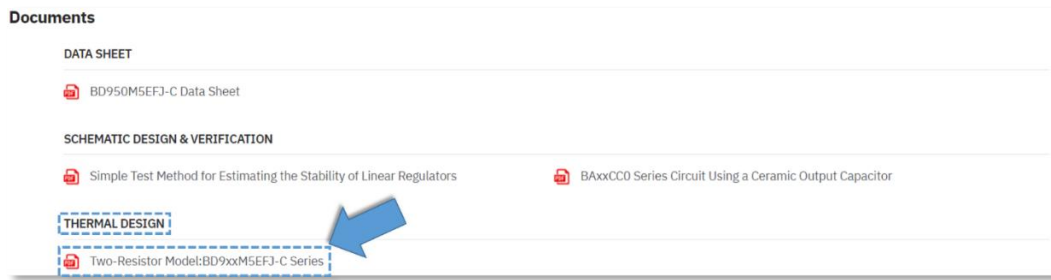Figure 5. Example of the product page (BD950M5EFJ-C)

Figure 6. Location of the link to the two-resistor model application note

Thermal simulation method

The setting method differs depending on the simulator used. This explanation uses Simcenter Flotherm™ (Siemens Industry Software Inc.).

1. As described above, obtain the two-resistor model application note for the applicable product from ROHM's website.

2. In the "Create" tab of Flotherm, select "Compact Component" to create a model.
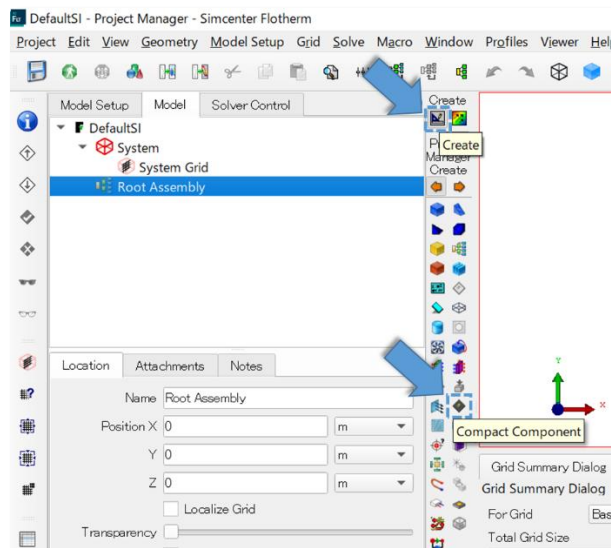

Figure 7. How to generate a compact component model

3. Select the created model and, in the "Model" tab, set the model type to "2-Resistor Model" and the junction heating value to the power consumption value expected when the device is used.
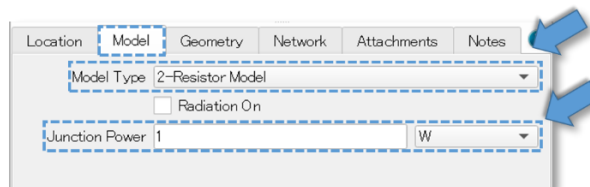

Figure 8. Example of entering the physical properties

4. By referring to the two-resistor model (Figure 9) in the application note obtained in step 1, enter the dimensions of the model to create in the "Geometry" tab as shown in Figure 10. At this time, for the top and bottom layer thickness values, enter half of the thickness in the Z-direction, respectively.
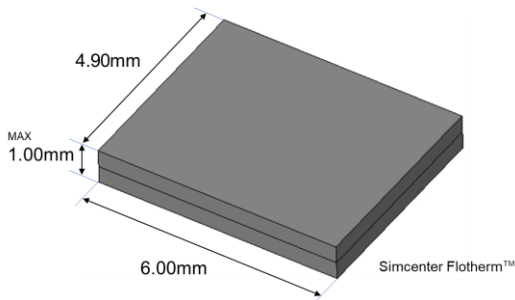
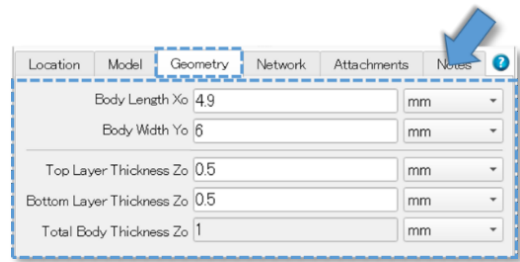Figure 9. Reference example of the two-resistor model
(Package name: HTSOP-J8)

Figure 10. Example of entering dimensions of the two-resistor model

5. By referring to the two-resistor model values (Figure 11) in the application note obtained in step 1., enter the resistance values in the "Network" tab. At this time, set the unit of thermal resistance to K/W, and enter the $\theta_{JC\text{-}TOP}$ and θ_{JB} values described on the two-resistor model application note in the Junction-Top and Junction-Bottom resistance fields, respectively.

Thermal Resistance

Element	Value
θ_{JCtop}	37.3 [°C/W]
θ_{JB}	7.1 [°C/W]

Figure 11. Reference example of the two-resistor model values
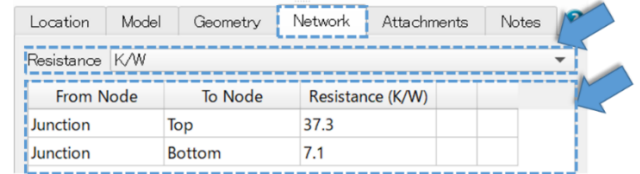(Package name: HTSOP-J8)

Figure 12. Example of entering the physical properties

6. Mount the created two-resistor model on any board and perform a thermal simulation.

Example of simulation

Based on the simulation method described above, an example of thermal design using the two-resistor model is shown below. Here, we consider as an example the detailed model of BD950M5EFJ-C mounted on a single-layer board with no via as shown in Figure 13. At this time, assume that the power consumption of the device is 1 W and that the junction temperature does not exceed 60°C.

Performing a thermal simulation under these conditions resulted in a junction temperature of 79.4°C, which exceeds the set condition of 60°C (Figure 14). To keep the junction temperature within the conditions, it is necessary to change the environmental conditions around components. However, performing a simulation using the detailed model each time after changing the conditions takes a long time. Therefore, perform the simulation using the two-resistor model, which is simpler than the detailed model.
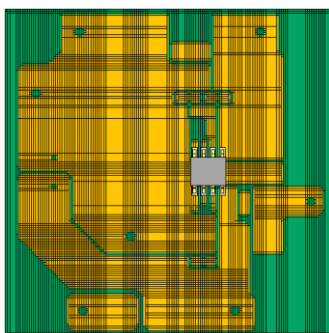

Figure 13. Example of a board on which the detailed model is mounted
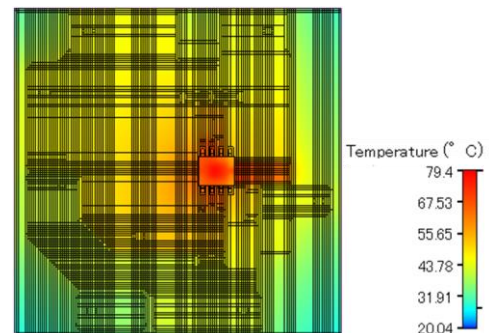

Figure 14. Results of thermal simulation of the board on which the detailed model is mounted

Using the two-resistor modeling method described above, create a two-resistor model (light blue part) as shown in Figure 15. Now, change the number of copper foil layers and the number of vias around components as shown in Figure 16 and perform a simulation. The result will show that the junction temperature is 57.8ºC, which is below 60ºC. If the simulation is actually performed using the original detailed model under the same conditions, the result will be 57.1ºC, which shows a fairly small error of less than 1ºC compared with the result using the two-resistor model. The simulation conditions and results are summarized in Table 1.
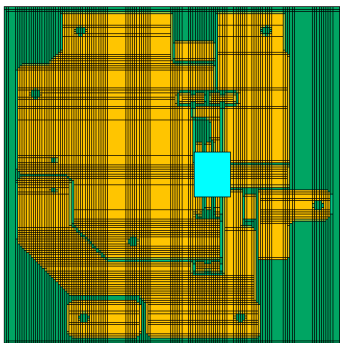

Figure 15. Board on which the two-resistor model is mounted

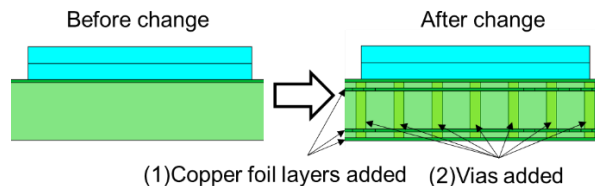(1)Copper foil layers added   (2)Vias added

Figure 16. Example of thermal improvements on a board on which the two-resistor model is mounted (Side view of the board)

Table 1. Simulation conditions and results

	Model before improvement (Detailed model)	Model after improvement (Two-resistor model)	Model after Improvement (Detailed model)
Number of Vias	0	84	84
Number of copper foil layers	1 layer (70 μ m)	4 layer (70 μ m)	4 layer (70 μ m)
Junction temperature	79.4℃	57.8℃	57.1℃

In addition, for the model after improvement, the number of grids and the time required in a simulation using the detailed model and the two-resistor model are summarized in Table 2. As shown in Table 2, the simulation using the two-resistor model requires a significantly fewer number of grids and less calculation time than the simulation using the detailed model. Note that the simulation results shown here are an example, so the time reduced by the two-resistor model will vary depending on the conditions.

Based on the above, the two-resistor model is useful when detailed changes to the condition settings are required since it enables quick simulation without large errors compared with the detailed model.

Table 2. Comparison of the model after improvement

	Two-resister model	Detailed model	Improvement rate
Number of grids	1,143,248	3,656,419	69% reduction
Simulation time	4 minutes 7 second	9 minutes 29 second	57% reduction

Finally, the specifications of the PC used this time are shown below.

OS: Windows 10 64-bit

CPU: Intel(R) Xeon(R) CPU E5-2650 v4 12-core (10 cores used)

Memory: 128 GB

Precautions for use

Since the two-resistor model is based on the thermal resistance that assumes the JEDEC Standard environment, the prediction precision will be lower as the deviation from the specific application environment becomes larger. In addition, θ_{JB} and $\theta_{JC\text{-}TOP}$ can be used as an index of the thermal performance to incorporate the device into thermal simulation models at the board level, the precision of the results will vary depending on how the information is used, other modeling and discretization errors in the environment, and the simulation software as well. Since θ_{JB} and $\theta_{JC\text{-}TOP}$ are mainly performance indices, the precision of the simulation results at the circuit board level is lower than the precision obtained with the detailed model.

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