

SPICE Modeling Report

Automotive 1ch 45 mΩ High-Side Switch with Variable OCD and OCD Mask Function BV1HD045EFJ-C

General Description

In this report, the characteristics that can be confirmed by the simulation using the SPICE model of the IPD series IC BV1HD045EFJ-C will be described.

Simulation Environment

- Circuit Simulator : PSpice / Cadence Design System, Inc.
- Version Information : 17.4-2019
- OS Information : Windows 10 64-bit Edition

File Information

- Library File Name : BV1HD045EFJ-C_PSpice.lib
- Symbol File Name : BV1HD045EFJ-C.olb
- Subcircuit and Symbol

Table 1 Correspondence Table

Product Name	Subcircuit	Symbol
BV1HD045EFJ-C	TOP_BV1HD045	TOP_BV1HD045

Caution

- These model characteristics are specifically at Ta = 25 °C. Thus, the simulation result with temperature variances may significantly differ from the result with the one done at actual application board (actual measurement).
- The simulation result and characteristics described in this report may differ depending on the board design. It is recommended to perform the measurement on the actual board to verify the result.
- The values from the simulation results are not guaranteed. Use these results as a guide for your design.
- Actual measurement was done using a specific sample, thus the measured data is just as a reference.

BV1HD045EFJ-C Spice Model

■ Pin Information

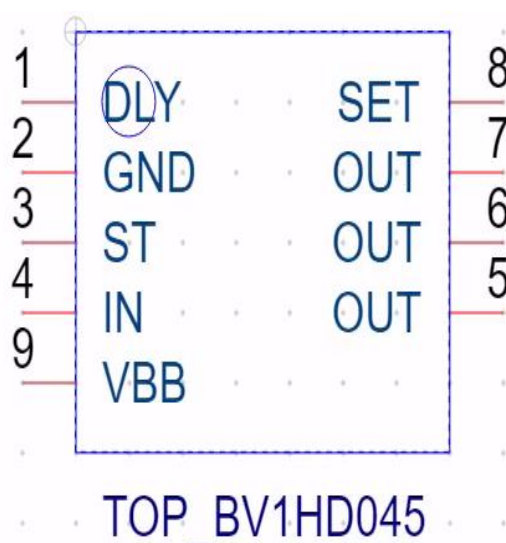


Figure 1. Symbol of BV1HD045EFJ-C

Table 2 Subcircuit Pin Table

Pin No.	Pin Name	Function
1	DLY	Over current mask time setting pin
2	GND	GND pin
3	ST	Diagnostic output pin
4	IN	Input pin, with internal pull-down resistor
5 to 7	OUT	Output pin
8	SET	Over current limit value setting pin
9	VBB	The EXP-PAD is connected to VBB

Verifiable Characteristics

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Electrical Characteristics (vs. Datasheet)

Table 3 Electrical Characteristics Comparison

(Unless otherwise specified $6\text{ V} \leq V_{\text{BB}} \leq 28\text{ V}$, $T_a = 25\text{ }^{\circ}\text{C}$)

Parameter	Modeled (Note 1)	Design Value		Unit	Error	Condition
		Datasheet	SPICE			
[Power Supply]						
Standby Current	Yes	-	0.01	μA	-	V _{BB} = 14 V, V _{IN} = 0 V V _{OUT} = 0 V
Operating Current	Yes	3	3.0	mA	0%	V _{BB} = 14 V, V _{IN} = 5 V V _{OUT} = open
UVLO Detection Voltage	Yes	-	3.1	V	-	
UVLO Hysteresis Voltage	Yes	0.30	0.30	V	0%	
[Input (V _{IN})]						
High-Level Input Voltage	Yes	-	2.3	V	-	
Low-Level Input Voltage	Yes	-	2.0	V	-	
Input Voltage Hysteresis	Yes	0.3	0.3	V	0%	
High-Level Input Current	Yes	50	50	μA	0%	V _{IN} = 5 V
Low-Level Input Current	Yes	-	0	μA	-	V _{IN} = 0 V
[Output]						
Output On Resistance	Yes	45	45.0	mΩ	0%	V _{BB} = 8 V to 19 V, I _{OUT} = 1A
	Yes	-	55.2	mΩ	-	V _{BB} = 4.5 V, I _{OUT} = 1A
Output Leak Current	Yes	-	0	μA	-	V _{IN} = 0 V, V _{OUT} = 0 V
Output ON Slew Rate	Yes	0.3	0.30	V/μs	0%	V _{BB} = 14 V, R _L = 6.5 Ω
Output OFF Slew Rate	Yes	0.3	0.30	V/μs	0%	V _{BB} = 14 V, R _L = 6.5 Ω
Output ON Propagation Delay Time	Yes	70	69.8	μs	0.2%	V _{BB} = 14 V, R _L = 6.5 Ω
Output OFF Propagation Delay Time	Yes	50	49.7	μs	0.6%	V _{BB} = 14 V, R _L = 6.5 Ω
Output Clamp Voltage	Yes	48	48.0	V	0%	V _{IN} = 0 V, I _{OUT} = 10 mA
[Diagnostic Output]						
Diagnostic Output Low Voltage	Yes	-	0.17	V	-	V _{IN} = 5 V, I _{ST} = 1 mA
Diagnostic Output Leak Current	Yes	-	0	μA	-	V _{IN} = 0 V, V _{ST} = 5 V
Diagnostic Output ON Propagation Delay Time	Yes	100	100	μs	0%	V _{BB} = 14 V, R _L = 6.5 Ω
Diagnostic Output OFF Propagation Delay Time	Yes	50	50.4	μs	0.8%	V _{BB} = 14 V, R _L = 6.5 Ω
[Diagnostic Function]						
Fixed Over Current Limit	Yes	30	30.0	A	0%	V _{IN} = 5 V
Variable Over Current Limit	Yes	4.1	4.10	A	0%	V _{IN} = 5 V, R _{SET} = 47 kΩ
Open Load Detection Voltage	Yes	3.0	3.0	V	0%	V _{IN} = 0 V
Open Load Detection Sink Current	Yes	-10	-10.0	μA	0%	V _{IN} = 0 V, V _{OUT} = 5 V

(Note 1) Yes: Model available (supported), No: Model not available (not supported).

Characteristic in SPICE (vs. Measured Waveform)
1. Standby Current

Simulation Setting

Type: Transient

Run Time: 100 s

(Maximum Step Size: 10 ms)

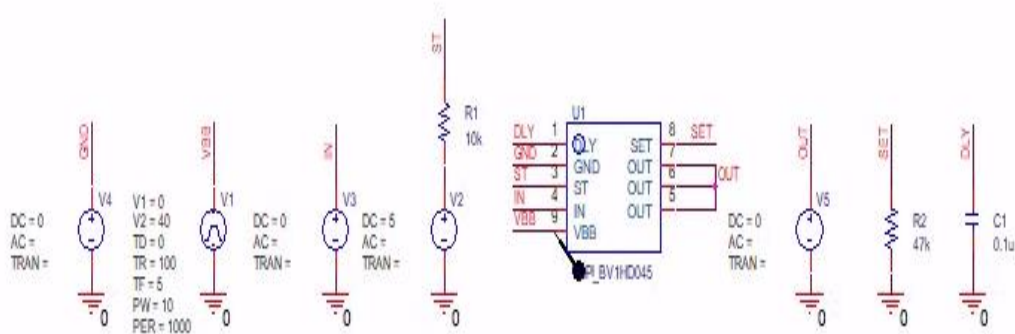


Figure 2.
Simulation Schematic 1

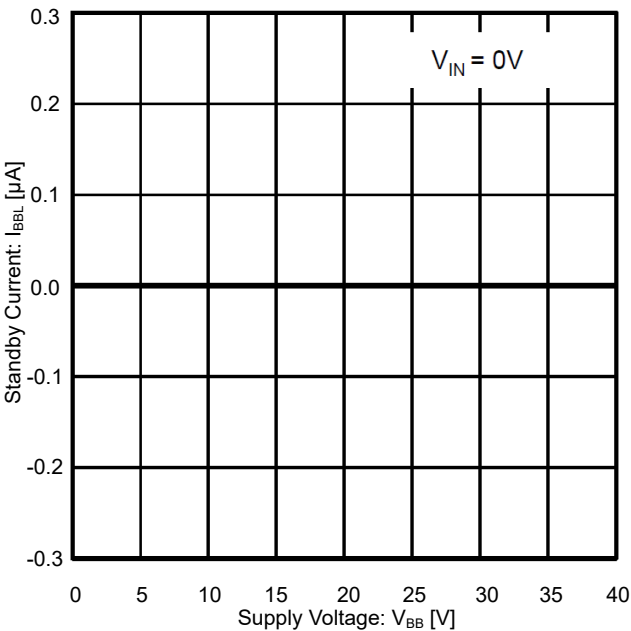


Figure 3.
Standby Current
(Measured Waveform)

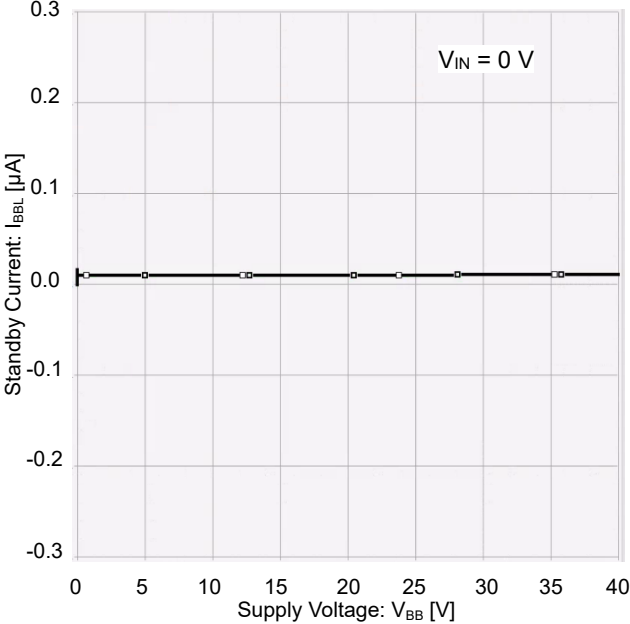


Figure 4.
Standby Current
(SPICE Simulation)

Table 4 Characteristics Comparison

Parameter	Measured Result (Note1)(Note2)	SPICE Simulation Result	Unit	Error	Condition
Standby Current	0.0	0.01	μA	-	V _{BB} = 14 V, V _{IN} = 0 V, V _{OUT} = 0 V

(Note 1) The above data is based on a specific sample and it is not a guaranteed value.
(Note 2) These characteristics depend on some dynamic characteristics of external components, input signal speed, PCB pattern and mounting condition of each on-board parts.

2. Operating Current

Simulation Setting
 Type: Transient
 Run Time: 100 s
 (Maximum Step Size: 10 ms)

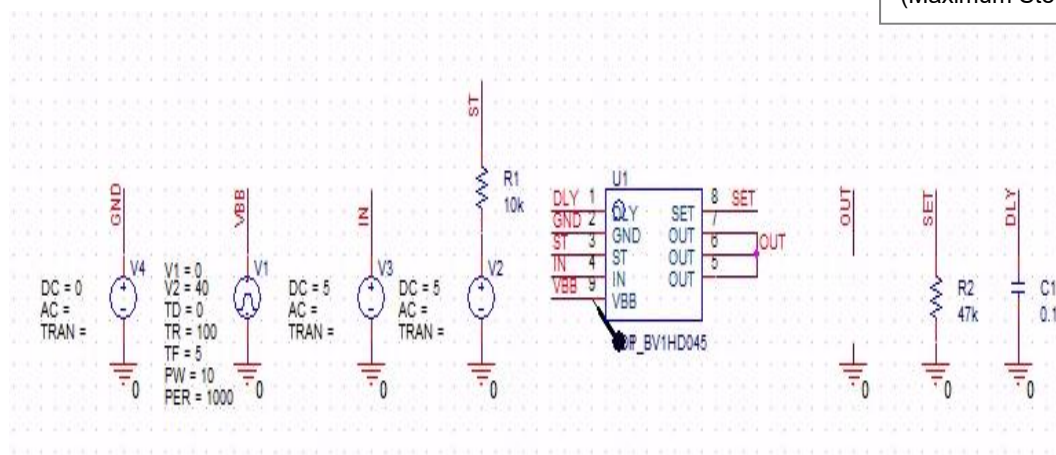


Figure 5.
Simulation Schematic 2

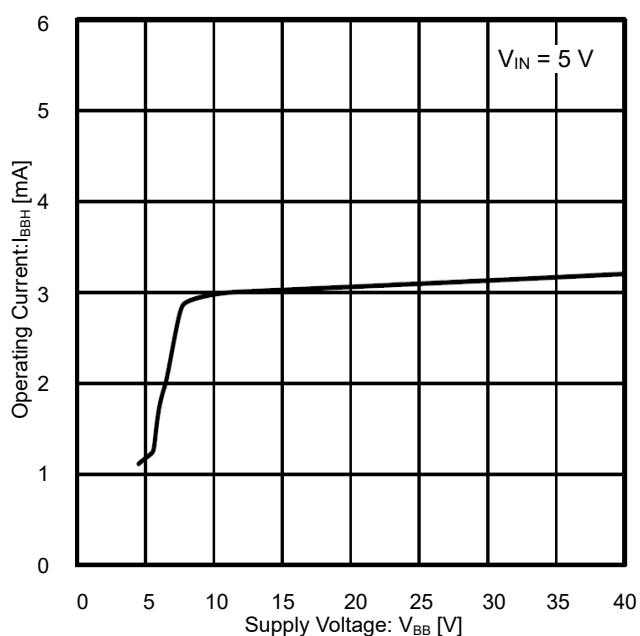


Figure 6.
Operating Current
(Measured Waveform)

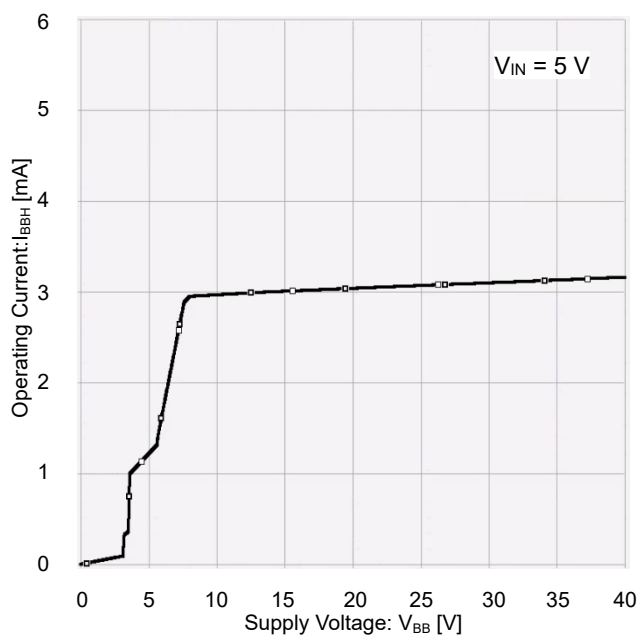


Figure 7.
Operating Current
(SPICE Simulation)

Table 5 Characteristics Comparison

Parameter	Measured Result (Note1)(Note2)	SPICE Simulation Result	Unit	Error	Condition
Operating Current	3.0	3.0	mA	0.0 %	$V_{BB} = 14 \text{ V}$, $V_{IN} = 5 \text{ V}$, OUT = OPEN

(Note 1) The above data is based on a specific sample and it is not a guaranteed value.

(Note 2) These characteristics depend on some dynamic characteristics of external components, input signal speed, PCB pattern and mounting condition of each on-board parts.

3. Output On Resistance

Simulation Setting

Type: Transient

Run Time: 0.5 ms

(Maximum Step Size: 1 us)

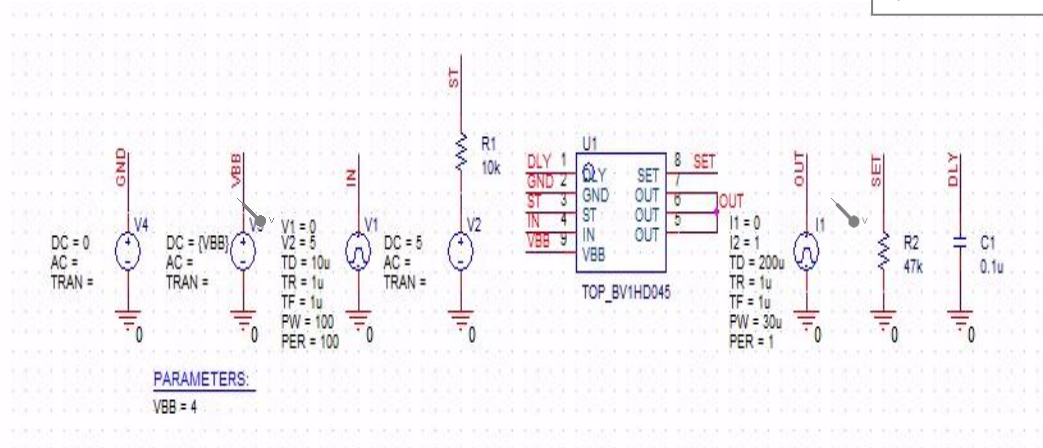
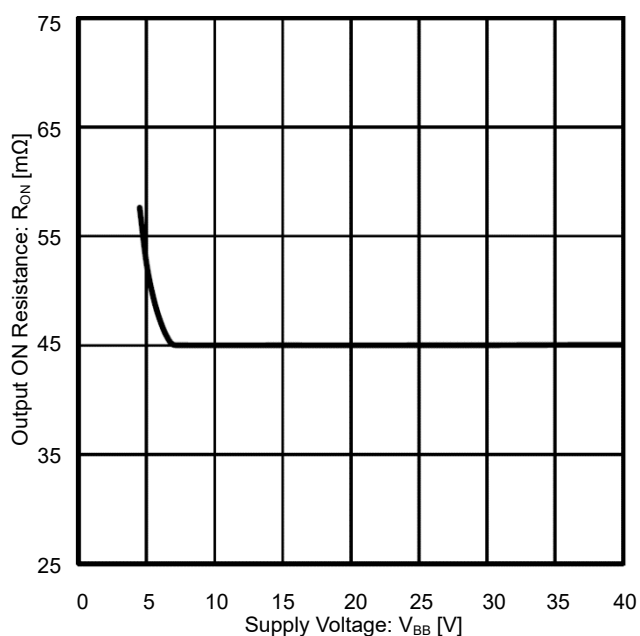
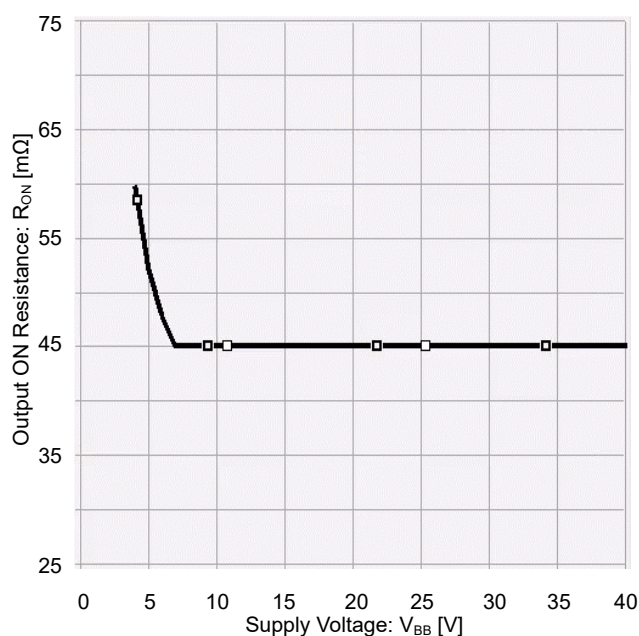
Figure 8.
Simulation Schematic 3Figure 9.
Output On Resistance
(Measured Waveform)Figure 10.
Output On Resistance
(SPICE Simulation)

Table 6 Characteristics Comparison

Parameter	Measured Result (Note1)(Note2)	SPICE Simulation Result	Unit	Error	Condition
Output On Resistance (V _{BB} = 8 to 19 V)	45	45.0	mΩ	0.0 %	V _{BB} = 8 V to 19 V V _{BB} = 4.5V, I _{OUT} = 1 A
Output On Resistance (V _{BB} = 4.5 V)	55.9	55.2	mΩ	0.2 %	

(Note 1) The above data is based on a specific sample and it is not a guaranteed value.

(Note 2) These characteristics depend on some dynamic characteristics of external components, input signal speed, PCB pattern and mounting condition of each on-board parts.

4. Variable Over Current Limit

Simulation Setting

Type: Transient

Run Time: 20 ms

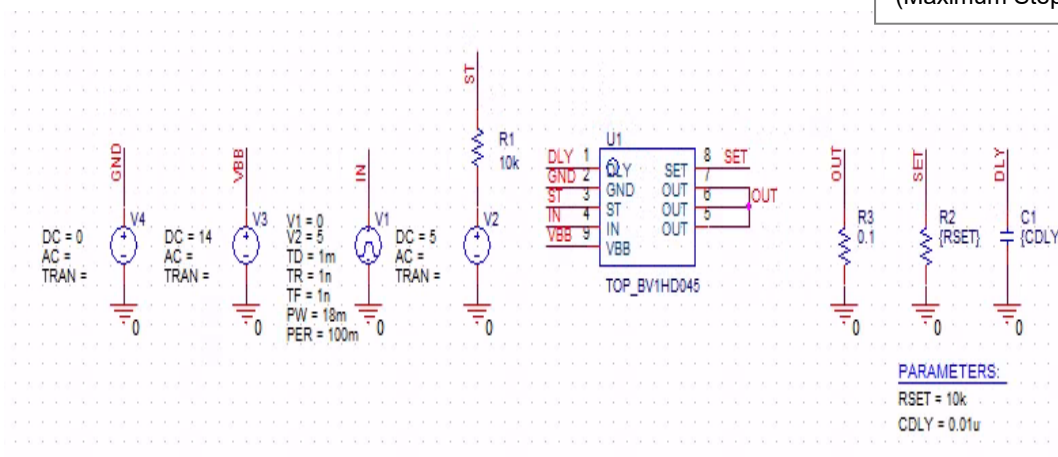
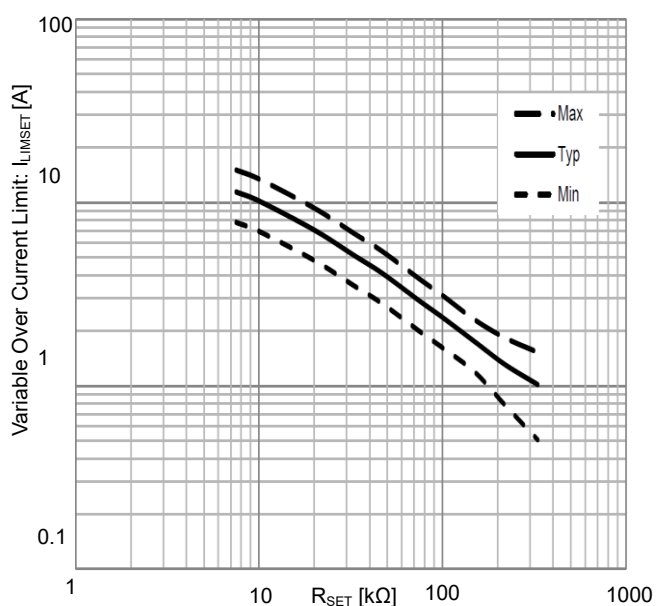
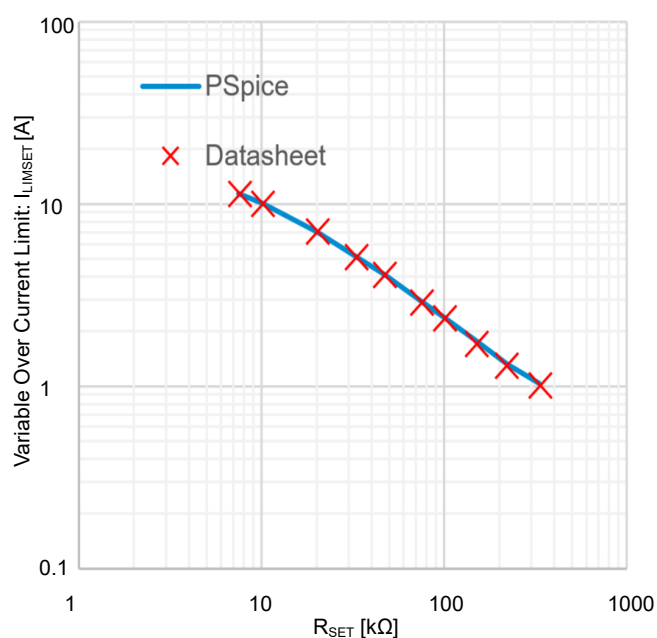
(Maximum Step Size: 1 μ s)Figure 11.
Simulation Schematic 4Figure 12.
Variable Over Current Limit
(Measured Waveform)Figure 13.
Variable Over Current Limit
(SPICE Simulation)

Table 7 Characteristics Comparison

Parameter	Measured Result (Note1)(Note2)	SPICE Simulation Result	Unit	Error	Condition
Variable Over Current Limit	4.1	4.10	A	0.0 %	V _{BB} = 14 V, V _{IN} = 0 to 5 V, OUT = 0.1 to 6.5 Ω , ST = 10 k Ω to 5 V, R _{SET} = 47 k Ω , C _{DLY} = 0.01 μ F

(Note 1) The above data is based on a specific sample and it is not a guaranteed value.

(Note 2) These characteristics depend on some dynamic characteristics of external components, input signal speed, PCB pattern and mounting condition of each on-board parts.

5. Variable Over Current Mask Time

Simulation Setting

Type: Transient

Run Time: 200 ms

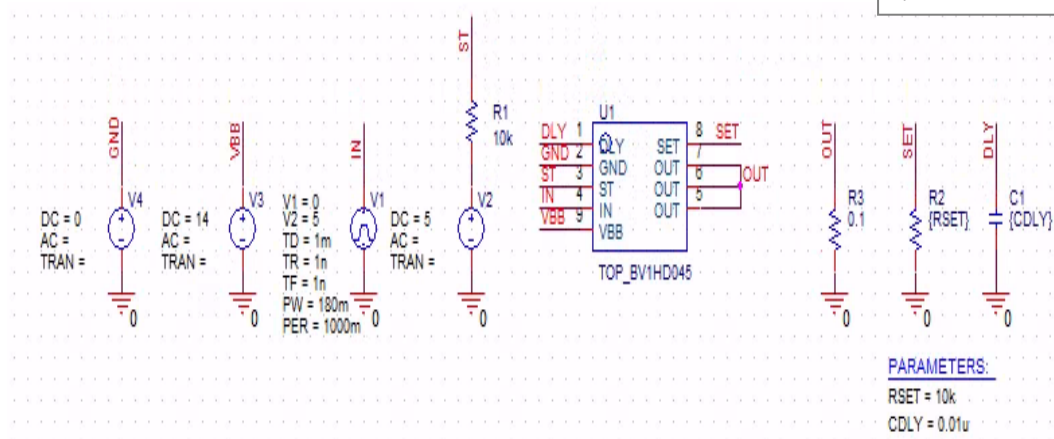
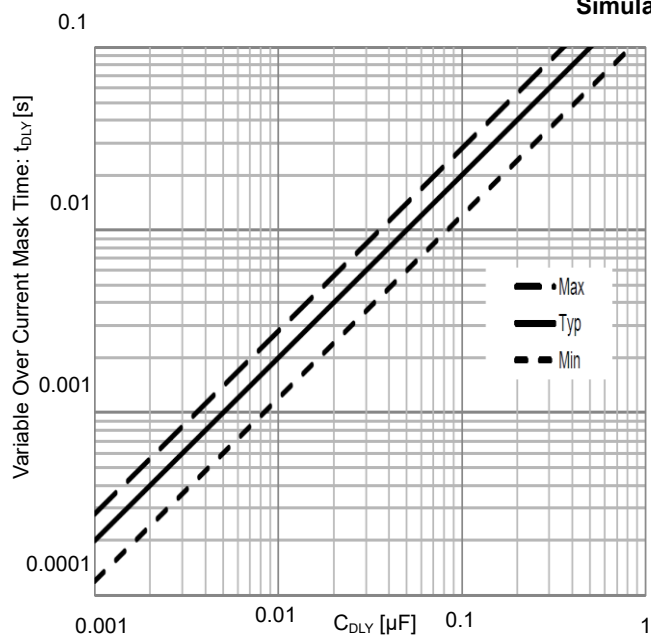
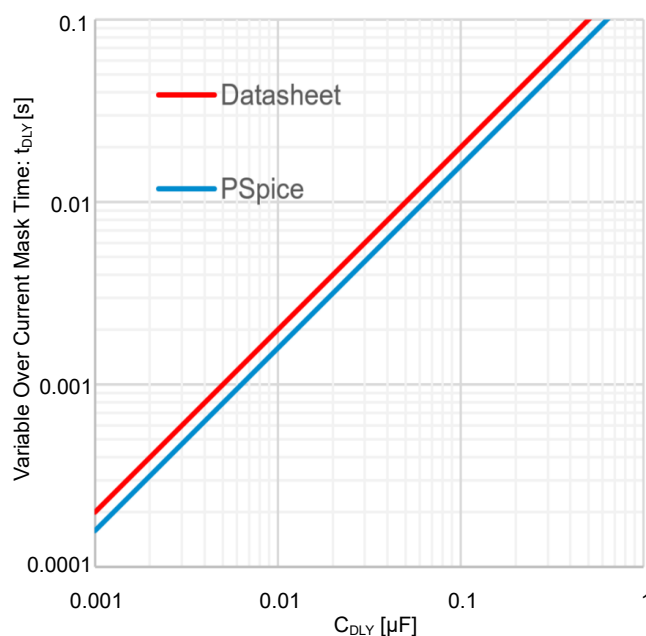
(Maximum Step Size: 1 μ s)Figure 14.
Simulation Schematic 5Figure 15.
Variable Over Current Mask Time
(Measured Waveform)Figure 16.
Variable Over Current Mask Time
(SPICE Simulation)

Table 8 Characteristics Comparison

Parameter	Measured Result (Note1)(Note2)	SPICE Simulation Result	Unit	Error	Condition
Variable Over Current Mask Time	0.0016	0.00159	s	0.6 %	V _{BB} = 14 V, V _{IN} = 0 to 5 V, OUT = 0.1 to 6.5 Ω , ST = 10 k Ω to 5 V, R _{SET} = 47 k Ω , C _{DLY} = 0.01 μ F

(Note 1) The above data is based on a specific sample and it is not a guaranteed value.

(Note 2) These characteristics depend on some dynamic characteristics of external components, input signal speed, PCB pattern and mounting condition of each on-board parts.

6. Timing Chart (Propagation Delay Time)

Simulation Setting
Type: Transient
Run Time: 0.5 ms
(Maximum Step Size: 1 μ s)

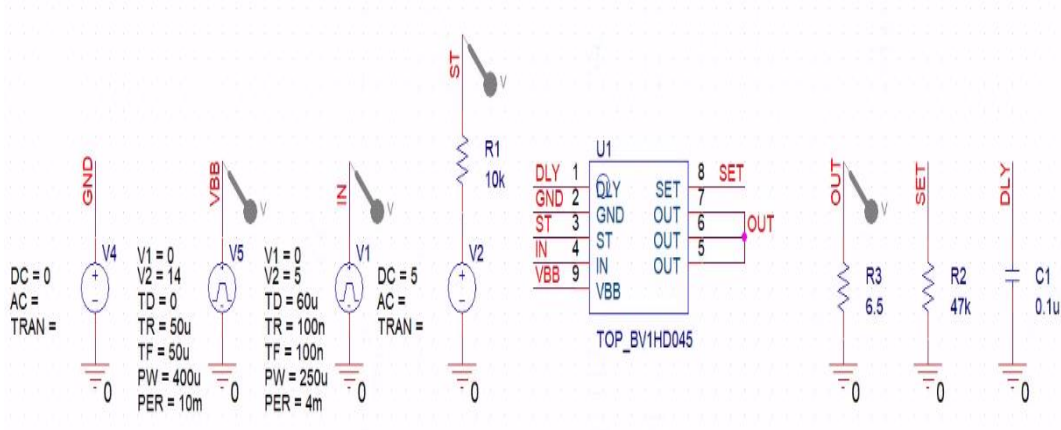


Figure 17.
Simulation Schematic 6

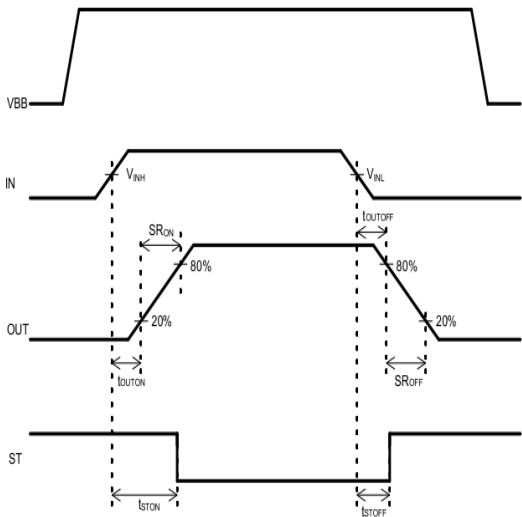


Figure 18.
Timing Chart (Propagation Delay Time)
(Target Waveform)

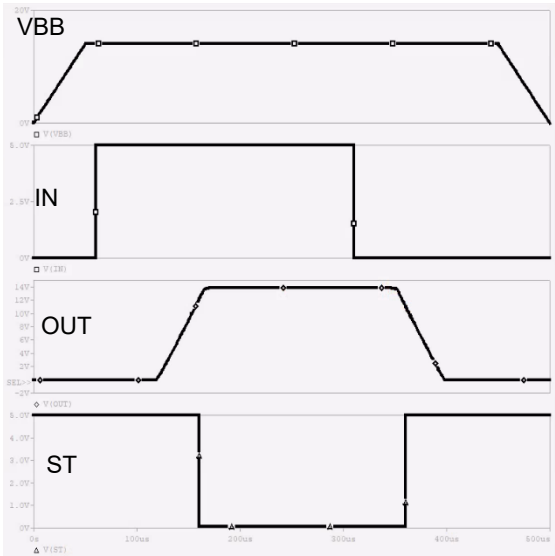


Figure 19.
Timing Chart (Propagation Delay Time)
(SPICE Simulation)

7. Over Current Limiting Operation

Simulation Setting
Type: Transient
Run Time: 20 ms
(Maximum Step Size: 1 μ s)

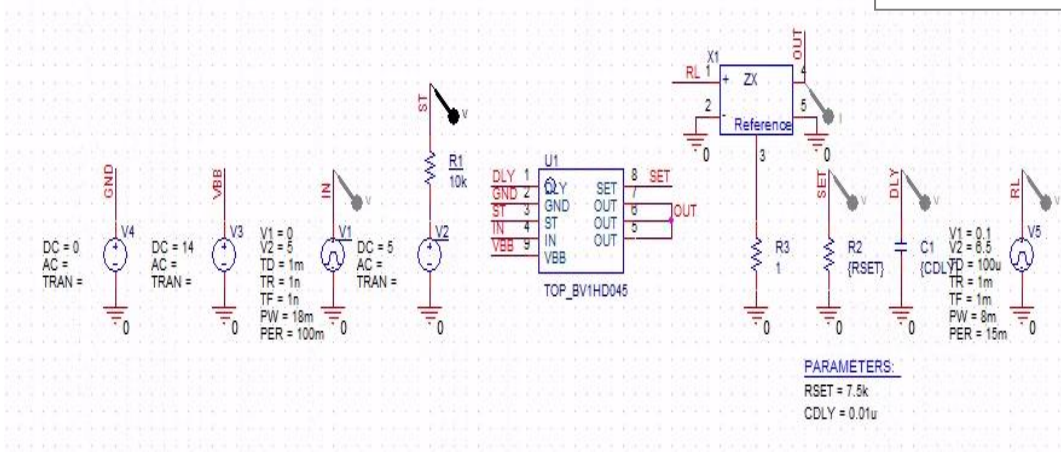


Figure 20.
Simulation Schematic 7

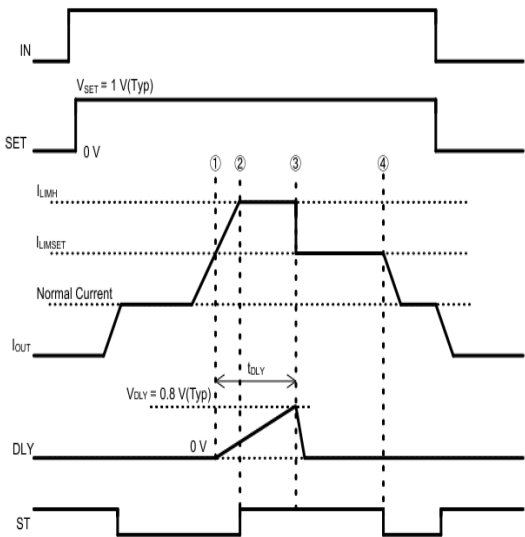


Figure 21.
Over Current Limiting Operation
(Target Waveform)

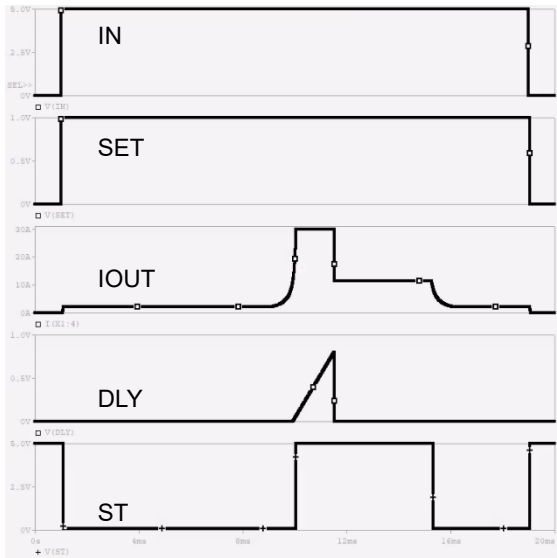


Figure 22.
Over Current Limiting Operation
(SPICE Simulation)

Revision History

Date	Revision	Changes
May.2023	001	New Release

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