System Reference for Automotive application

BD18330EFV-M / BD18332EUV-M
Application note for design

Abstract

Purpose

This document describes topics for Animation lamp design.

Agenda

Contents

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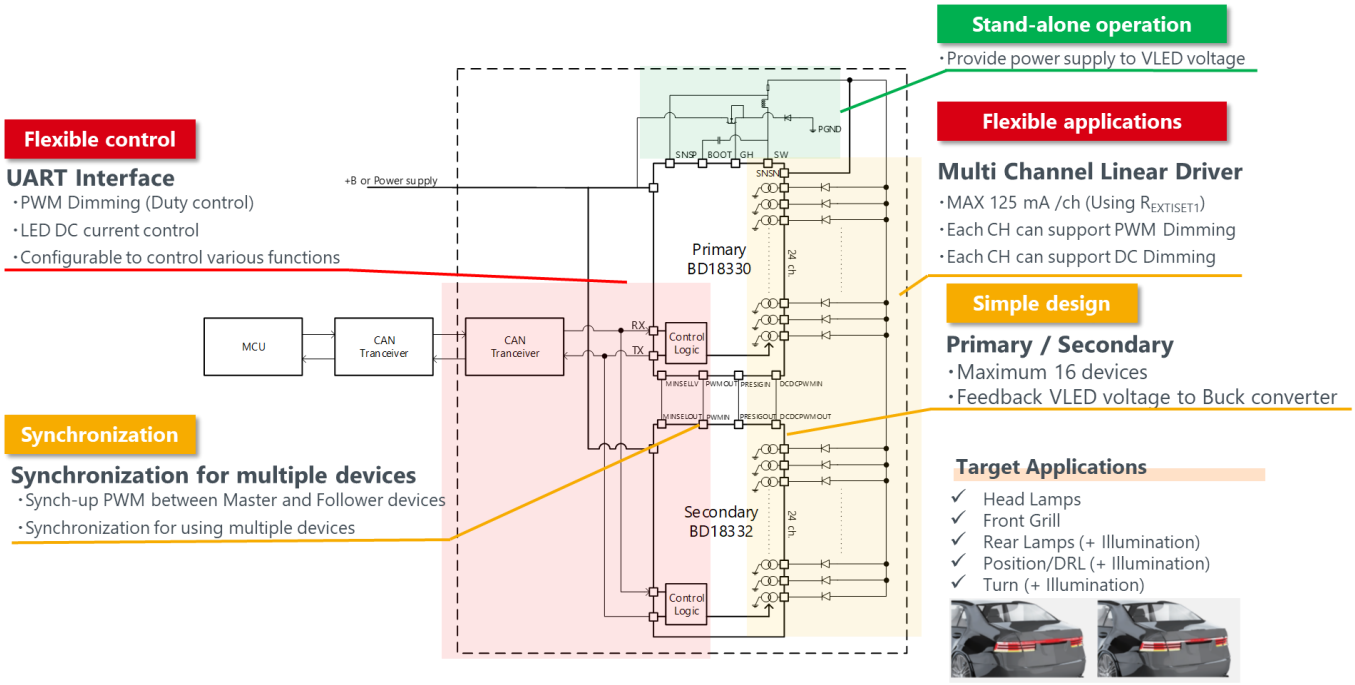
1-1. Features : BD1833x series

Product overview of BD18330EFV-M and BD18332EUV-M



1-2-1. Product overview : BD18330EFV-M

Key Features

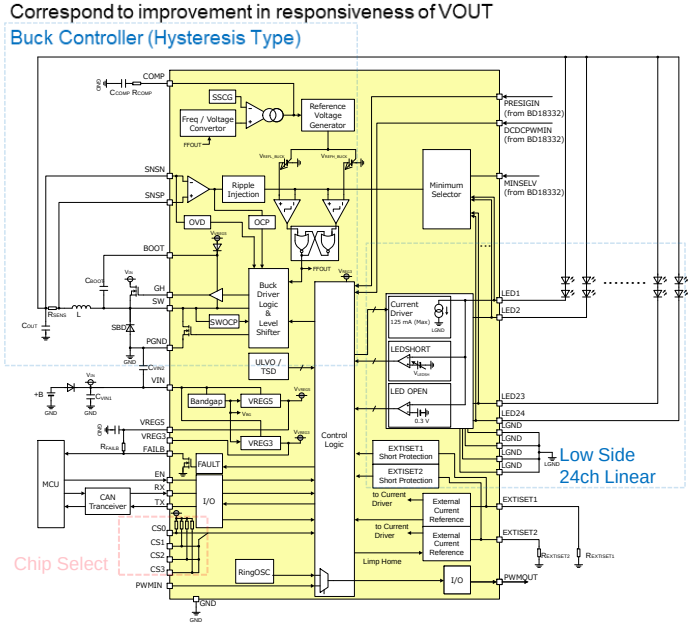
- ✓ 1ch Buck Controller(Hysteresis Type)
  + 24ch Linear LED Driver(Integrated FET)
- ✓ Input Voltage Range ：4.5～42V
- ✓ LEDx Pin Absolute Maximum Rating：42V
- ✓ Maximum Output Current ：125mA/ch (Total：3.0A)
- ✓ LED Current Accuracy：±5.5%@60mA
  （Ta=-40～125℃）
- ✓ Switching frequency：400kHz
- ✓ Output PWM Frequency：488Hz/967Hz/1952Hz/3904Hz
- ✓ UART interface (Max. 1Mbps)
  - Maximum 16 devices
  - Output Current DC Dimming
  - Output Current PWM ON Duty
  - PWM phase setting
  - OUT Pin Short Circuit Protection threshold
  - Diagnosis Enable function threshold
- ✓ LED Open Detection / LED Short Detection
- ✓ Fault diagnosis (FAILB)
- ✓ UVLO,TSD protection
- ✓ Built-in Limp Home Function

Target Applications

- ✓ Rear Lamps (+ Illumination)
- ✓ Position/DRL (+ Illumination)
- ✓ Turn (+ Illumination)

Block Diagram

Frequency stabilization Bang-Bang Type adopted.
Correspond to improvement in responsiveness of VOUT



Package

- ✓ HTSSOP-B54

1-2-2. Product overview : BD18332EUV-M

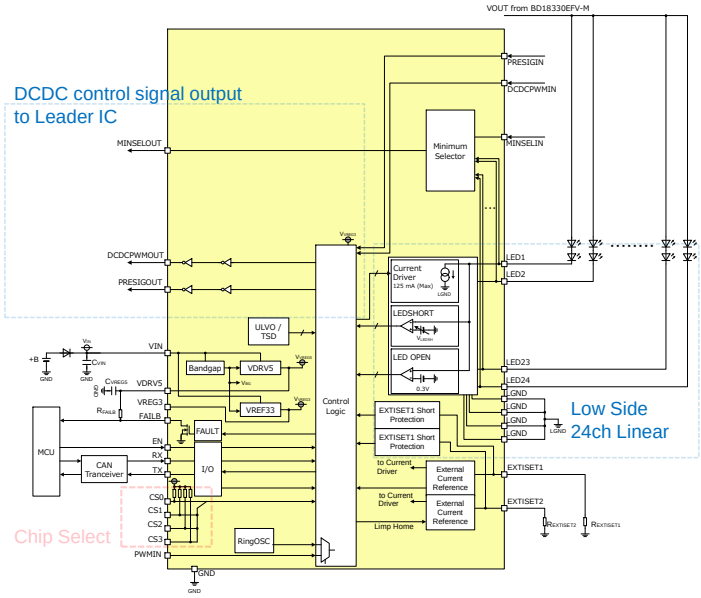
Key Features

- ✓ 24ch Linear LED Driver(Integrated FET)
- ✓ Input Voltage Range ：4.5～42V
- ✓ LEDx Pin Absolute Maximum Rating：42V
- ✓ Maximum Output Current ：125mA/ch (Total：3.0A)
- ✓ LED Current Accuracy：±5.5%@60mA
  （Ta=-40～125℃）
- ✓ Switching frequency：400kHz
- ✓ Output PWM Frequency：488Hz/967Hz/1952Hz/3904Hz
- ✓ UART interface (Max. 1Mbps)
  - Maximum 16 devices
  - Output Current DC Dimming
  - Output Current PWM ON Duty
  - PWM phase setting
  - OUT Pin Short Circuit Protection threshold
  - Diagnosis Enable function threshold
- ✓ LED Open Detection / LED Short Detection
- ✓ Fault diagnosis (FAILB)
- ✓ UVLO,TSD protection
- ✓ Built-in Limp Home Function

Target Applications

- ✓ Rear Lamps (+ Illumination)
- ✓ Position/DRL (+ Illumination)
- ✓ Turn (+ Illumination)

Block Diagram



Package

- ✓ HTSSOP-C48

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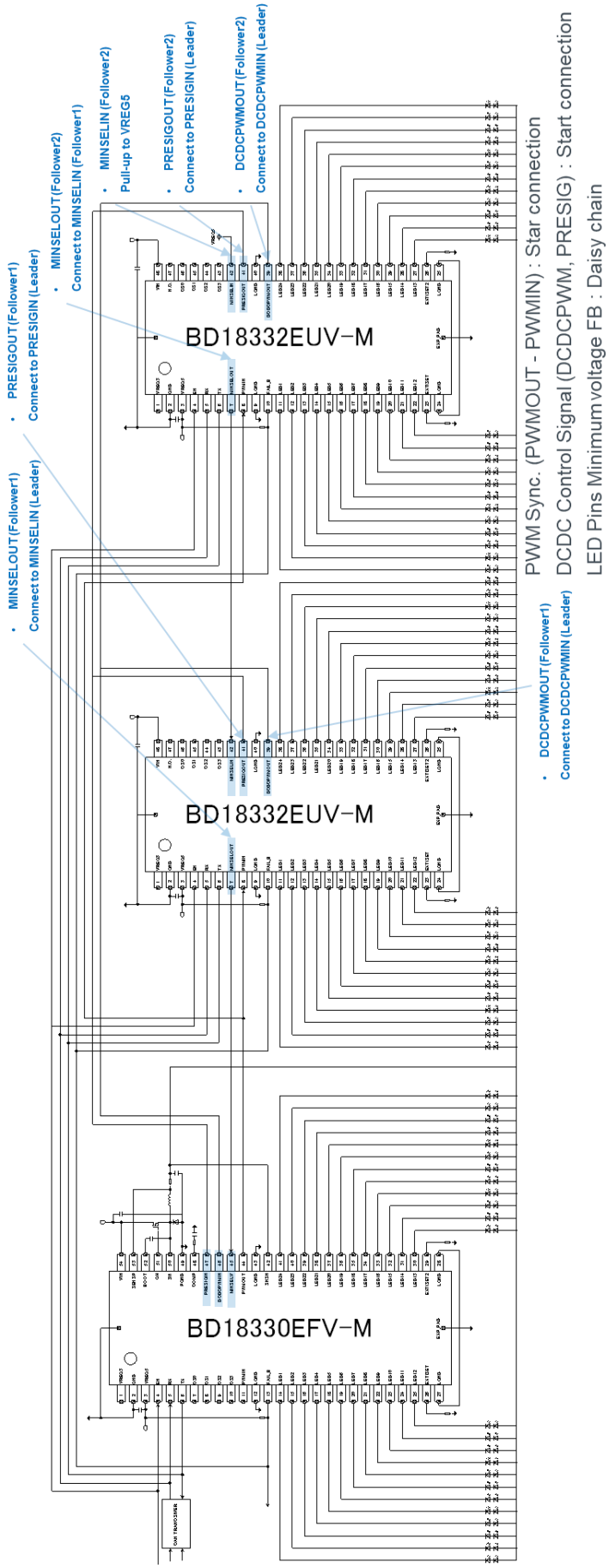
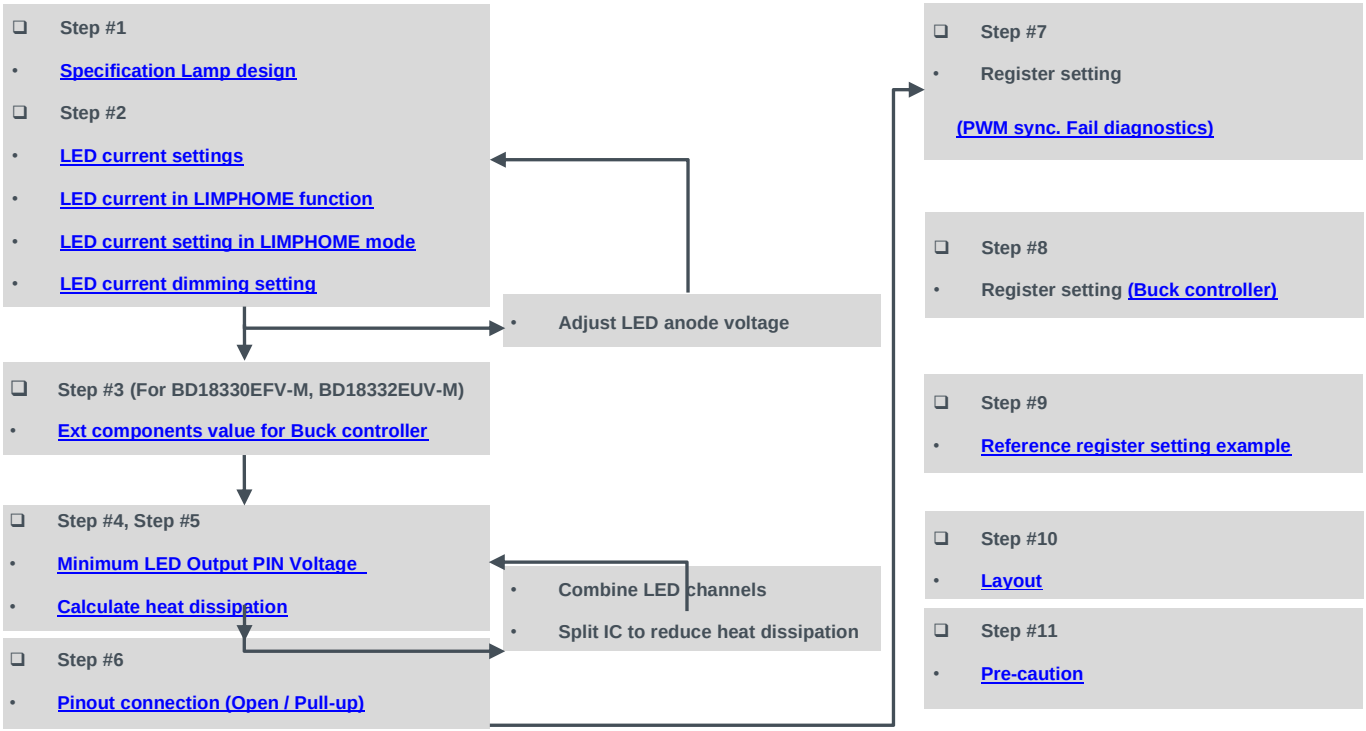
1-3. Schematic configuration example



2-1. Design flowchart

Design flow for BD18330EFV-M & BD18332EUV-M

Below flow-chart describes step by step design procedures.



2-2. Lamp Design Specification

1st step : Specification of Animation Lamp design example

Extracting of design specification.

Operating condition

Item	Provided by	Min.	Typ.	Max.	Note
VIN,EN voltage	+B	9V	12V	16V	Need VIN > 5.5V
LED forward voltage	-	3V	3.2V	3.5V	-
LED current / string	-		90mA		-
LED current / channel	-		45mA		-
LED anode voltage	External buck	4.2V	4.4V	4.7V	Provided by module

System configuration

Item	Information	Note
Numbers of LEDs	72	-
LEDs/string in series	1	-
Numbers of layer of PCB board	4	Recommend 4layer
LIMPHOME function	YES	-

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2-3-1. LED current setting

2nd step : LED current settings

The table describes DC current settings in each modes. LED current dimming can be done by internal register setting.

LED current setting by Modes *Dim ratio depends on register setting

MODE	REXTISET1	REXTISET2	ILEDx Requirement	Formula	Register setting	Dimming register value
Normal1	-	-	0.045A	$I_{LED1} = \frac{(DCDIM[3:0]+1)}{16} \times 0.060$ $I_{LED2} = \frac{(DIMSET[7:0]+1)}{256} \times 0.060$	ISETSEL = 0 (note1) DIMMODE = 0 DIMMODE = 1	DCDIM[3:0] = 0xB DIMSET[7:0] = 0xC3
Normal2	160kohm	-	0.045A	$I_{LED1} = \frac{(DCDIM[3:0]+1)}{16} \times (\frac{V_{EXTISET1}}{R_{EXTISET1}} \times 12000)$ $I_{LED2} = \frac{(DIMSET[7:0]+1)}{256} \times (\frac{V_{EXTISET1}}{R_{EXTISET1}} \times 12000)$	ISETSEL = 1 DIMMODE = 0 DIMMODE = 1	-
LIMPHOME1	-	80kohm	0.045A	$I_{LIMPHOME1} = \frac{V_{EXTISET2}}{R_{EXTISET2}} \times 12000$ $I_{LIMPHOME1} = \frac{0.3}{80k} \times 12000 = 0.045A$	-	-

Note1 : Not Recommended Setting

2-3-2. LED current setting

2nd step : LED current settings

The table describes DC current settings in each modes. LED current dimming can be done by internal register setting.

LED current setting by Modes *Dim ratio depends on register setting

MODE	REXTISET1	REXTISET 2	ILEDx Requirement	Formula	Register setting		Dimming register value
LIMPHOME2-1	-	-	0.045A	$I_{LIMPHOME2\_1} = \frac{(DCDIM[3:0]+1)}{16} \times 0.060$ $I_{LIMPHOME2\_1} = \frac{(DIMSET[7:0]+1)}{256} \times 0.060$	LEXTISET2SEL = "0" *Datasheet p52	ISETSEL = 0 DIMMODE = 0 DIMMODE = 1	DCDIM[3:0] = 0xB DIMSET[7:0] = 0xC3
	160kohm	-	0.045A	$I_{LIMPHOME2\_1} = \frac{(DCDIM[3:0]+1)}{16} \times (\frac{V_{EXTISET1}}{R_{EXTISET1}} \times 12000)$ $I_{LIMPHOME2\_1} = \frac{(DIMSET[7:0]+1)}{256} \times (\frac{V_{EXTISET1}}{R_{EXTISET1}} \times 12000)$		*Recommend ISETSEL = 1 DIMMODE = 0 DIMMODE =1	-
LIMPHOME2-2	160kohm	80kohm	0.090A	$I_{LEDLIMPHOME2\_2} = \frac{(DCDIM[3:0]+1)}{16} \times (\frac{V_{EXTISET1}}{R_{EXTISET1}} + \frac{V_{EXTISET2}}{R_{EXTISET2}}) \times 12000$	LEXTISET2SEL = "1" *Datasheet p52	ISETSEL = 1 DIMMODE = 0	-
	160kohm	80kohm	0.090A	$I_{LEDLIMPHOME2\_2} = \frac{(DIMSET[7:0]+1)}{256} \times (\frac{V_{EXTISET1}}{R_{EXTISET1}} + \frac{V_{EXTISET2}}{R_{EXTISET2}}) \times 12000$		ISETSEL = 1 DIMMODE =1	-

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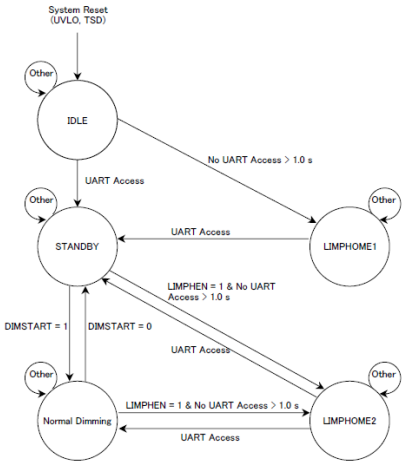
2-3-3. LED current setting

2nd step : Register settings for LIMPHOME function

Item	LED current	DIM mode	Note
LIMPHOME1 LED current	45mA	DC/PWM dimming	100% fixed
LIMPHOME2 LED current	45mA	DC/PWM dimming	Set by register

LIMPHOME function flow chart



State	Description	Dimming setting		
		Current reference setting	DC current setting	PWM duty setting
IDLE	Reset condition, No lighting	-	-	-
STANDBY	During initial setting, No lighting	-	-	-
LIMPHOME1	lighting by EXTISET2 resistor (UART error condition)	EXTISET2	100 % (DCDIMx)	100 % (LHDTYx)
Normal Dimming	Normal dimming condition	ISETSEL = 0 (Internal ISET) ISETSEL = 1 (EXTISET1) ※ISETSEL=0 (Note 1)	DIMMODE = 0 DCDIMx DIMMODE = 1 DIMSETx	DIMMODE = 0 DIMSETx DIMMODE = 1 100 %
LIMPHOME2	lighting by UART LIMPHOME setting (UART error condition)	LEXTISET2SEL = 1 *(Note 1)* EXTISET1 + EXTISET2 LEXTISET2SEL = 0 ISETSEL = 0 (Internal ISET) ISETSEL = 1 (EXTISET1)	DIMMODE = 0 DCDIMx DIMMODE = 1 DIMSETx	LHDTYx

(Note 1) Not Recommended Setting

2-3-4. LED current setting

2nd step : Settings Zero LED Current in LIMPHOME mode

If LIMPHOME modes are not being used, leave REXTISET2 terminal open sets LED current to Zero.

Conditions for Zero current in LIMPHOME mode

MODE	REXTISET1	REXTISET2	ILEDx Requirement	Register setting mandatory
LIMPHOME1 No LED current	-	Open	0A	-
LIMPHOME2 No LED current	-	Open	0A	LEXTISET2SEL = "1" (Initial) *BD18330 Datasheet p58

❑ **Normal current setting**

$$I_{Normal} = \frac{V_{EXTISET1}}{R_{EXTISET1}} \times 12000 \ (\mathbf{ISETSEL = 1})$$

❑ **LIMPHOME1 current setting xx mA**

$$I_{LIMPHOME1} = \frac{V_{EXTISET2}}{R_{EXTISET2}} \times 12000$$

❑ **LIMPHOME1 current setting 0 A**

$$R_{EXTISET2} = Open$$

❑ **LIMPHOME2-1 current setting xx mA**

$$I_{LIMPHOME2\_1} = \frac{V_{EXTISET1}}{R_{EXTISET1}} \times 12000$$

LEXTISET2SEL = "0" ISETSEL = "1"

❑ **LIMPHOME2-2 current setting 0 A**

$$R_{EXTISET2} = Open$$

LEXTISET2SEL = "1" (Initial value)

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2-4. LED current setting with DC and PWM dimming

2nd step : LED current dimming settings

Dimming function can be set by internal register setting. (Way of dimming, resolution)

Can choice PWM or DC dimming which are required by system requirement.

Dimming function specification

- ✓ Individual 24ch DC and PWM dimming supported
- ✓ Current output PWM Dimming : 8bit *1
- ✓ Current output DC Dimming : 8bit *1
- ✓ LED abnormal detection Function : Open/Short

*1 : DIMMODE="0" : PWM, DIMMODE ="1" : DC

LED current dimming formula

In case of using the EXTISET1 pin

$$I_{LEDn} = \frac{(DIMSETx[7:0]+1)}{256} \times \left(\frac{V_{EXTISET1}}{R_{EXTISET1}} \times 12000\right) \text{ [A]}$$

where:
$DIMSETx[7:0]$ is the decimal number of DIMSETx[7:0].
$V_{EXTISET1}$ is the EXTISET1 pin voltage, 600 mV (Typ).
$R_{EXTISET1}$ is the Resitor for connecting the EXTISET1 pin.

DIMSET Register

Table 44. DIMSET Register

DIMMODE	PWMOUTEN[0]	DIMSET01[7:0]	PWM Duty	DC current
0	0	0x00h to 0xFFh	0.0 %	DCDIM01[3:0] register setting
	1	0x00h	0.4 %	
		0x01h	0.8 %	
		0x02h	1.2 %	
		0x03h	1.6 %	
		-	-	
		xx	(xx + 1) / 256	
		-	-	
		0xFEh	99.6 %	
		0xFFh	Normally set to High (Duty 100 %)	
1	0	0x00h to 0xFFh	0 %	0.23 mA
	1	0x00h	100 %	0.23 mA
		0x01h		0.47 mA
		0x02h		0.70 mA
		0x03h		0.94 mA
		-		-
		xx		(xx + 1) / 256 x 60 mA
		-		-
		0xFEh		59.77 mA
		0xFFh		60.00 mA

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3-1. BD18330EFV-M external buck controller setting

3rd step : Setting external components value

ROHM can provide design calculation sheet. Please contact our sales team.

BD18330EFV adjusts its buck controller output voltage according to the forward voltage of the LED used in the design.

For MOSFET, Diode, inductor and capacitor selection and calculation,

please refer to the “BD18330EFV_design_support_sheet” document provided separately.

❑ BD18330EFV_design_support_sheet.xlsx

BD18330EFV-M Parts Setting Sheet

*Fomula does not include internal delay.

Legend

Input cell	→To be filled in condition
Output cell	→Calculated result
Predetermined values cell	→Predetermined values
Blank cell	→No input required

Step 1 : Input the set target value

Condition	min	Typ	Max	unit/Address	Input Range min	Input Range max
VIN	9	13.5	18	V	4.5	40
ILED	-	45	-	mA	0.1	60
CH	-	72	-			
total LED Vf	3	3.2	3.5	V	0	30
Frequency	376	400	424	kHz		
PWMDTYx	-	255	-	Address 0x33 to 0x4A	0	255
DCDIMxx	-	15	-	Address 0x24 to 0x2F	0	15

Step 2 : Check the result

Parameter	Typ	unit
REXTSET1	160	kohm

Step 3 : Select and input the value referring to Step 2

Parameter	min	Typ	Max	unit/Address		
REXTSET1	158.4	160	161.6	kohm		
Tolerance of REXTSET1	-	1	-	%		
LLSDAC[1:0]	-	1	-	Address 0x17	0	3
DC/DC low level refence Voltage	-	1.0	-	V	0.6	1.2
Inductor	-	4.7	-	µH		

- Calculate these values

①REXTISET
②Inductor
③RSNS
④Output Capacitor
⑤External MOSFET Ron
⑥OVD setting

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4-1-1. Minimum LED Output PIN Voltage

4th step : LED terminal voltage & Thermal design

Deriving available numbers of series LEDs per channel and index for heat deconcentration

LED terminal voltage requirement

1. **0.4V ＜ VLED pin voltage ＜ LED short detection** * 0.4V need for LED open detection (Including transient voltage drop)
2. **ILED ≦ 125mA pin voltage : Ron x ILED (Including transient voltage drop)**

*Worst case is in maximum Ron.

LED Pin ON Resistance	R_{LED1}	-	-	6.5	Ω	Tj = 25 °C,
	R_{LED2}	-	-	9.5	Ω	Tj = -40 °C to +150 °C,

Thermal design

- **Thermal resistance**

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 4)	2s2p(Note 5)	
HTSSOP-B54				
Junction to Ambient	θ_{JA}	59.10	26.10	℃/W
Junction to Top Characterization Parameter(Note 3)	Ψ_{JT}	8.00	7.00	℃/W

(Note 2) Based on JESD51-2A (Still-Air), using a BD18330EFV-M Chip.
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-7.

4-1-2. Minimum LED Output PIN Voltage

4th step : Estimate LED terminal voltage requirement

LED terminal voltage potential must be within below conditions for stable operation.

LED terminal voltage requirement

1. **0.4V ＜ VLED pin voltage ＜ LED short detection (Including transient voltage drop)**

   ・Maximum LEDOPEN Detection Voltage = 0.4V

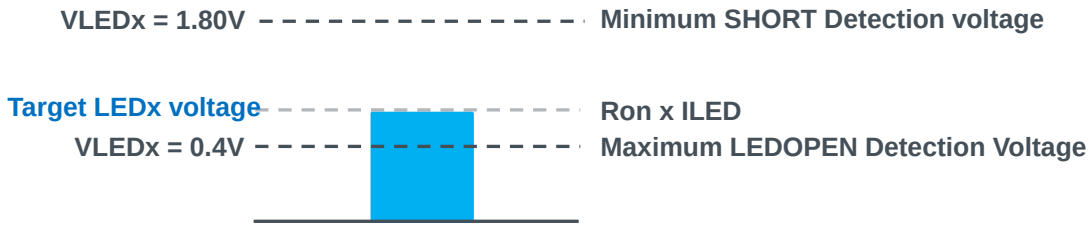
   ・Minimum SHORT Detection voltage = 1.80V *LEDSH=0x21h

2. **ILED ≦ 125mA pin voltage : Ron x ILED (Including transient voltage drop)**

*Worst case is in maximum Ron.

SHORT Detection Voltage	V_{LEDSH}	1.8	2.0	2.2	V	V_{LEDn} rising detect threshold (n = 1 to 24) LEDSHx[7:0] = 0x21h (x = 01 to 24)

LED Pin ON Resistance	R_{LED1}	-	-	6.5	Ω	Tj = 25 °C,
	R_{LED2}	-	-	9.5	Ω	Tj = -40 °C to +150 °C,



4-1-3. Minimum LED Output PIN Voltage

4th step : Estimate LED terminal voltage requirement

LED terminal voltage requirement example

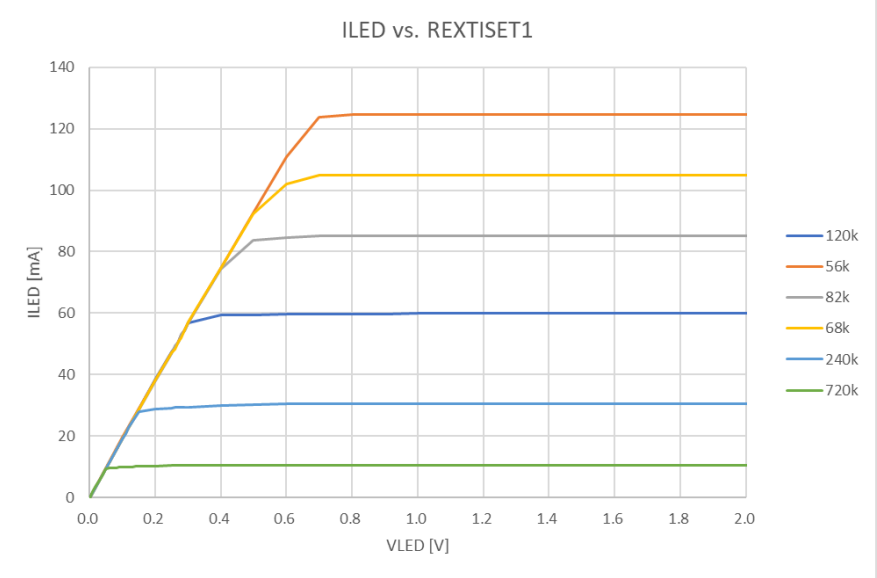
VLEDx = 0.6V : ILED ≦ 60mA

VLEDx = 0.8V : 60mA < ILED ≦ 80mA

VLEDx = 1.0V : 80mA < ILED ≦ 100mA

VLEDx = 1.2V : 100mA < ILED ≦ 125mA

Reference data : Minimum LED terminal voltage



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4-2. Calculate heat dissipation

5th step : Estimate heat dissipation example

Total power dissipation is estimated by Numbers of channels, LED anode voltage, LED current and LED forward voltage (Vf)

LED terminal voltage is calculated LED forward voltage and LED anode voltage. Design parameters are numbers of channels, LED anode voltage, LED current and LED forward voltage.

ROHM can provide the thermal calculation sheet. Please contact our sales team.

						Input		
						VMLD mini(Typ)(V)	3.6	VMLD
						Vf 35mA(Min)(V)	3	at 25C
						Vf 125mA(Min)(V)	0	at 25C
						Resister(ohm)(Typ)	0	Typ
						Resister(ohm)(Typ)	0	Typ
U2			Input	25C			Output	
Terminal	LED	current(A)	VMLD mini(Max)(V)	Vf(Min)(V)	Resister(ohm)(Typ)	Wiring parastic resister(Ohm)(Typ)	VLED terminal(V)	Heat dissipation(W)
OUT1	LED1	0.045	3.6	3	0	0	0.6	0.027
OUT2	LED2	0.045	3.6	3	0	0	0.6	0.027
OUT3	LED3	0.045	3.6	3	0	0	0.6	0.027
OUT4	LED4	0.045	3.6	3	0	0	0.6	0.027
OUT5	LED5	0.045	3.6	3	0	0	0.6	0.027
OUT6	LED6	0.045	3.6	3	0	0	0.6	0.027
OUT7	LED7	0.045	3.6	3	0	0	0.6	0.027
OUT8	LED8	0.045	3.6	3	0	0	0.6	0.027
OUT9	LED9	0.045	3.6	3	0	0	0.6	0.027
OUT10	LED10	0.045	3.6	3	0	0	0.6	0.027
OUT11	LED11	0.045	3.6	3	0	0	0.6	0.027
OUT12	LED12	0.045	3.6	3	0	0	0.6	0.027
OUT13	LED13	0.045	3.6	3	0	0	0.6	0.027
OUT14	LED14	0.045	3.6	3	0	0	0.6	0.027
OUT15	LED15	0.045	3.6	3	0	0	0.6	0.027
OUT16	LED16	0.045	3.6	3	0	0	0.6	0.027
OUT17	LED17	0.045	3.6	3	0	0	0.6	0.027
OUT18	LED18	0.045	3.6	3	0	0	0.6	0.027
OUT19	LED19	0.045	3.6	3	0	0	0.6	0.027
OUT20	LED20	0.045	3.6	3	0	0	0.6	0.027
OUT21	LED21	0.045	3.6	3	0	0	0.6	0.027
OUT22	LED22	0.045	3.6	3	0	0	0.6	0.027
OUT23	LED23	0.045	3.6	3	0	0	0.6	0.027
OUT24	LED24	0.045	3.6	3	0	0	0.6	0.027
								0.648

	Thermal resistance(C/W)
2S2P	26.1

	DegC
Ta	85
Tj U2	102

***Please ask about excel sheet**

Tj calculation example

Ta = 85deg, VLED = 2.0V, delta Target Tj < 125deg

$$TjMAX = Ta + 24ch * VFB * \mathrm{ILED} * \theta\mathrm{ja} = 85 + 24 * 0.6 * 0.045 * 26.1 = 101.9\mathrm{deg} < 125\mathrm{deg}$$

*LSSDAC[1:0] = 0x02 =V_{FB} = 0.6V

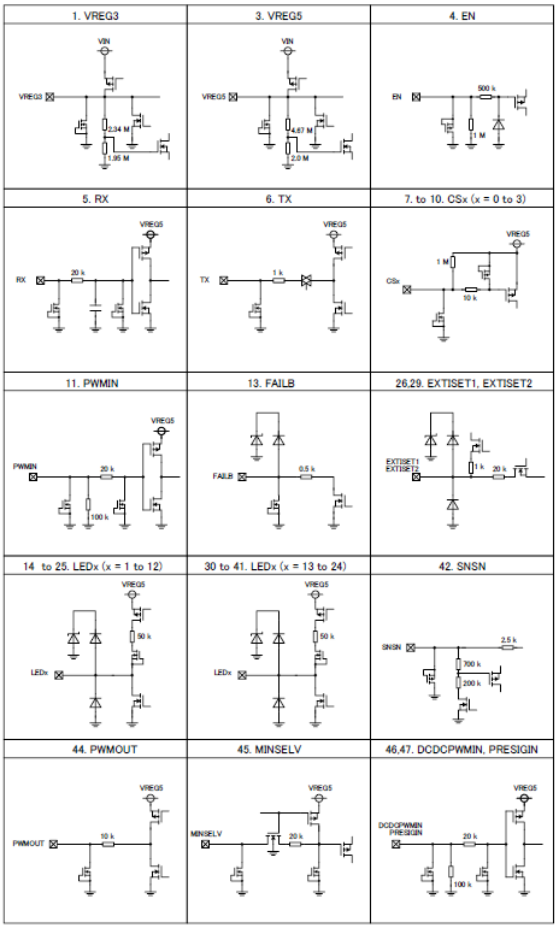
4-3. Pinout connections

6th step : Recommendation physical terminal connection

Recommended pin connections for stable operation . Do not use VREG5 for CAN transceiver power supply.

Terminal	Function	Recommendation	Note
VIN	Power	Populate Cap	Recommend short wiring of Cap
EN	Enable	Can connect to VIN	-
VREG3	Internal power	Not populate Cap.	No need external Cap on VREG3
VREG5	Internal power	Populate Cap.	Recommend short wiring of Cap Typ. = 4.7uF Do not use as power supply for CAN Tr
RX	RX	Populate Cap for EMC	Input terminal
TX	TX	Populate Cap for EMC	Output terminal
PWMIN	Sync PWM	Can be left open if not used	Recommend to use PWMSYNC function
FAILB	Diagnostic	Pull-up external supply or VREG5	Recommend pull-up to external power for daisy chain
EXTISET1,2	LED current setting	Connect resistors	Open EXTISET2 operates Zero LED current in LIMPHOME
LEDx	LED terminal	Populate Cap for EMC	Recommend populate Cap for EMC (1000pF/1005) Recommend short wiring of Cap
PWMOUT	Sync PWM	Can be left open if not used	Recommend to use PWMSYNC function
CSx	Chip select	Can be left open if not used	Invert operation. Open will be “L” Pull-down to GND will be “H”

・I/O Equivalence circuit



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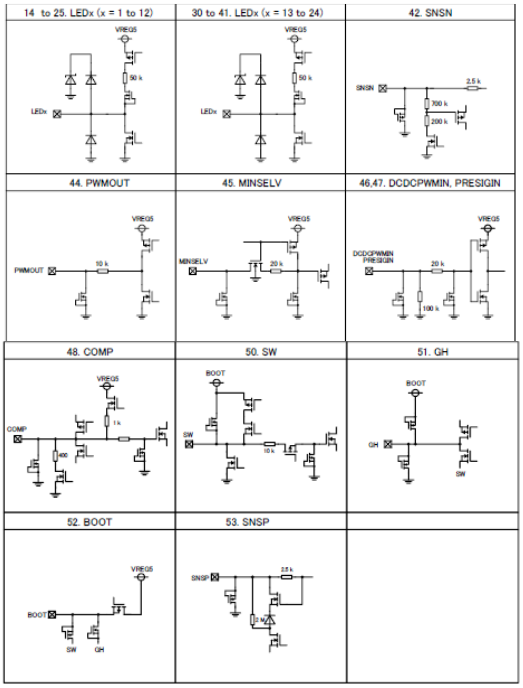
4-3. Pinout connections

6th step : Recommendation physical terminal connection

Terminal	Function	Recommendation	Note
SNSN	Output current sense N pin	Connect VOUT of DC/DC convertor	Avoid active line in parallel
MINSELV	LED pins minimum voltage select input pin	Connect MINSELOUT of BD18332EUV	Avoid active line in parallel
DCDCPWMIN	DCDCPWM operation signal input pin	Connect DCDCPWMOUT of BD18332EUV	-
PRESIGIN	Pre FB setting signal input pin	Connect PRESIGOUT of BD18332EUV	Avoid active line in parallel
COMP	Erramp output pin	Connect RC network	As possible as close to device
SW	External high side FET source pin	Connect FET,SBD,L and CBOOT	As possible as short connection
GH	External high side FET gate control pin	Connect FET gate	As possible as short connection
Boot	External high side FET driver supply pin	Connect CBOOT	As possible as close to device
SNSP	Output current sense P pin	Connect L and RSENS	Avoid active line in parallel

・I/O Equivalence circuit



5-1-1. PWM synchronization setting

7th step : PWM synchronization function setting

1. **Start-up Sequence**

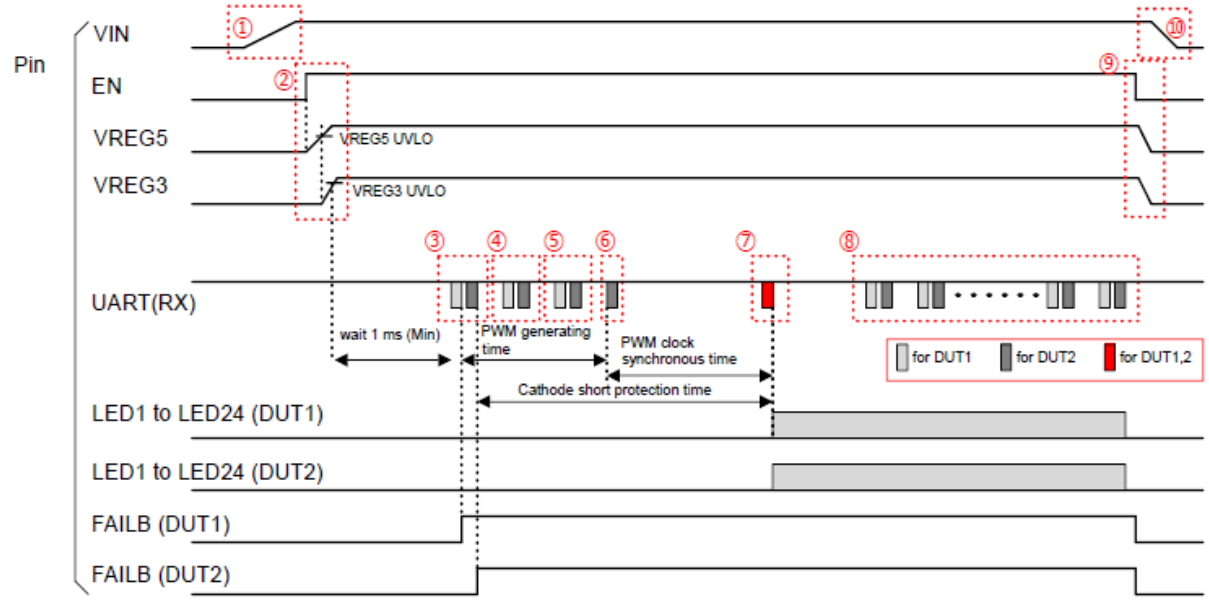


Figure 90. Starting Sequence for Normal Operation

When you light the LED by general UART control, please follow the below sequence.

① Input power supply in the VIN pin.
② Launch the EN pin from "Low" to "High", the VREG5 and VREG3 pins are generated.
③ Write initial setting from address 0x01h to 0x17h.
Write ERRCLR, to release FAILB. If you write CATHEN, it starts to operate cathode short error.
④ Write initial setting from address 0x18h to 0x2Fh.
⑤ Write initial setting from address 0x30h to 0x4Ah.
⑥ Write SYNCSET register to 10b.
⑦ All device starts dimming at same timing.
⑧ Operate dimming control for each channel.
⑨ Dimming is stopped.
⑩ Stop input power supply in the VIN pin.

- **Sync. Timing is synchronized by internal clock**
- **All devices dim after internal sync. Time**
- **PWMIN and PWMOUT function are able to adjust more sync. timing.**

5-1-2. PWM synchronization setting

7th step : PWM synchronization function setting

Recommend to use PWM sync. function for Animation Lamp

To reduce noise of power supply by PWM sync. function

- ✓ Primary PWMOUT connects to Secondary PWMIN
- ✓ Secondary PWMOUT connects to tertiary PWMIN
- ✓ PWMFREQ[1:0] register is set by address 0x17
- ✓ Initial frequency 488Hz. (0x0)
- ✓ Recommend to set 488Hz.

7. PWM Synchronization for Each Device

This feature allows the BD18330EFV-M to synchronize its internal clock with Leader device. SYNCSET register can set this IC as Leader or Follower. As Leader device (BD18330EFV-M), it generates 488 Hz (Typ) reference signal (Duty = 50 %) in PWMOUT that other Follower devices (BD18332EUV-M) use to adjust internal clock. As Follower device, it enables PWMIN input to receive the reference signal to adjust internal clock and LED output timing.

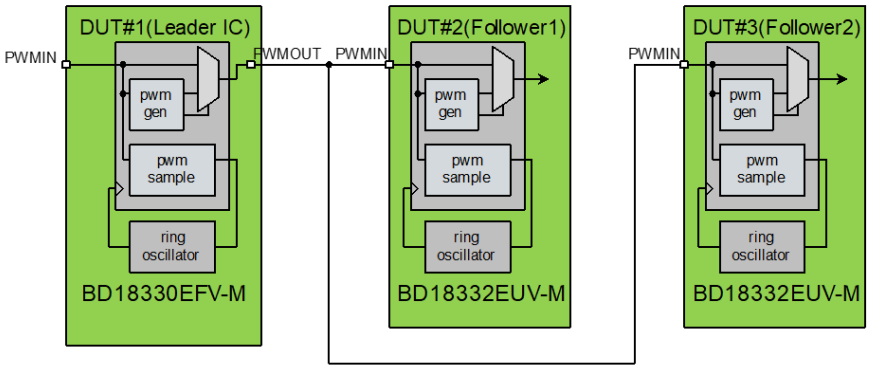


Figure 10. PWM Synchronization Setting

Address 0x17h: DENVOLT DEN Threshold voltage setting register [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LLSDAC[1:0]		PWMFREQ[1:0]		DENVOLT[3:0]			
Initial value	0	0	0	0	0	0	0	0

Update: immediately

These data in register are updated to the newest data immediately when the new data is written.

bit[7:0] LLSDAC[1:0]
DCDC Low level reference selector for feedback voltage

Table 39. LLSDAC Register

LLSDAC[1:0]	DCDC Low level Refence Voltage [V]
0x0h	1.2
0x1h	1.0
0x2h	0.8
0x3h	0.6

bit[5:4] PWMFREQ[1:0]
This register setting determines the LED output frequency.
This setting is also applicable to PWMTIM.

Table 40. PWM Frequency Setting

PWMFREQ[1:0]	LED PWM Dimming Frequency(Note 1)
0x0h	488 Hz (Typ)
0x1h	976 Hz (Typ)
0x2h	1952 Hz (Typ)
0x3h	3904 Hz (Typ)

(Note 1) The frequency indicated above is based on 18 MHz (Typ) system clock. It may vary depending on internal clock frequency.

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5-2. Diagnostic Enable VIN Voltage setting

7th step : Condition for enable diagnostics

VIN operating voltage for LED open detection and LED short protection

Set DENVOLT[3:0] according to VIN voltage to be able to detect VLEDOP and VLEDSH

1. $V_{IN\_DEN} < V_{IN}$
2. V_{IN_DEN} voltage setting must satisfy above equation

*V_{LEDx} : LEDx pin voltage
*V_{LEDOP} : LED open detect voltage, 0.3V (Typ.)
*V_{LEDSH} : LED short detect voltage, 2.0V (Typ., LEDSH=0x21h)
*V_{IN_DEN} : Diagnosis Enable VIN voltage 7.0V (Typ., DEN=0x07h)

Setting for DENVOLT[3:0] register

[LED Abnormal Detection Block]						
LEDOPEN Detection Voltage	V_{LEDOP}	0.2	0.3	0.4	V	V_{LEDn} falling detect threshold (n = 1 to 24)
SHORT Detection Voltage	V_{LEDSH}	1.8	2.0	2.2	V	V_{LEDn} rising detect threshold (n = 1 to 24) LEDSHx[7:0] = 0x21h (x = 01 to 24)
Diagnosis Enable VIN Voltage	V_{IN_DEN}	6.3	7.0	7.7	V	DENVOLT[3:0] = 0x7h

Address 0x17h: DENVOLT DEN Threshold voltage setting register [Read/Write] initial value 0x00h

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	RESERVED		PWMFREQ[1:0]		DENVOLT[3:0]			
Initial value	0	0	0	0	0	0	0	0

Update: immediately

Table 41. DENVOLT Register

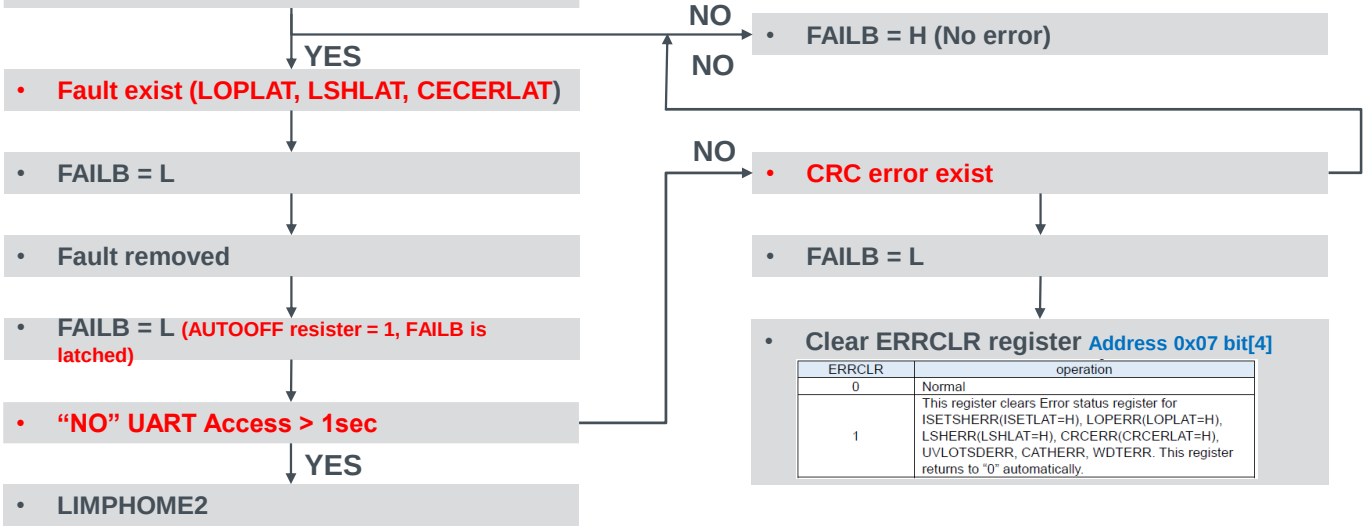
DENVOLT[3:0]	V_{IN_DEN} detection voltage [V]
0x0h	4.5
0x1h	
0x2h	
0x3h	
0x4h	
0x5h	5.0
0x6h	6.0
0x7h	7.0
0x8h	8.0
0x9h	9.0
0xAh	10.0
0xBh	11.0
0xCh	12.0
0xDh	13.0
0xEh	14.0
0xFh	15.0

5-3. AUTOOFF Function Detail

7th step : Descriptions of AUTOOFF function

- ❑ AUTOOFF register = "1" Address 0x07 bit[7]
- ❑ FAILB = H (No error)

AUTOOFF	operation
0	Normal
1	Target channel is disabled automatically when "LED open error" or "LED short error" is detected



ERRCLR	operation
0	Normal
1	This register clears Error status register for ISETSHERR(ISETLAT=H), LOPERR(LOPLAT=H), LSHERR(LSHLAT=H), CRCERR(CRCERLAT=H), UVLOTSDERR, CATHERR, WDTERR. This register returns to "0" automatically.

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5-4-1. Register setting for Buck controller

8th step : Constant pulse mode for light load

Recommend to use DCDCSLSW function for animation lamp

To prevent from pulse skip in light load condition

- ✓ **Setting for BD18330EFV-M**
- ✓ **Select Synchronous mode (DCDCSLSW="1") to stabilize the switching freq. during light load condition in animation lamp operation.**

Address 0x00h: SYNC **Setting of PWM phase synchronized for all device[Write]** **initial value 0x00h**

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	DCDCSLSW	PWMTIM	ISETSEL	SLOPEEN	DIMMODE	PWMPSYNC	DIMSTART	SWRST
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

bit[7] DCDCSLSW
This register is control the DCDC operation mode.
Please set this register in initial setting.

Table 5. DCDCSLSW Setting

DCDCSLSW	DCDC operation
0	Diode Rectification Mode
1	Synchronous Rectification Mode

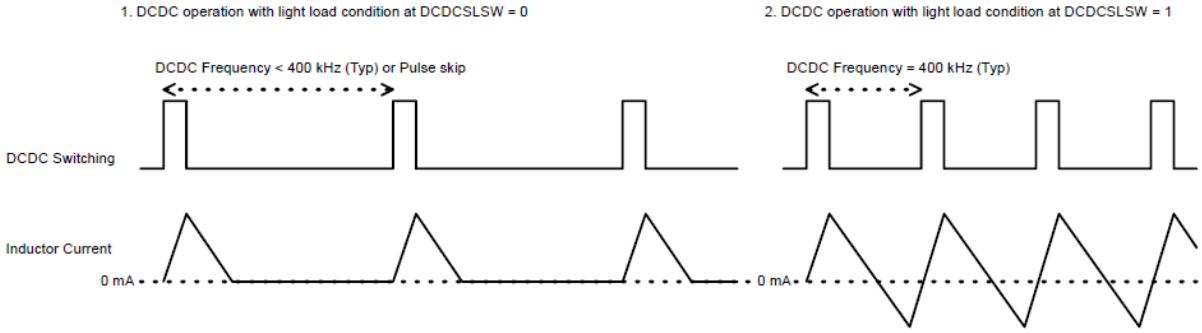

Figure 37. DCDCSLSW Function at light load condition

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5-4-2. Register setting for Buck controller

8th step : Setting register for Spread Spectrum Clock Generation function

SSCG can reduce EMI noise

To prevent concern from EMI noise

- ✓ **Setting for BD18330EFV-M**
- ✓ **SSFM[2:0] to set sweep frequency and modulation rate (SSCG OFF to 366.2Hz).**

●Address 0x01: SYSSET1 system setting1 [Read / Write] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	FAILBCNT	FAILBEN	SSFM[2:0]			PWMFSYNC	SYNCSET[1:0]	
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

bit[5:3] SSFM
This register controls SSCG ON/OFF for DC/DC.

Table 14. SSFM setting

SSFM	CLK_SSM	SSCG modulation ratio
0	SSCG OFF (Fixed frequency of DC/DC)	
1	15.625Khz	122.1Hz
2	17.578Khz	137.3Hz
3	20.089Khz	156.9Hz
4	23.438Khz	183.1Hz
5	28.125Khz	219.7Hz
6	35.156Khz	274.7Hz
7	46.875Khz	366.2Hz

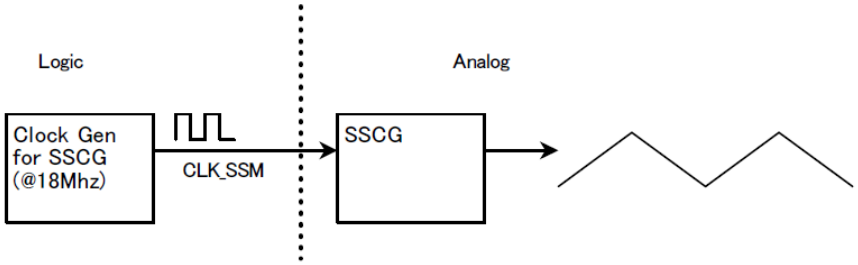

Figure 33. SSCG Structure

(Unless otherwise specified: V_{IN} = 13 V, Tj = -40 °C to +150 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Spread Spectrum Frequency	f_{RAMP}	103.2	122.1	140.9	Hz	
Spread Spectrum Width	W_{SPREAD}	8	9	10	%	

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5-4-3. Register setting for Buck controller

8th step : OVDVOLT & PREBOOST setting

PREBOOST function prevents LED flickering from load

- ✓ **Setting for BD18330EFV-M**
- ✓ **Function to prevent the potential flickering during PWM / DC dimming.**
- ✓ **Set and increase SNSN pin voltage before LED turn on.**
- ✓ **PREBOOST[3:0] to set PREBOOST time.**
- ✓ **OVDVOLT[3:0] to set the voltage at SNSN pin and Over Voltage detection threshold during PREBOOST period. Refer 5-4-5.Register setting for Buck controller.**

Setting register

●Address 0x02: SYSSET2 system setting2 [Read / Write] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	OVDVOLT[3:0]				PREBOOST [3:0]			
Initial value	0	0	0	0	0	0	0	0

Update: immediately

5-4-4. Register setting for Buck controller

8th step : SSMASK time setting

- ✓ **Setting for BD18330EFV-M**
- ✓ **Setting for Protection detection mask time during the soft start time of Buck converter.**
- ✓ **LED open protection and LED short protection will be detected after SSMASK time.**

Setting register

●Address 0x03: SYSSET3 system setting3 [Read / Write] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	ERRMASK[3:0]				SSMASK[3:0]			
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

Table 63. Soft Start Mask time

SSMASK[3:0]	Soft Start Mask time [ms]
0x0	-
0x1	0.68 + PREBOOST time Setting
0x2	1.37 + PREBOOST time Setting
0x3	1.82 + PREBOOST time Setting
0x4	2.50 + PREBOOST time Setting
0x5	3.19 + PREBOOST time Setting
0x6	3.87 + PREBOOST time Setting
0x7	4.32 + PREBOOST time Setting
0x8	5.01 + PREBOOST time Setting
0x9	5.69 + PREBOOST time Setting
0xA	6.14 + PREBOOST time Setting
0xB	6.83 + PREBOOST time Setting
0xC	7.51 + PREBOOST time Setting
0xD	8.19 + PREBOOST time Setting
0xE	8.65 + PREBOOST time Setting
0xF	9.33 + PREBOOST time Setting

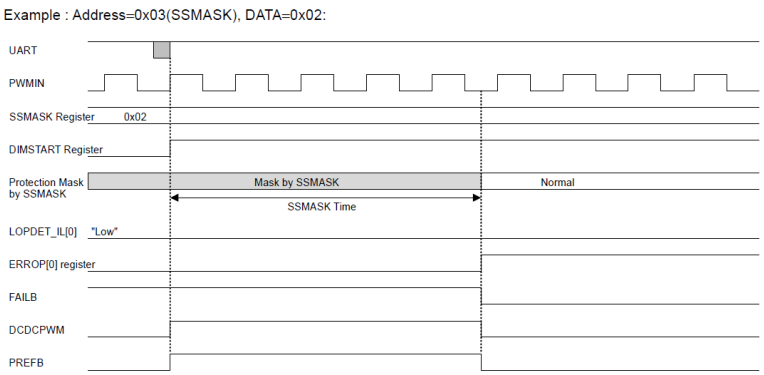

Figure 65. Setting for Soft Start Mask

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5-4-5. Register setting for Buck controller

8th step : OVDVOLT, PREBOOST & SSMASK setting

- ✓ **Setting for BD18330EFV-M**
- ✓ **Protect over voltage during PREBOOST setting time.**
- ✓ **FAILB status keeps “H” during PREBOOST setting time but protected by detecting OVDVOLT.**
- ✓ **STOP switching during detect error. Restart switching after decreasing VOUT voltage.**
- ✓ **PREBOOST voltage = OVD voltage during PREBOOST setting time.**
- ✓ **SSMASK time (ms) include PREBOOST time (µs).**

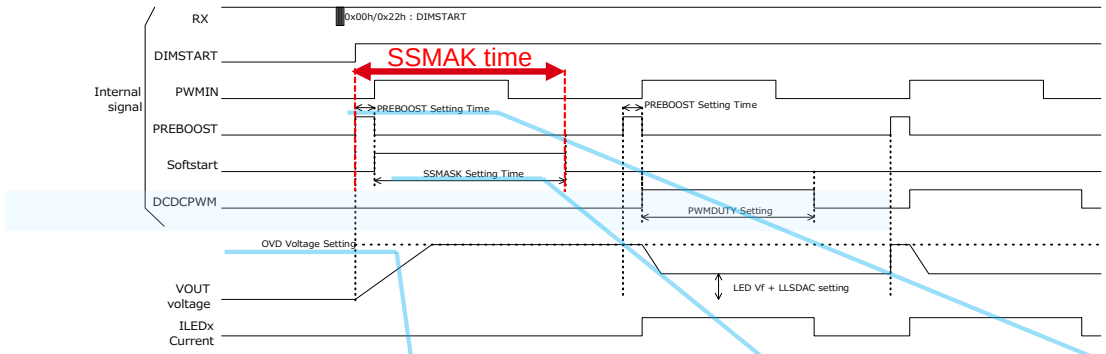

Table 17. OVDVOLT setting

bit[7:4] OVDVOLT[3:0]	Detection voltage [V]
0x0	5.0
0x1	
0x2	
0x3	
0x4	
0x5	
0x6	6.0
0x7	7.0
0x8	8.0
0x9	9.0
0xA	10.0
0xB	11.0
0xC	12.0
0xD	13.0
0xE	14.0
0xF	15.0

Table 63. Soft Start Mask time

SSMASK[3:0]	Soft Start Mask time [ms]
0x0	-
0x1	0.68 + PREBOOST time Setting
0x2	1.37 + PREBOOST time Setting
0x3	1.82 + PREBOOST time Setting
0x4	2.50 + PREBOOST time Setting
0x5	3.19 + PREBOOST time Setting
0x6	3.87 + PREBOOST time Setting
0x7	4.32 + PREBOOST time Setting
0x8	5.01 + PREBOOST time Setting
0x9	5.69 + PREBOOST time Setting
0xA	6.14 + PREBOOST time Setting
0xB	6.83 + PREBOOST time Setting
0xC	7.51 + PREBOOST time Setting
0xD	8.19 + PREBOOST time Setting
0xE	8.65 + PREBOOST time Setting
0xF	9.33 + PREBOOST time Setting

Table 18. Preboost time setting

PREBOOST[3:0]	Time [us]
0x0	8
0x1	16
0x2	24
0x3	32
0x4	40
0x5	48
0x6	56
0x7	64
0x8	72
0x9	80
0xA	88
0xB	96
0xC	104
0xD	112
0xE	120
0xF	128

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5-4-6. Register setting for Buck controller

8th step : Latch or un-Latch function for OCP

- ✓ **Setting for BD18330EFV-M**
- ✓ **External MOSFET will be turned off to prevent its damage by detecting OCP.**
- ✓ **DCDC OCP protection function normally un-latch mode.**
- ✓ **OCPEN is to set enable or disable for Over Current Protection.**
- ✓ **OCPLAT = "1", FAILB = "L", OCPERROR = "1" when by detecting OCP.**
- ✓ **Stop DCDC output by detecting OCP.**

Setting register

●Address 0x07: SYSSET4 system setting4 [Read / Write] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	ISETLAT	AUTOOFF	ERRCLR	OCPLAT	CRCERLAT	LSHLAT	LOPLAT
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

●Address 0x08: SYSSET5 ERROR output mask setting register [Read / Write] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	SWOCPEN	OCPEN	CATHEN	TSDWEN	WDTEN	LOPEN
Initial value	0	0	0	0	0	0	0	0

Update: immediately

bit[3] OCPLAT
Please set this register in initial setting.

Table 25. OCPLAT setting

OCPLAT	operation
0	Normal(auto release)
1	FAILB output (Low) and "OCP error" status register (OCPERR) are latched until writing '1' in ERRCLR register.

Error register

●Address 0x51: UVLOERR CRC and UVLO,TSD error status [Read] initial value 0x01

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	ISETSHERR	SWOCPERR	OCPERR	CATHERR	TSDW	WDTERR	CRCERR	UVLOTSDERR
Initial value	0	0	0	0	0	0	0	1

Update: -

●Address 0x07: SYSSET4 system setting4 [Read / Write] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	ISETLAT	AUTOOFF	ERRCLR	OCPLAT	CRCERLAT	LSHLAT	LOPLAT
Initial value	0	0	0	0	0	0	0	0

Update: Immediately

Table 51. OCPERR Register Setting

OCPERR	Status
0	Normal
1	Detect OCP error

Table 52. OCP Detection Setting

OCPEN	OCPLAT	Release condition
0	*	It is not available to control status and FAILB output
1	0	OCP error condition is released when protection is released
1	1	Status condition is released when "ERRCLR = 1" is set

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5-4-7. Register setting for Buck controller

8th step : Setting for External MOSFET over current protection

- ✓ **Setting for BD18330EFV-M**
- ✓ **SWOCP is Short to GND protection for SW pin terminal.**
- ✓ **SWOCP is monitoring SW pin terminal shorted to GND or not every 10ms.**
- ✓ **SWOCP operates in condition $V_{IN} – V_{SW} > 1.0V$ (Typ.).**

  ***V_{IN} : VIN pin voltage**

  ***V_{SW} : SW pin voltage**

  V_{SWOCP} : External MOSFET Over Current Protection threshold voltage
- ✓ **SWOCPEN = 1 : FAILB = L, SWOCPERR = "1" when by detecting error.**
- ✓ **SWOCP is masked depends on hiccup time specification (10ms typ.).**

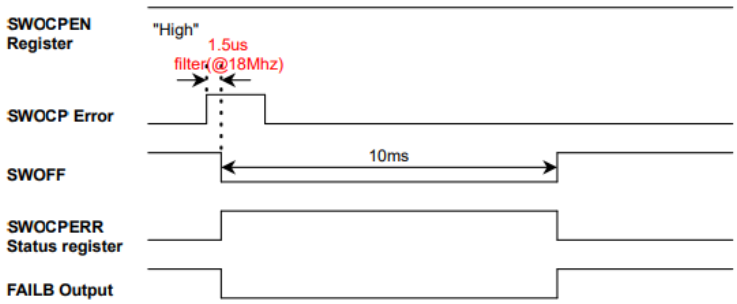

Figure 66. SWOCP Detection Protection

Setting register

●Address 0x08: SYSSET5 ERROR output mask setting register [Read / Write] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	-	-	SWOCPEN	OCPEN	CATHEN	TSDWEN	WDTEN	LOPEN
Initial value	0	0	0	0	0	0	0	0

Update: immediately

Bit[5] SWOCPEN
Please set this register in initial setting.

Table 29. SWOCPEN register

SWOCPEN	Operation
0	"SWOCP" protection is disabled.
1	"SWOCP" protection is enabled. If it detects, It controls SWOCPERR and FAILB =Low. This only affect protection detection and will not release the protection when already detected.

Error register

●Address 0x51: UVLOERR CRC and UVLO,TSD error status [Read] initial value 0x01

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	ISETSHERR	SWOCPERR	OCPERR	CATHERR	TSDW	WDTERR	CRCERR	UVLOTSDERR
Initial value	0	0	0	0	0	0	0	1

Update: -

Table 49. SWOCPERR Register Setting

SWOCPERR	Status
0	Normal
1	Detect SWOCP error

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5-4-8. Register setting for Buck controller

8th step : Provide Dedicate LED anode voltage from BD18330EFV-M

- ✓ **Setting for BD18330EFV-M**
- ✓ **Setting LLSDAC[1:0] register for DCDC low level reference voltage.**
- ✓ **VLEDFB is feedback voltage from Minimum Selector functional block.**
- ✓ **VLEDFB is reference voltage to set minimum head room voltage for LEDx terminal.**
- ✓ **Auto adjust LED Anode voltage by setting minimum headroom voltage as selected LLSDAC[1:0] register value.**

●Address 0x17: DENVOLT DEN Threshold voltage setting register [Read / Write] initial value 0x00

bit No	bit[7]	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0]
Name	LLSDAC[1:0]		PWMFREQ[1:0]		DENVOLT[3:0]			
Initial value	0	0	0	0	0	0	0	0

Update: immediately

bit[7:0] LLSDAC[1:0]
DCDC Low level reference selector for feedback voltage

Table 39. LLSDAC Register

LLSDAC[1:0]	DCDC Low level Refence Voltage [V]
0x0h	1.2
0x1h	1.0
0x2h	0.8
0x3h	0.6

Minimum required VLEDx voltage
0.6V : ILED ≦ 60mA
0.8V : 60mA < ILED ≦ 80mA
1.0V : 80mA < ILED ≦ 100mA
1.2V : 100mA < ILED ≦ 125mA

3. Buck DC/DC Controller

This IC has a built-in Buck DC/DC controller that reduces the heat generation of the IC. This controller operates so that the Lowest voltage of LED1 pin to LED24 pin voltage becomes a constant voltage. By using the hysteresis type, it is possible to respond to sudden load changes during animation. In addition, to suppress the ripple voltage of the LEDx pin voltage, a ripple injection circuit that adds information on the current flowing through the coil to the feedback voltage is built in. Built-in SSCG circuit and frequency stabilization circuit to prevent EMC noise.

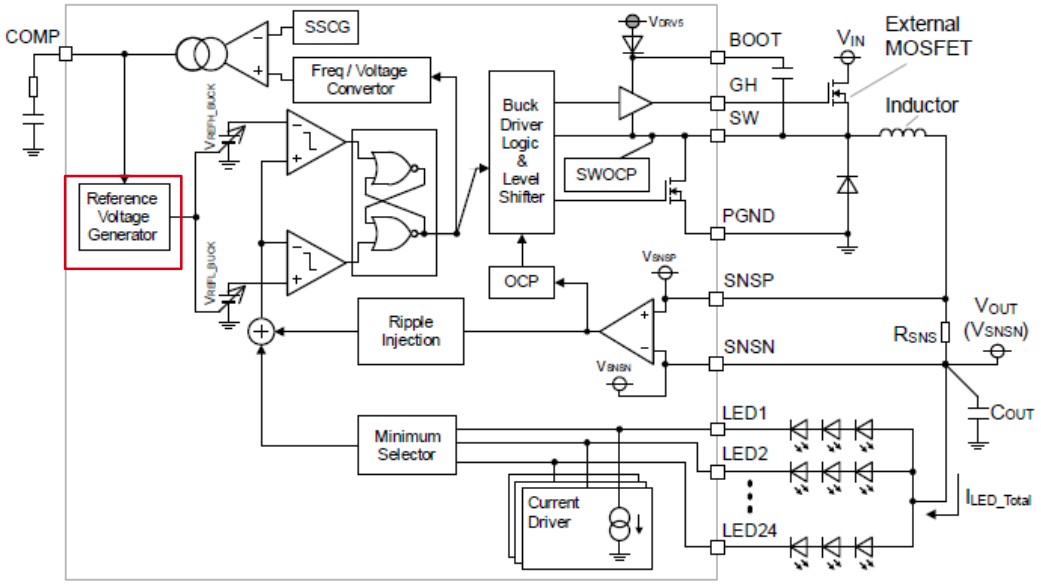

Figure 6. Buck DC/DC Controller

3.1. LEDx pin Auto Feedback type Buck DC/DC Controller

In order to minimize the power consumption of the IC, this IC controls the minimum voltage from the LED1 pin to the LED24 pin to LED Terminal Feedback Voltage (V_{LEDFB}, 1.0V (Typ)).

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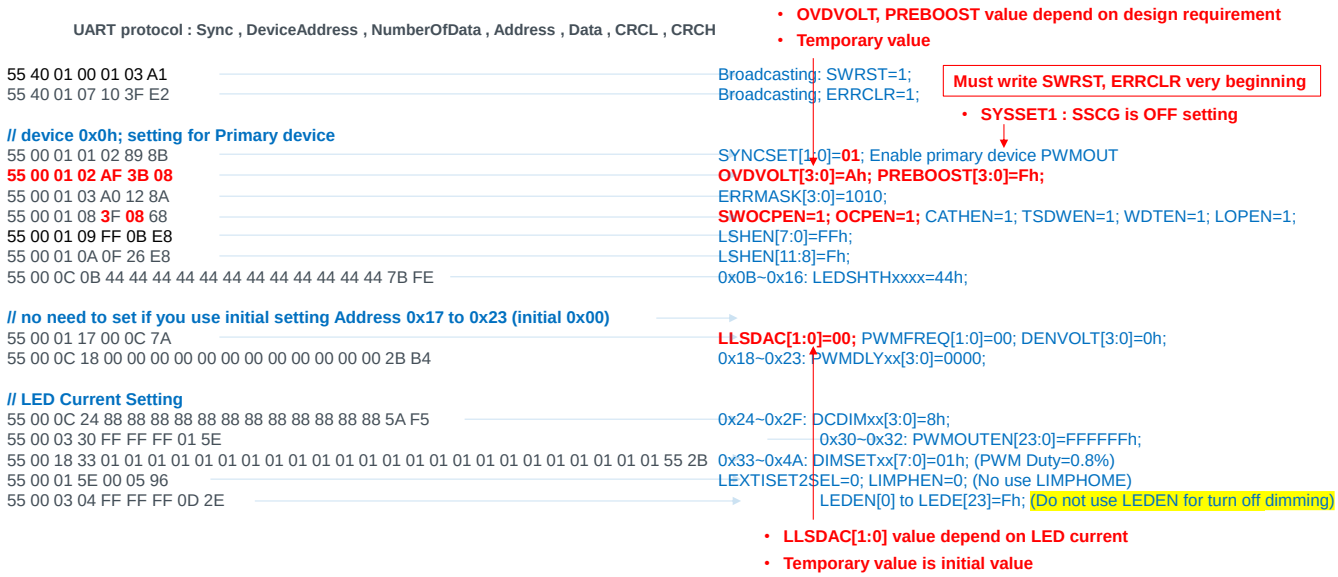
5-5-1. Reference register setting example

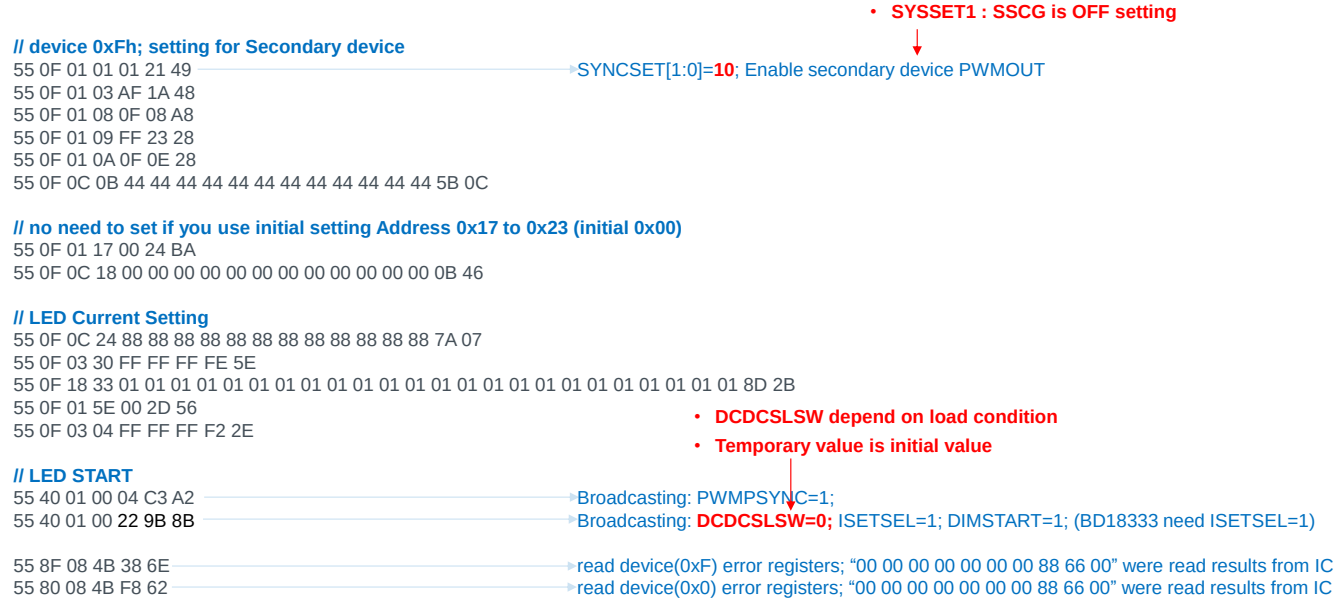
9th Step : Register setting example

UART protocol: Sync, Device Address, Number Of Data, Address, Data, CRCL, CRCH



5-5-2. Reference register setting example

9th Step : Register setting example



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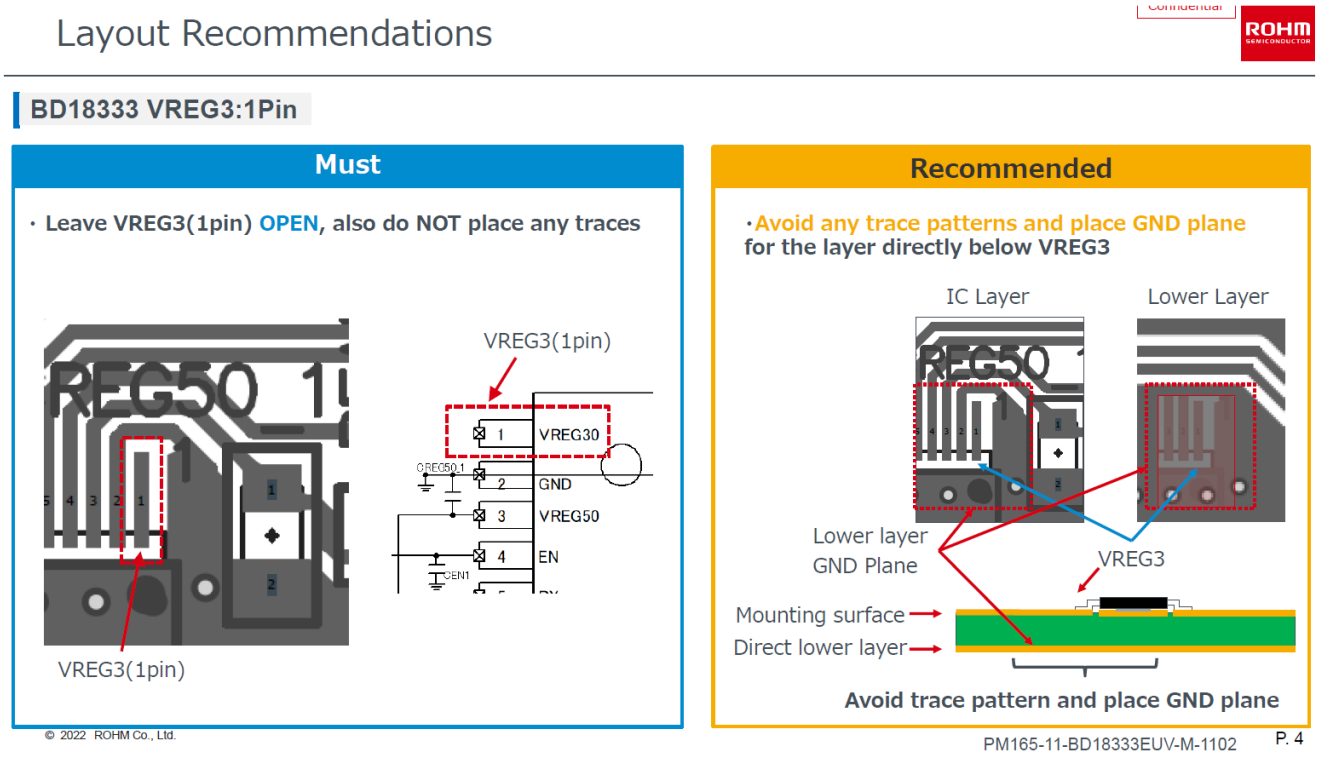
6. Reference layout guideline

10th step : Reference layout guideline example

ROHM can provide Layout guideline.

Layout guideline for EMC mitigation *Need admin. number

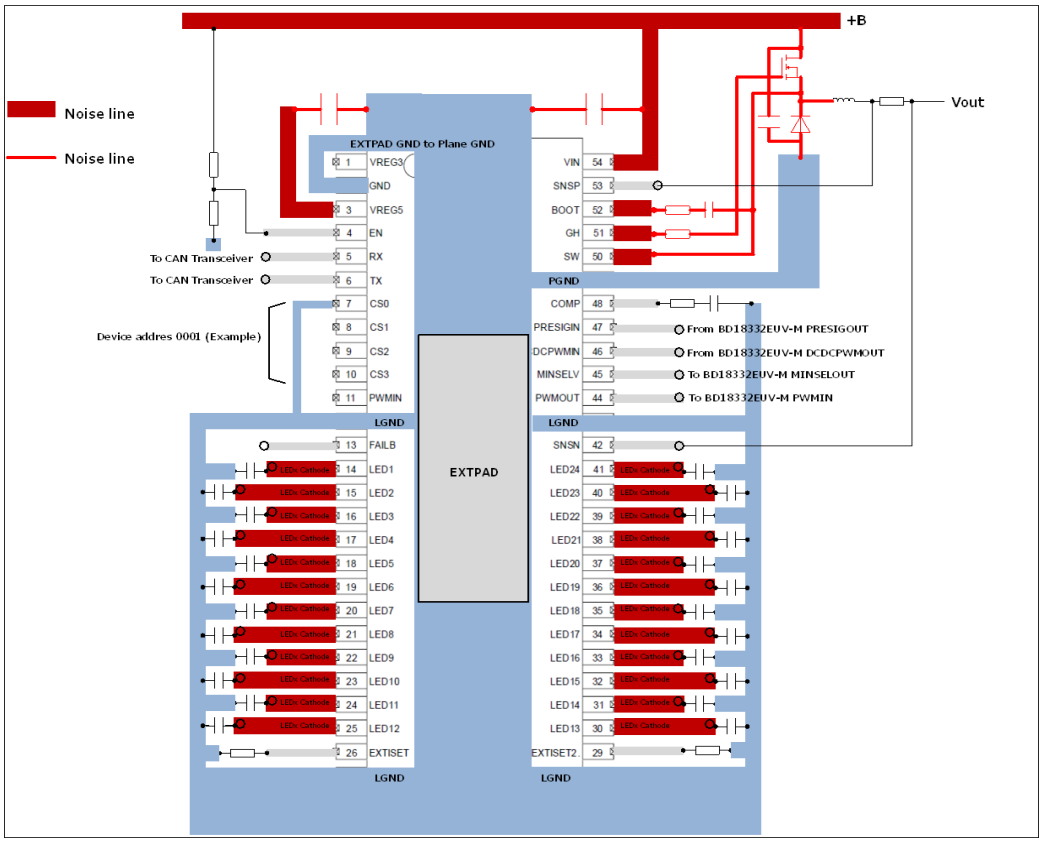
*More detailed layout guidelines are available. Please contact our sales team.



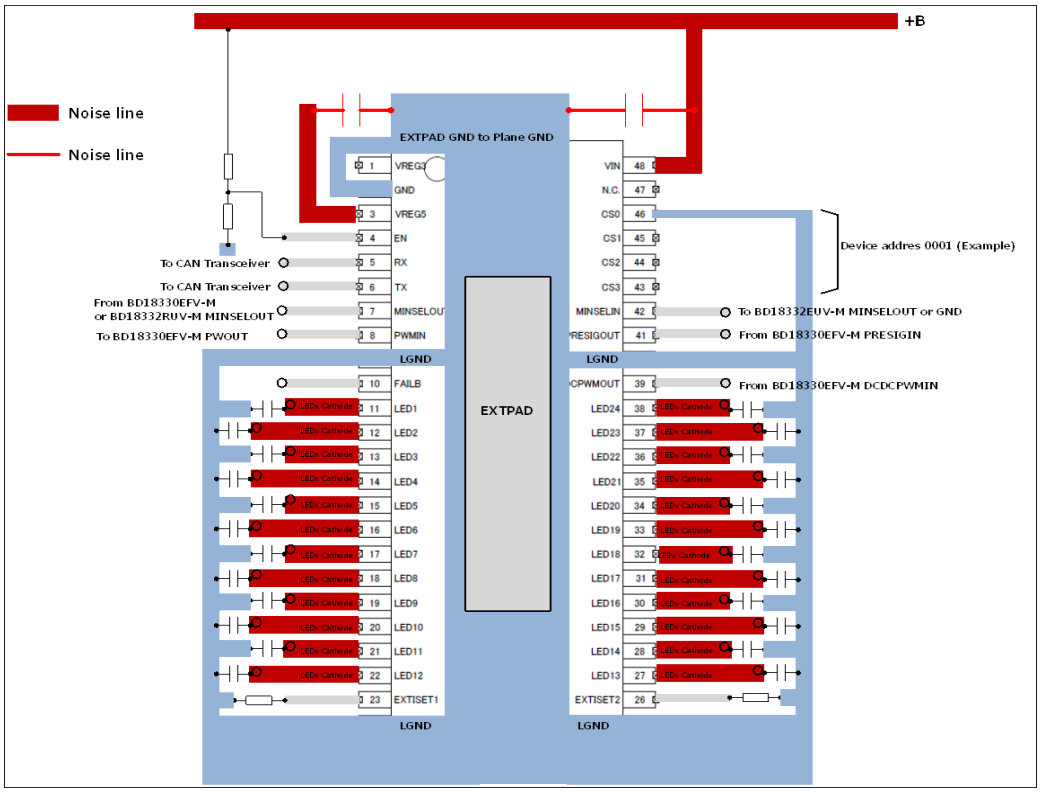
10th step : Reference layout guideline example

Here shows part of the Layout guideline.

BD18330EFV-M



BD18332EUV-M



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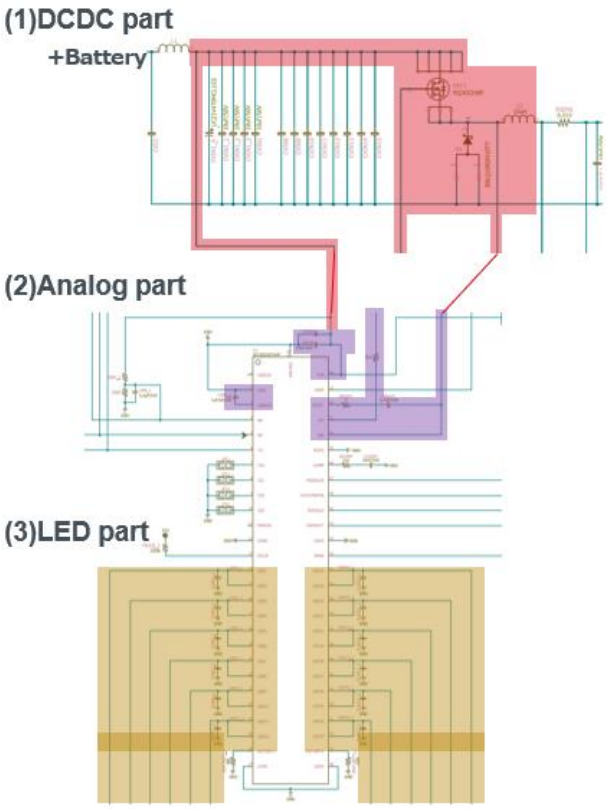
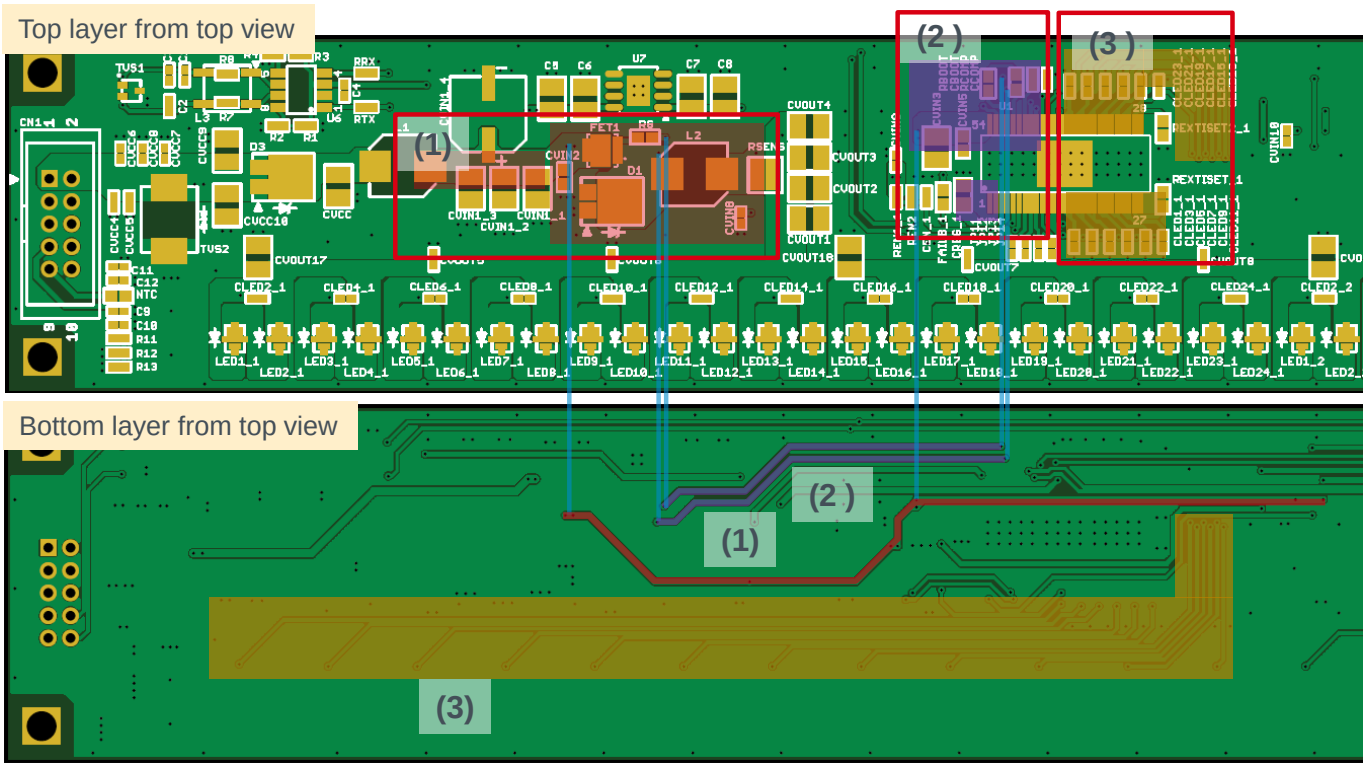
10th step : Reference layout guideline example

Noise of the BD18330EFV is generated in the following locations and is transmitted to various components and wires on the board. It is important to pay attention to component placement and wiring to reduce noise levels.





Go to flow-chart

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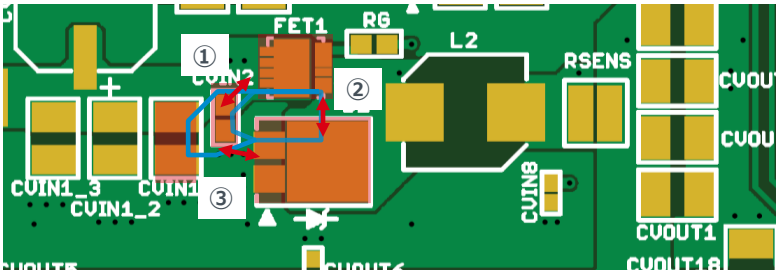
10th step : Reference layout guideline example

(1)DCDC part

1. The decoupling capacitors (CIN1, CIN2) should be placed closest to the MOSFET and the diode pins.
   Less than 15 mm, and should be as short as 1 mm.
   In addition, placing a capacitor 0.1 μF(CIN2) close to the drain of the MOSFET and the cathode of the diode results in minimizing the high-frequency noise.

2. The input capacitors, the MOSFET, the diode, the output inductor(L2), the sense resistor(RSENS) and the output capacitor should be placed on the same side of the board and the connection of each part should be made on the same layer.

Top View



①VIN side of CVIN ⇔ MOSFET Drain
②MOSFET Source ⇔ Diode Cathode
③Diode Anode ⇔ GND side of CVINあ

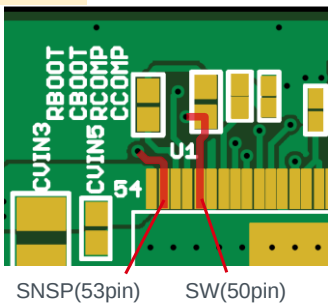
Noted: An improper layout can cause common mode noise of several 10~100 MHz.

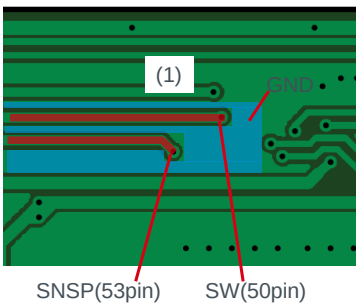
3. Recommend more than 4 layers PCB for better heat dissipation and EMC performance.

4. For 4-layer board, adjacent layer (Layer 1) to be a plane GND layer, make layer 2 to plane GND as well.
   Place the ground plane in a layer closest to the surface layer where the input capacitor, the MOSFET, the diode and the inductor(L2) are mounted.

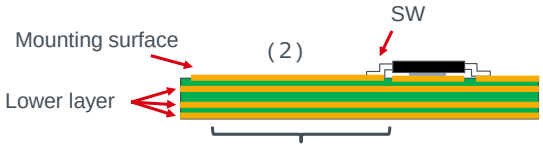
5. Insert a GND line between SW (pin 50) and SNSP (pin 53) and wire them to the switching node with no adjacent wiring.
   ・Wiring is surrounded by a GND pattern (1)
   ・Adjacent layers of wiring should be GND pattern (2)

Top View





Side View



Avoid trace pattern and place GND plane

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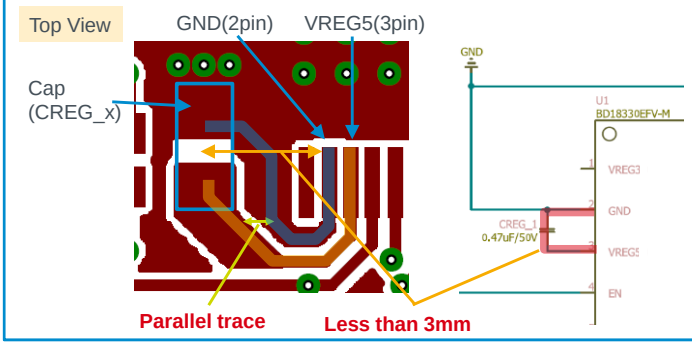
10th step : Reference layout guideline example

(2)Analog part

Must

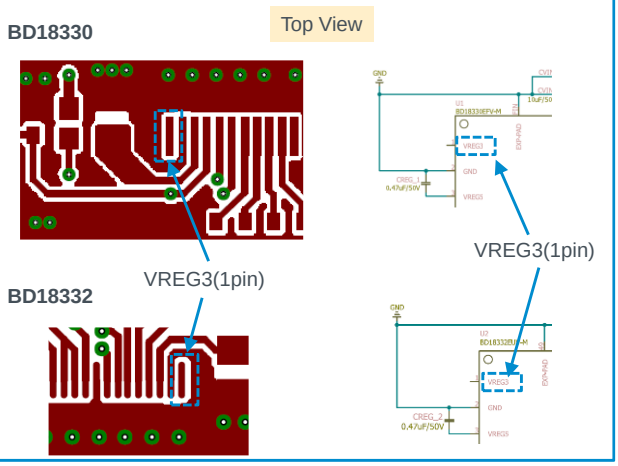
・Short trace the VREG5(3pin)-Cap(CREG_x)-GND(2pin)
・VREG5 trace pattern and GND pattern should paced on the same layer and traced in parallel

Recommend to place CREG_x on the right of IC and connect as Rohm recommended layout. Recommended estimated distance from terminal pin to capacitor edge is less than 3mm



Must

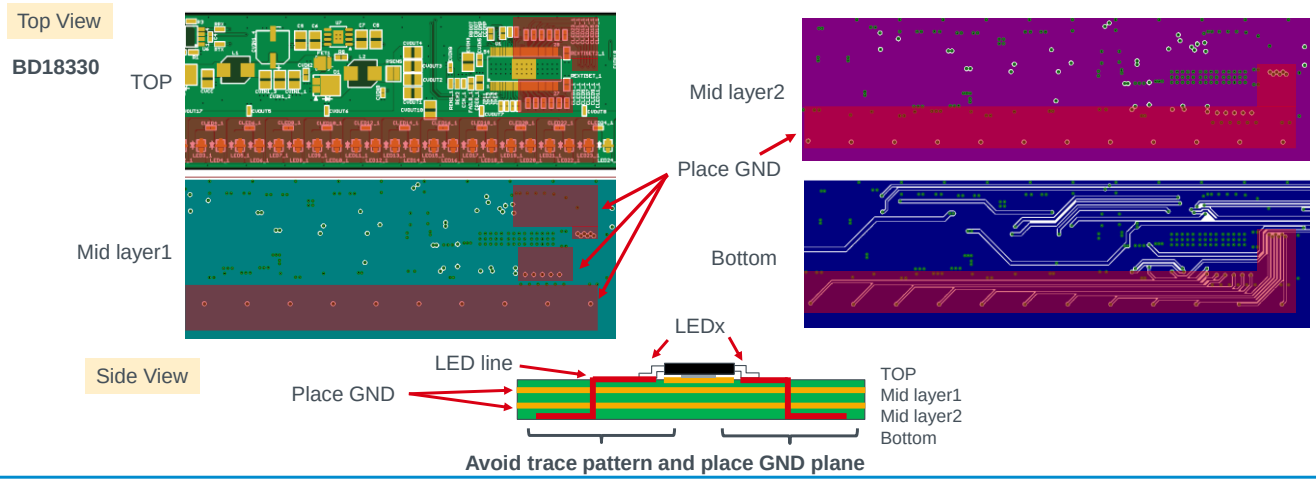
・Leave VREG3(1pin) **OPEN**, also do NOT place any traces



(3)LED part

Must

・Place GND pattern for each LED connection, lower layer of LED anode/cathode

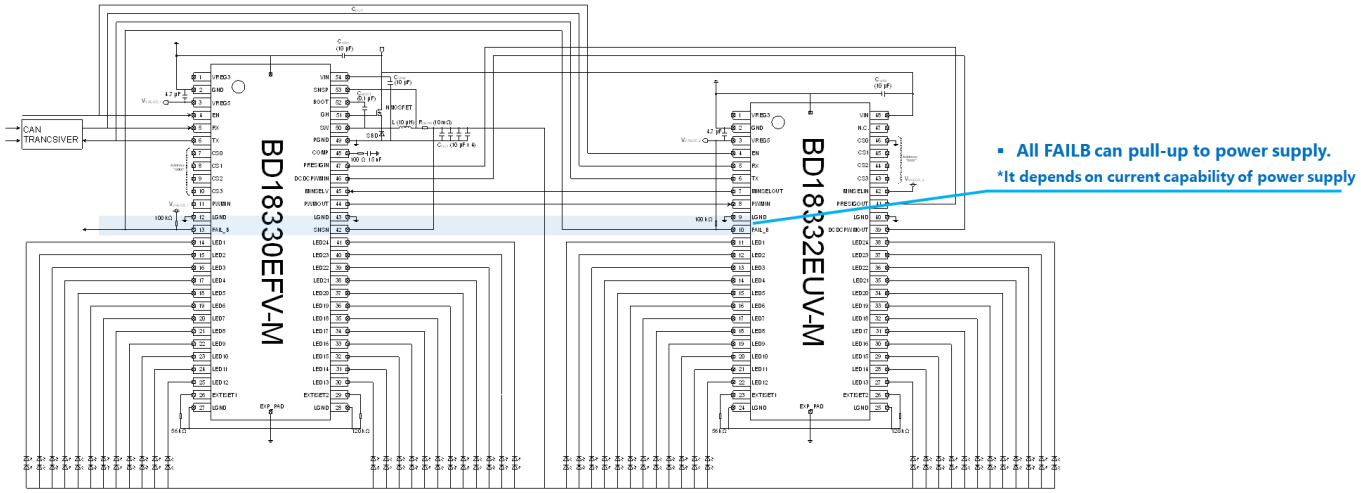


Avoid trace pattern and place GND plane

7. Pre-cautions : FAILB Pin

11th step : Pull-up all FAILB terminal to VREG5

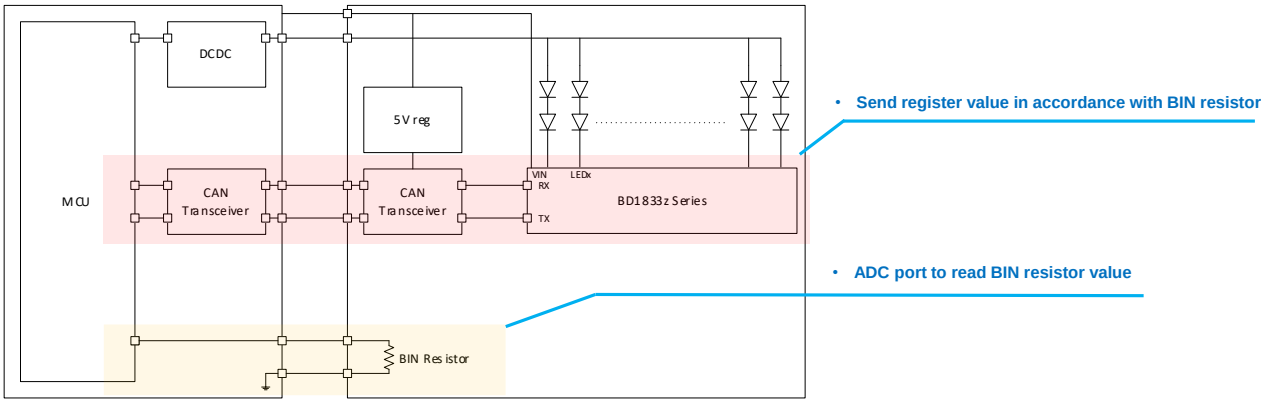
All FAILB terminals can be pull-up to power supply. *Int capability of power supply.



8. Pre-cautions : LED Binning

11th step : LED current adjustment with LED flux Bin

Example



1. To realize higher accuracy of LED current, one solution is to read populated BIN resistor value on each LED boards
2. Read resistor value by ADC port of MCU. BIN resistor is same value as $R_{EXTISET1,2}$
3. Adjust LED current setting register in accordance with BIN resistor value information

*To minimize usage of ADC port, recommend to use same ranked LEDs

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