ROHM SEMICONDUCTOR

Application Note

SPICE Modeling Report

BD18340FV-M
Constant Current Controller
For Automotive LED Lamps

In this report, the characteristics that can be confirmed by the simulation using the SPICE model of the constant current controller IC BD18340FV-M will be described.

Simulation Environment

- Circuit Simulator : PSpice / Cadence Design System, Inc.
- Version Information : 17.2-2016
- OS Information : Windows 7 Ultimate

File Information

- Library File Name : BD1834xFV.lib
- Symbol File Name : BD1834xFV.olb
- Subcircuit and Symbol

Table 1. Correspondence Table

Product Name	Subcircuit	Symbol
BD18340FV-M	BD18340FV	BD18340FV
BD18341FV-M	BD18341FV	BD18341FV

BD1834xFV SPICE MODEL

- Terminal Information

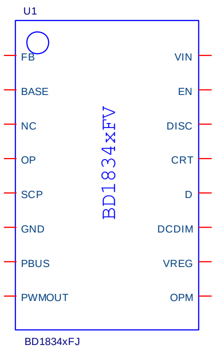

Figure 1. Symbol of BD1834xFV

Table 2. Pin Table

Pin No.	Pin Name	Pin No.	Pin Name
1	FB	9	OPM
2	BASE	10	VREG
3	NC	11	DCDIM
4	OP	12	D
5	SCP	13	CRT
6	GND	14	DISC
7	PBUS	15	EN
8	PWMOUT	16	VIN

Verifiable Characteristics

(Note 2) This model is not compatible with the influence of ambient temperature.
(Note 3) Please use the simulation results only as a design guide and the data reported herein is not a guaranteed value. Moreover, the characteristics which are not included in the report may change depending on the actual board design and ROHM strongly recommend to double check those characteristics with actual board where the chips will be mounted on.

Electrical Characteristics (vs. Datasheet)

Table 3. Electrical Characteristics Comparison

(Unless otherwise specified, V_{IN}=13V, C_{VREG}=1.0µF, Transistor PNP = 2SAR573D)

Parameter	Modeled *(Note1)*	Design Value		Unit	Error	Condition
		Datasheet	SPICE			
[Circuit Current I_{VIN}]						
Circuit Current at Stand-by Mode (I_{VIN1})	✓	0	0.0	µA	0.0%	V_{EN}=0V, V_{FB}=V_{IN}
Circuit Current at Normal Mode (I_{VIN2})	✓	2.0	1.89	mA	5.5%	V_{EN}=V_{IN}, V_{FB}=V_{IN}-1.0V **Base current subtracted**
Circuit Current at LED Open Detection (I_{VIN3})	X	2.0	1.89	mA	5.5%	V_{EN}=V_{IN}, V_{FB}=V_{IN}-1.0V, **at LED Open Detection**
Circuit Current at PBUS=Low (I_{VIN4})	X	2.0	2.19	mA	9.5%	V_{EN}=V_{IN}, V_{FB}=V_{IN}-1.0V, V_{PBUS}=0
[VREG Voltage]						
VREG Terminal Voltage (V_{REG})	✓	5.00	5.000	V	0.0%	I_{VREG}=-100µA
VREG Terminal Current Capability (I_{VREG})	X	-	32.8	mA	-	
[DRV]						
FB Terminal Voltage (V_{FBREG})	✓	650	651.8	mV	0.3%	V_{FBREG}=V_{IN}-V_{FB} R_{FB1}=R_{FB2}=1.8Ω
FB Terminal Input Current (I_{FB})	✓	15	15.0	µA	0.0%	V_{FB}=V_{IN}
BASE Terminal Sink Current Capability (I_{BASE})	X	-	37.5	mA	-	V_{FB}=V_{IN}, V_{BASE}=V_{IN}-1.5V
BASE Terminal Pull-up Resistor (R_{BASE})	✓	1.0	1.00	kΩ	0.0%	V_{CRT}=0V, V_{FB}=V_{IN} V_{BASE}=V_{IN}-1.0V
[LED Current De-rating Function (DC Diming Function)]						
DC Diming Gain (D_{DG})	✓	725	732.8	mV/V	1.1%	⊿V_{FBREG}/⊿V_{DCDIM} V_{DCDIM} : 0.75V -> 0.35V
FB Terminal Voltage V_{DCDIM}=0.75 (V_{FB_DC1})	✓	466	468.6	mV	0.6%	
FB Terminal Voltage V_{DCDIM}=0.50 (V_{FB_DC2})	✓	284	285.4	mV	0.5%	
FB Terminal Voltage V_{DCDIM}=0.35 (V_{FB_DC3})	✓	175	175.5	mV	0.3%	
[Over Voltage Mute Function(OVM)]						
Over Voltage Mute Start Voltage (V_{OVMS})	✓	22.0	22.22	V	1.0%	⊿V_{FB}=10.0mV ⊿V_{FB}= V_{FB}(@V_{IN}=13V) - V_{FB}(@V_{IN}=V_{OVM})
Over Voltage Mute Gain (V_{OVMG})	✓	-25	-25.0	mV/V	0.0%	⊿V_{FB}/⊿V_{IN}

(Note 1) ✓: Model available (supported), X: Model not available" (not supported).

(Unless otherwise specified, V_{IN}=13V, C_{VREG}=1.0µF, Transistor PNP = 2SAR573D)

Parameter	Modeled *(Note1)*	Design Value		Unit	Error	Condition
		Datasheet	SPICE			
[CRTIMER]						
CRT Terminal Charge Current (I_{CRT})	✓	40	40.0	µA	0.0%	
CRT Terminal Charge Voltage (V_{CRT_CHA})	✓	0.80	0.800	V	0.0%	
CRT Terminal Discharge Voltage 1 (V_{CRT_DIS1})	✓	2.00	2.000	V	0.0%	
CRT Terminal Discharge Voltage 2 (V_{CRT_DIS2})	✓	2.40	2.400	V	0.0%	When V_{CRT} > V_{CRT_DIS2} R_{D1} -> R_{D2}
CRT Terminal Charge Resistor (R_{CHA})	✓	30.0	30.00	kΩ	0.0%	R_{CHA}= (V_{CRT_DIS1}-V_{CRT_CHA}) /I_{CRT}
CR Timer Discharge Constant (V_{CRT_CHA}/V_{CRT_DIS1})	✓	0.40	0.400	V/V	0.0%	
DISC Terminal On Resistor 1 (R_{DISC1})	✓	50	50.0	Ω	0.0%	I_{DISC}=10mA
DISC Terminal On Resistor 2 (R_{DISC2})	✓	5.0	5.00	kΩ	0.0%	I_{DISC}=100µA
PWMOUT Terminal Output High Voltage ($V_{PMWOUTH}$)	X	-	4.98	V		I_{PWMOUT}=-100µA
PWMOUT Terminal Output High Voltage ($V_{PMWOUTL}$)	X	-	0.02	V		I_{PWMOUT}=100µA
PWMOUT Terminal Sink Current Capability (I_{PWMOUT_SINK})	X	-	10.00	mA		
PWMOUT Terminal Source Current Capability (I_{PWMOUT_SOURCE})	X	-	10.0	mA		
CRT Terminal Leakage Current (I_{CRT_LEAK})	X	-	0.0	µA		V_{CRT}=70V
[LED Open Detection]						
LED Open Detection Voltage (V_{OPD})	✓	1.2	1.20	V	0.0%	V_{OPD}=V_{IN}-V_{OP}
OP Terminal Input Current (I_{OP})	✓	21	21.0	µA	0.0%	V_{OPD}=V_{IN}-0.5V
[Disable LED open Detection Function at Reduced-Voltage]						
OPM Terminal Source Current (I_{OPM})	✓	40	40.0	µA	0.0%	
VIN Terminal Disable LED Open Detection Voltage at Reduced-Voltage (V_{IN_OPM})	✓	V_{OPM} x 6.0	V_{OPM} x 6.0	V		VIN Terminal Voltage
OPM Terminal Input Voltage Range (V_{OPM_R})	X	-	-	V	-	
[Disable LED Open Detection Time Setting]						
Input Threshold Voltage (V_{DH})	✓	1.0	1.00	V	0.0%	
D Terminal Source Current ($I_{DSOURCE}$)	✓	230	230.0	µA	0.0%	
D Terminal On Resistor (R_D)	X	-	250.5	Ω	-	I_{D_EXT}=100µA

(Note 1) ✓: Model available (supported), X: Model not available” (not supported).

(Unless otherwise specified, V_{IN}=13V, C_{VREG}=1.0μF, Transistor PNP = 2SAR573D)

Parameter	Modeled *(Note1)*	Design Value		Unit	Error	Condition
		Datasheet	SPICE			
[Short Circuit Protection(SCP)]						
Short Circuit Protection Voltage (V_{SCP1})	✓	1.2	1.20	V	0.0%	
Short Circuit Protection Release Voltage (V_{SCPR})	✓	1.25	1.250	V	0.0%	
Short Circuit Protection Hysteresis Voltage (V_{SCPHYS})	✓	50	50.0	mV	0.0%	
SCP Terminal Source Current (I_{SCP})	✓	1.0	1.00	mA	0.0%	
SCP Terminal Source Current On Voltage (V_{SCP2})	✓	1.30	1.300	V	0.0%	
SCP Delay Time (t_{SCP2})	✓	20	20.0	µs	0.0%	
[PBUS]						
Input High Voltage (V_{PBUSH})	X	-	1.60	V	-	
Input Low Voltage (V_{PBUSL})	X	-	1.40	V	-	
Hysteresis Voltage ($V_{PBUSHYS}$)	✓	200	200.0	mV	0.0%	
PBUS Terminal Source Current (I_{PBUS})	✓	150	150	µA	0.0%	V_{EN}=5V
PBUS Terminal Output Low Voltage (V_{PBUSL})	X	-	0.18	V	-	I_{PBUS_EXT}=3mA
PBUS Terminal Output High Voltage (V_{PBUS_OH})	✓	4.5	4.39	V	2.4%	I_{PBUS_EXT}=-10µA
PBUS Terminal Leakage Current (I_{PBUS_LEAK})	X	-	0.0	µA	-	V_{PBUS}=7V
[EN]						
Input High Voltage (V_{ENH})	X	-	1.50	V	0.0%	
Input Low Voltage (V_{ENL})	X	-	1.44	V	0.0%	
Hysteresis Voltage (V_{ENHYS})	✓	60	60.0	mV	0.0%	
Terminal Input Current (I_{EN})	✓	7	7.0	µA	0.0%	V_{EN} = 5V
[UVLO VIN]						
UVLO Detection Voltage (V_{UVLOD})	✓	4.10	4.100	V	0.0%	V_{IN} : Sweep down
UVLO Release Voltage (V_{UVLOR})	✓	4.50	4.500	V	0.0%	V_{IN} : Sweep up, V_{REG} > 3.75V
UVLO Hysteresis Voltage (V_{HYS})	✓	0.4	0.40	V	0.0%	

(Note 1) ✓: Model available (supported), X: Model not available” (not supported).

Characteristic on Board (vs. Measured Waveform)

1. I_{VIN2} vs. V_{IN}

<u>Simulation Setting</u>
Type: DC Sweep
Sweep variable : VIN
(0V to 20V, 0.1Vstep)

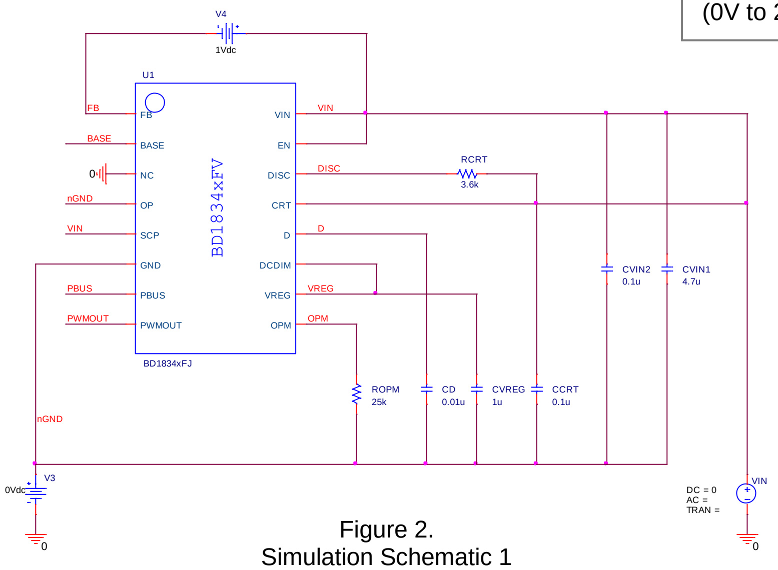

Figure 2.
Simulation Schematic 1

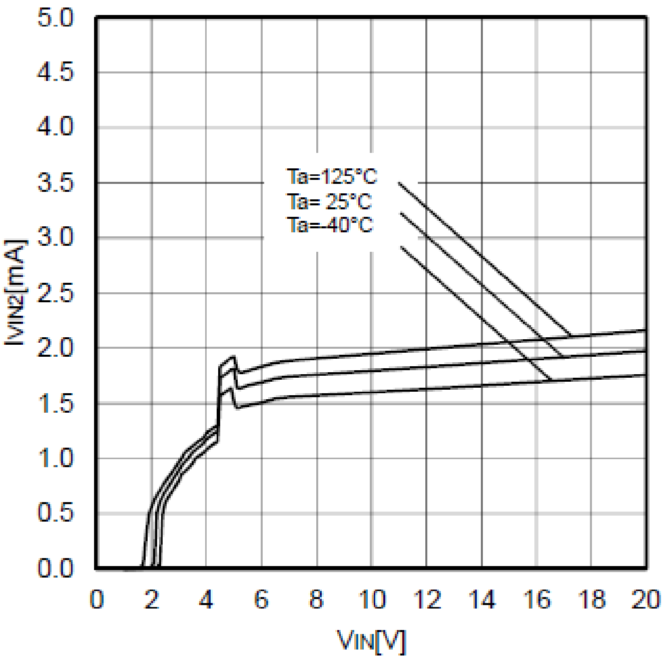

Figure 3.
I_{VIN2} vs. V_{IN}
(Measured Waveform)

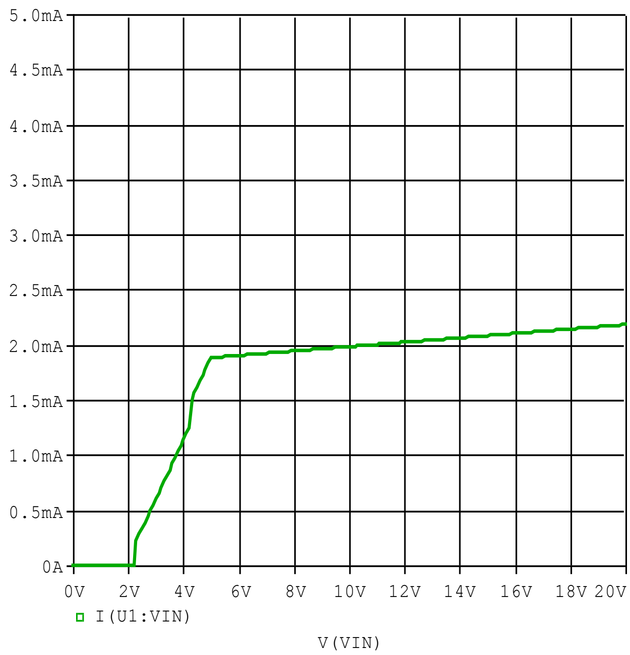

Figure 4.
I_{VIN2} vs. V_{IN}
(SPICE Simulation)

Table 4. Characteristics Comparison

(Unless otherwise specified, V_{IN}=13V, C_{VREG}=1.0μF, Transistor PNP = 2SAR573D)

Parameter	Measured Result	SPICE Simulation Result	Unit	Error	Condition
Circuit Current	1.8	1.89	mA	5.0%	-

(Note 1) The above data is based on a specific sample and it is not a guaranteed value.

2. VREG vs. VIN

Simulation Setting
Type: DC Sweep
Sweep variable : VIN
(0V to 20V, 0.1V step)

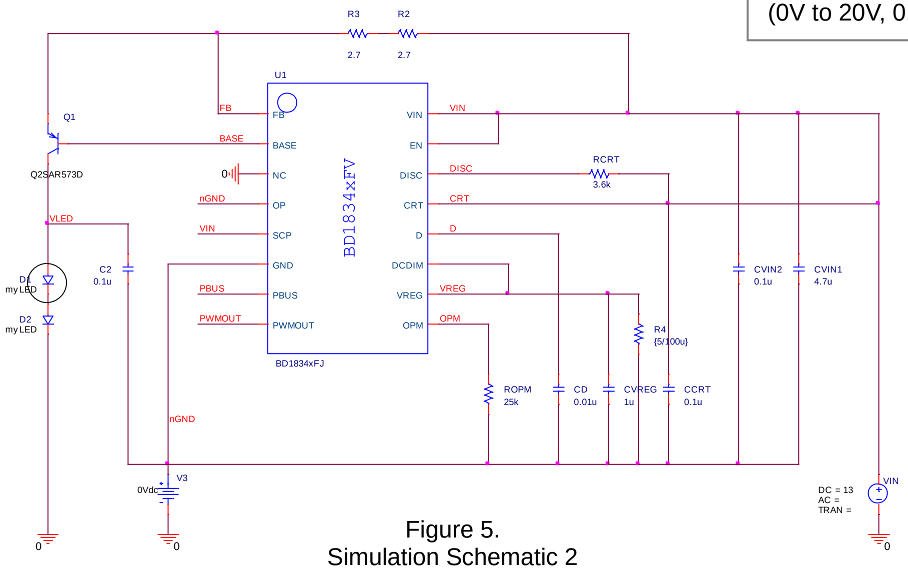

Figure 5.
Simulation Schematic 2

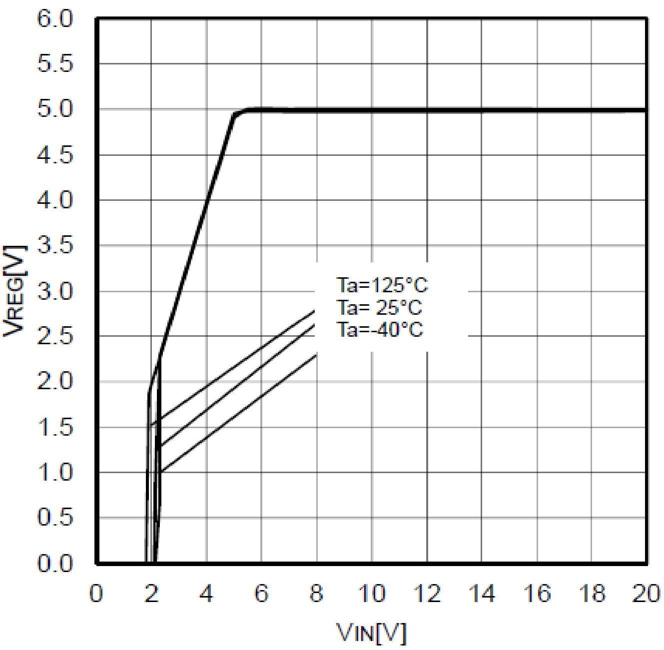

Figure 6.
VREG vs. VIN
(Measured Waveform)

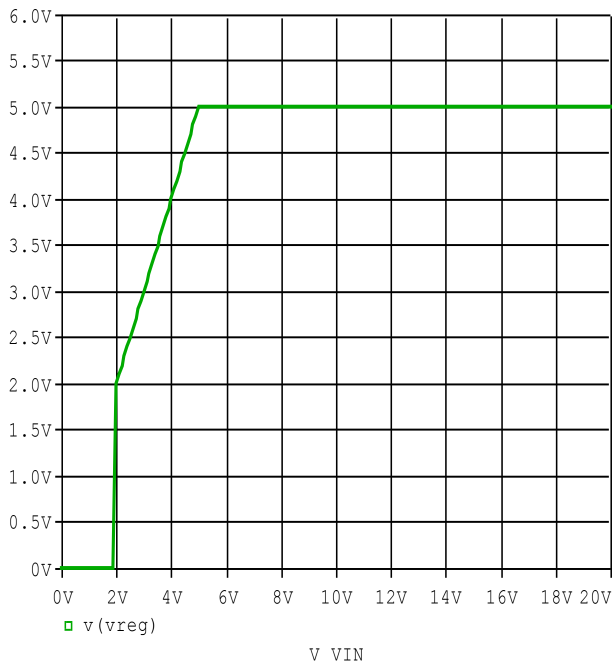

Figure 7.
VREG vs. VIN
(SPICE Simulation)

Table 5. Characteristics Comparison

(Unless otherwise specified, V_{IN}=13V, C_{VREG}=1.0µF, Transistor PNP = 2SAR573D)

Parameter	Measured Result	SPICE Simulation Result	Unit	Error	Condition
VREG Terminal Voltage	5.0	5.00	V	0.0%	-

(Note 1) The above data is based on a specific sample and it is not a guaranteed value.

3. I_{LED} vs. $R_{FB1}+R_{FB2}$

Simulation Setting
Type: DC Sweep
Sweep variable : RFB
(1Ω to 14Ω, 1Ωstep)

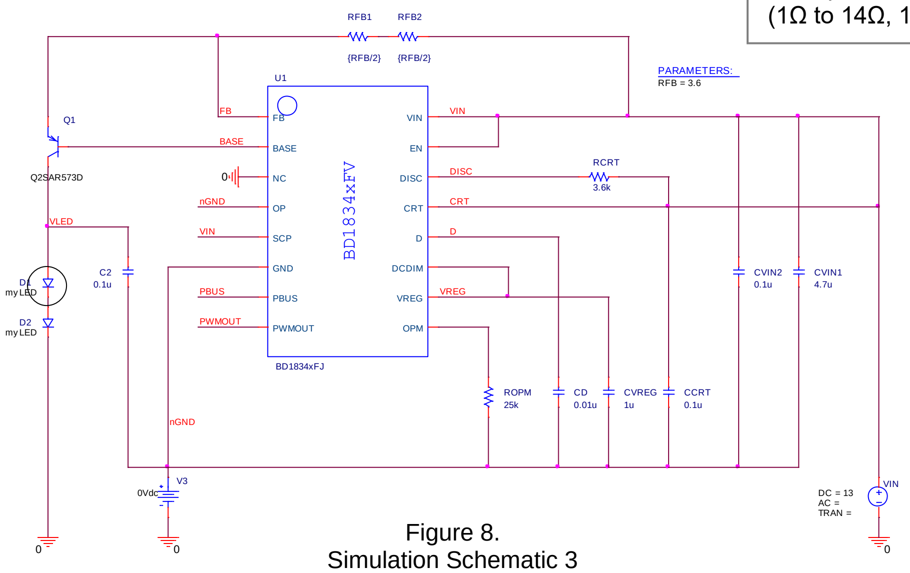

Figure 8.
Simulation Schematic 3

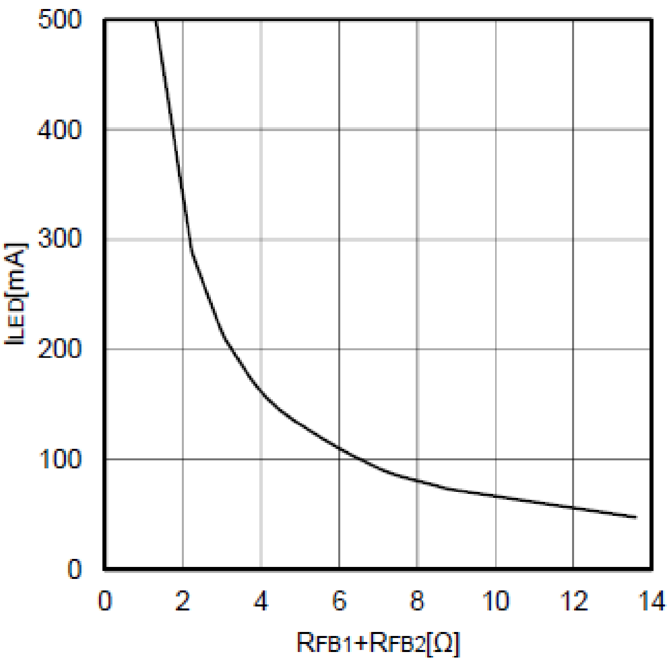

Figure 9.
I_{LED} vs. $R_{FB1}+R_{FB2}$
(Measured Waveform)

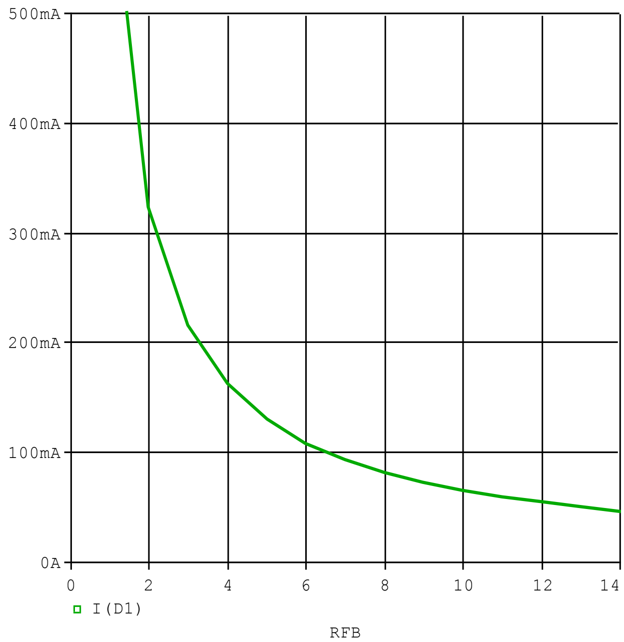

Figure 10.
I_{LED} vs. $R_{FB1}+R_{FB2}$
(SPICE Simulation)

Table 6. Characteristics Comparison

(Unless otherwise specified, V_{IN}=13V, C_{VREG}=1.0µF, Transistor PNP = 2SAR573D)

Parameter	Measured Result	SPICE Simulation Result	Unit	Error	Condition
I_{LED}	120	120.9	mA	0.8%	$R_{FB1}=R_{FB2}$=2.7Ω

(Note 1) The above data is based on a specific sample and it is not a guaranteed value.

4. I_{LED} vs. R_{FB1}+R_{FB2}

Simulation Setting
Type: DC Sweep
Sweep variable : RFB
(1Ω to 14Ω, 1Ωstep)

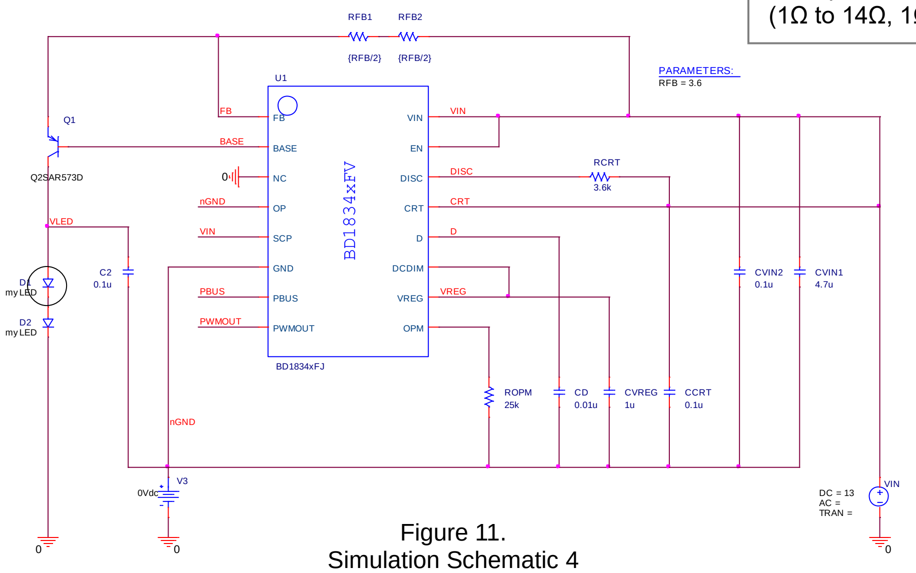

Figure 11.
Simulation Schematic 4

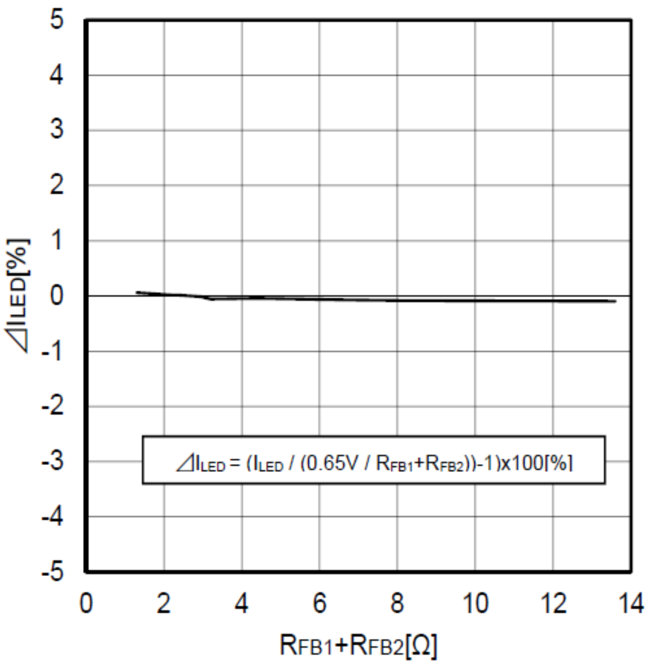

Figure 12.
Δ I_{LED} vs. R_{FB1}+R_{FB2}
(Measured Waveform)

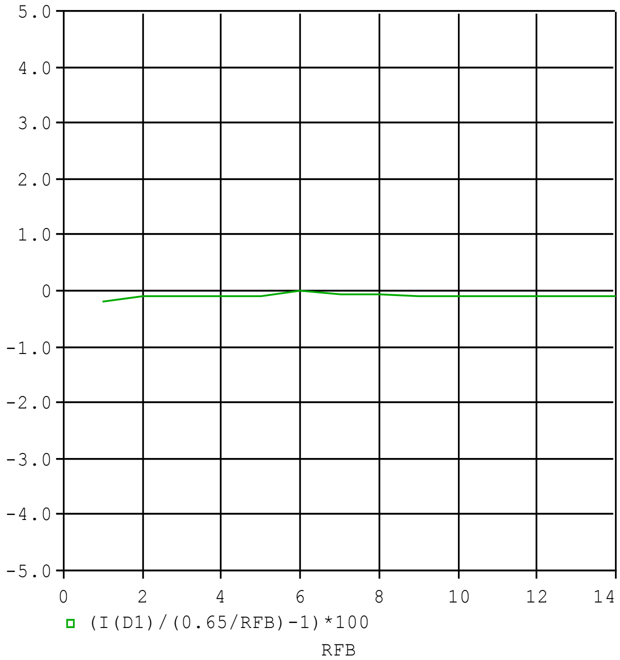

Figure 13.
Δ I_{LED} vs. R_{FB1}+R_{FB2}
(SPICE Simulation)

Table 7. Characteristics Comparison

(Unless otherwise specified, V_{IN}=13V, C_{VREG}=1.0µF, Transistor PNP = 2SAR573D)

Parameter	Measured Result	SPICE Simulation Result	Unit	Error	Condition
⊿I_{LED}	-0.05	-0.066	%	32.0%	R_{FB1}=R_{FB2}=2.7Ω

(Note 1) The above data is based on a specific sample and it is not a guaranteed value.

5. VFBREG vs. VDCDIM

Simulation Setting
Type: DC Sweep
Sweep variable : VDCDIM
(0V to 2V, 0.1V step)

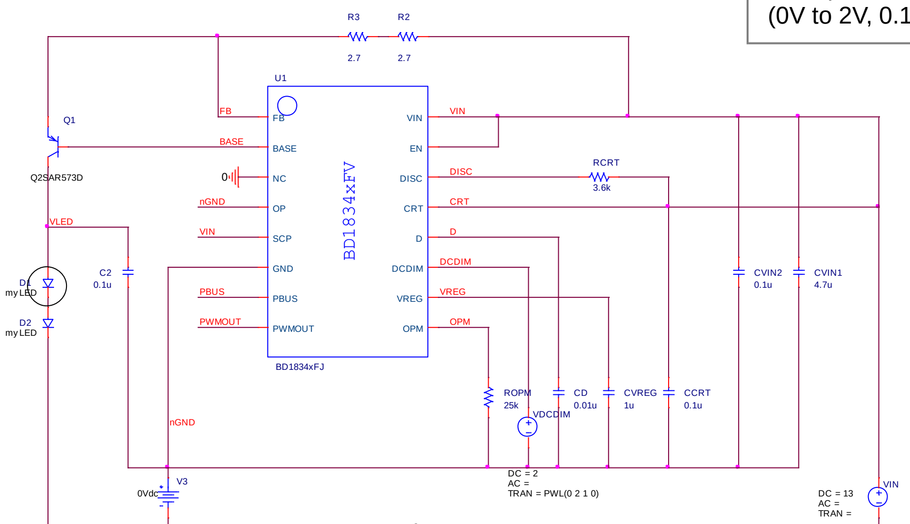

Figure 14.
Simulation Schematic 5

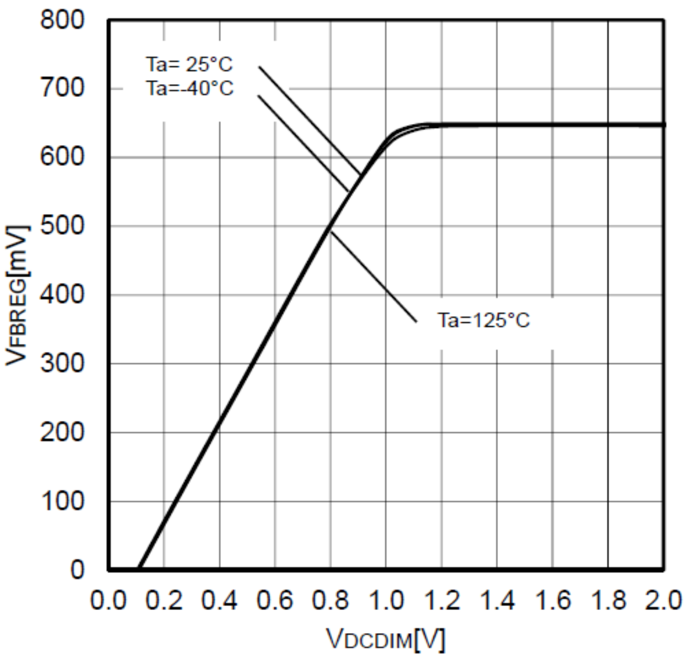

Figure 15.
VFBREG vs. VDCDIM
(Measured Waveform)

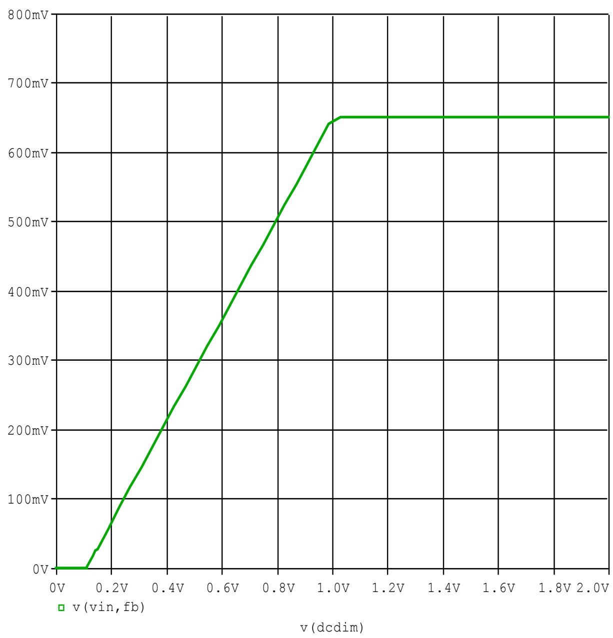

Figure 16.
VFBREG vs. VDCDIM
(SPICE Simulation)

Table 8. Characteristics Comparison

(Unless otherwise specified, V_{IN}=13V, C_{VREG}=1.0µF, Transistor PNP = 2SAR573D)

Parameter	Measured Result	SPICE Simulation Result	Unit	Error	Condition
DC Diming Gain	725	730.5	mV/V	0.8%	V_{DCDIM}:0.75V -> 0.35V

(Note 1) The above data is based on a specific sample and it is not a guaranteed value.

6. IBASE vs. VIN

Simulation Setting
Type: DC Sweep
Sweep variable : VIN
(0V to 20V, 0.1V step)

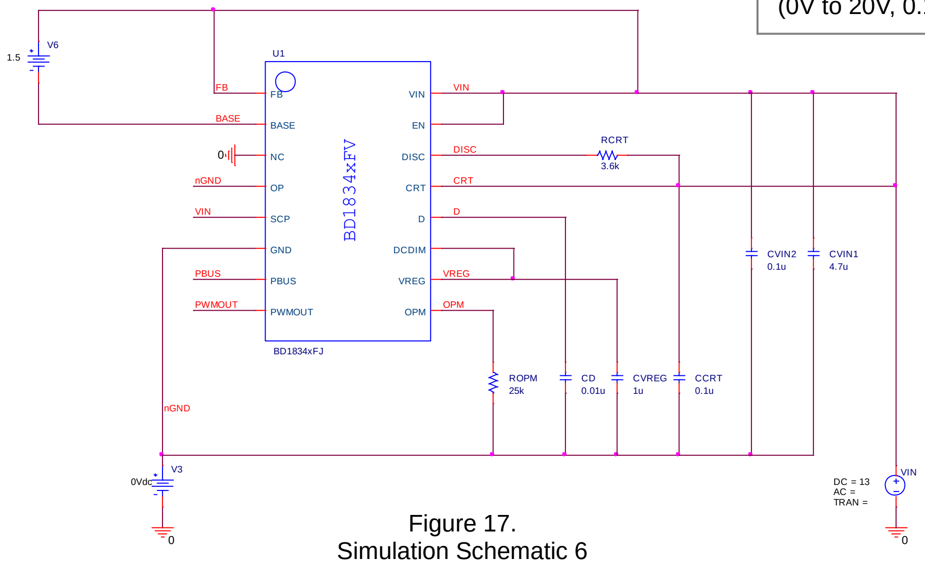

Figure 17.
Simulation Schematic 6

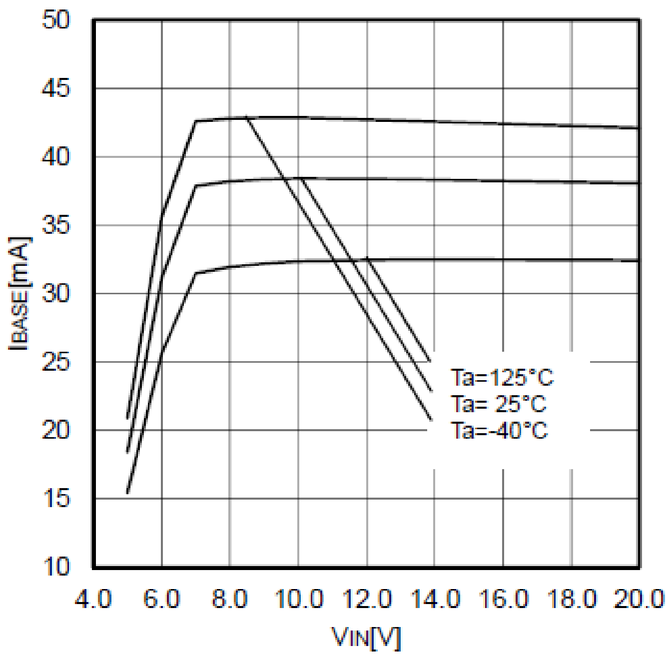

Figure 18.
IBASE vs. VIN
(Measured Waveform)

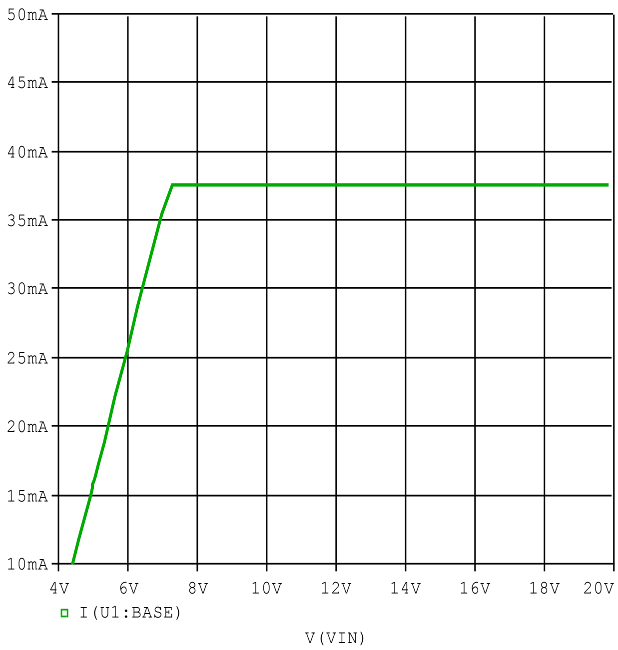

Figure 19.
IBASE vs. VIN
(SPICE Simulation)

Table 9. Characteristics Comparison

(Unless otherwise specified, V_{IN}=13V, C_{VREG}=1.0μF, Transistor PNP = 2SAR573D)

Parameter	Measured Result	SPICE Simulation Result	Unit	Error	Condition
BASE Terminal Sink Current Capability	38	37.5	mA	1.3%	V_{FB}=V_{IN}, V_{BASE}=V_{IN}-1.5V

(Note 1) The above data is based on a specific sample and it is not a guaranteed value.

7. VFBREG vs. VIN

Simulation Setting
Type: DC Sweep
Sweep variable : VIN
(6V to 56V, 0.1V step)

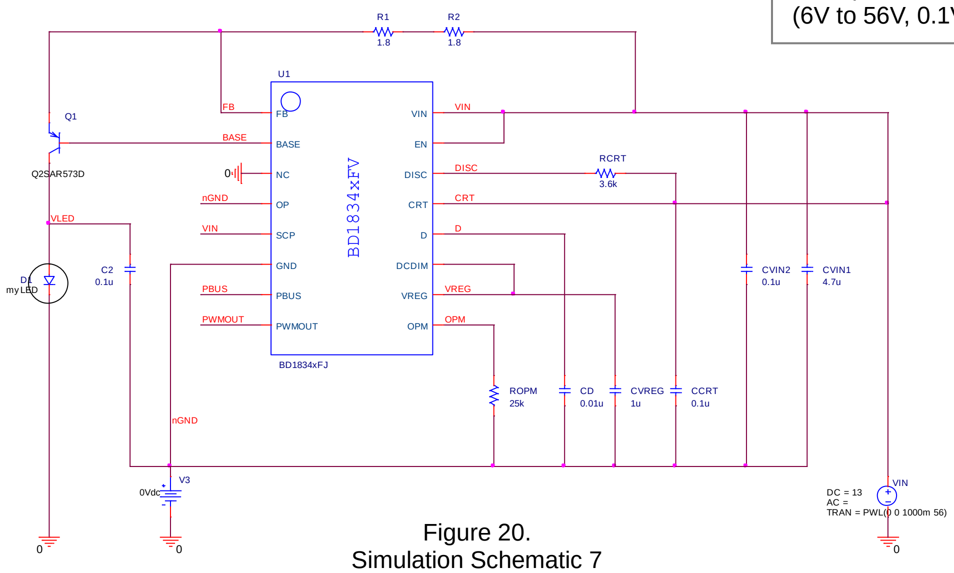

Figure 20.
Simulation Schematic 7

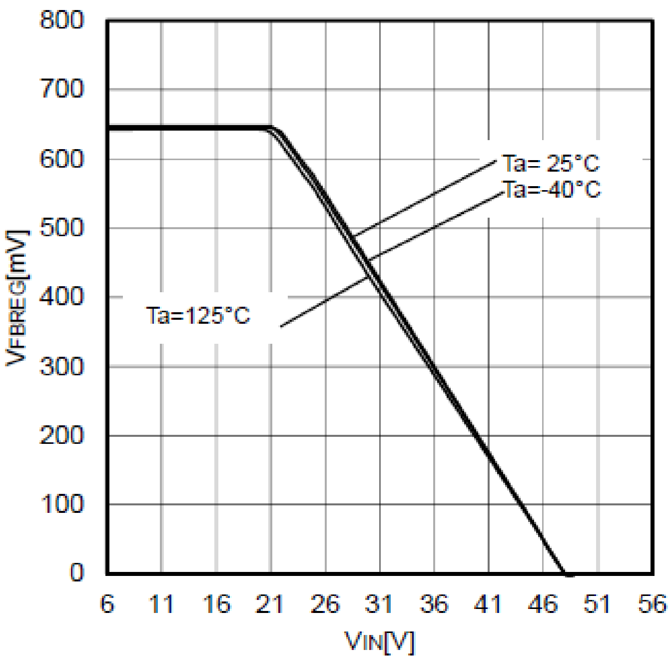

Figure 21.
IBASE vs. VIN
(Measured Waveform)

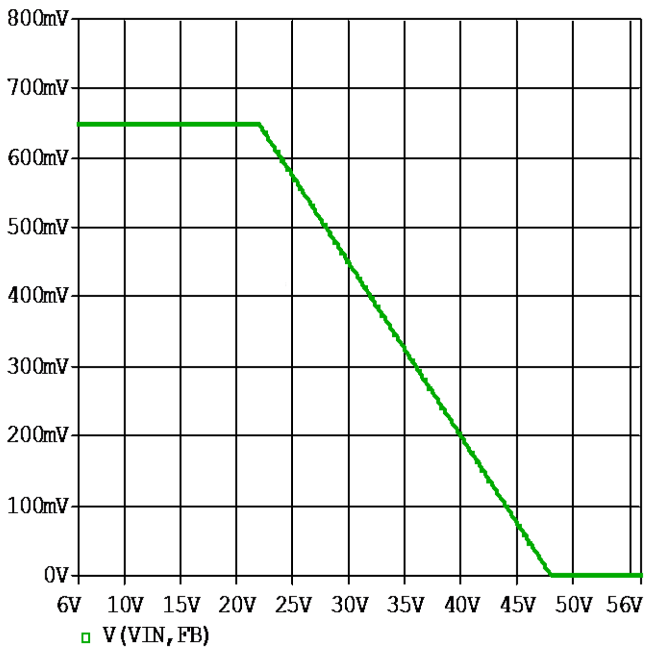

Figure 22.
IBASE vs. VIN
(SPICE Simulation)

Table 10. Characteristics Comparison

(Unless otherwise specified, V_{IN}=13V, C_{VREG}=1.0µF, Transistor PNP = 2SAR573D)

Parameter	Measured Result	SPICE Simulation Result	Unit	Error	Condition
Over Voltage Mute Gain	-25	-24.8	mV/V	0.8%	$\Delta V_{FB}/\Delta V_{IN}$

(Note 1) The above data is based on a specific sample and it is not a guaranteed value.

Revision History

Date	Revision	Changes
Sep.2019	001	New Release

Notes

1) The information contained herein is subject to change without notice.

2) Before you use our Products, please contact our sales representative and verify the latest specifications :

3) Although ROHM is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors.
Therefore, in order to prevent personal injury or fire arising from failure, please take safety measures such as complying with the derating characteristics, implementing redundant and fire prevention designs, and utilizing backups and fail-safe procedures. ROHM shall have no responsibility for any damages arising out of the use of our Poducts beyond the rating specified by ROHM.

4) Examples of application circuits, circuit constants and any other information contained herein are provided only to illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

5) The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM or any other parties. ROHM shall have no responsibility whatsoever for any dispute arising out of the use of such technical information.

6) The Products specified in this document are not designed to be radiation tolerant.

7) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a ROHM representative : transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.

8) Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters.

9) ROHM shall have no responsibility for any damages or injury arising from non-compliance with the recommended usage conditions and specifications contained herein.

10) ROHM has used reasonable care to ensure the accuracy of the information contained in this document. However, ROHM does not warrants that such information is error-free, and ROHM shall have no responsibility for any damages arising from any inaccuracy or misprint of such information.

11) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. For more details, including RoHS compatibility, please contact a ROHM sales office. ROHM shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

12) When providing our Products and technologies contained in this document to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.

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