

## SPICE Modeling Report

# 35V Voltage Resistance

# 1A LDO Regulator BD00C0AWFP-C

In this report, the characteristics that can be confirmed by the simulation using the SPICE model of the regulator IC BD00C0AWFP-C will be described.

### Simulation Environment

- Circuit Simulator : PSpice / Cadence Design System, Inc.
- Version Information : 17.2-2016
- OS Information : Windows 10 64-bit Edition

### File Information

- Library File Name : BDxxC0AxFP.lib
- Symbol File Name : BDxxC0AxFP.olb
- Subcircuit and Symbol

Table 1. Correspondence Table

Product Name	Subcircuit	Symbol	Product Name	Subcircuit	Symbol
BD00C0AWFP-C	BD00C0AWFP (Rev:5.00)	BD00C0AWFP	BD33C0AFP-C	BD33C0AFP (Rev:3.00)	BD33C0AFP
BD00C0AWHFP-C			BD33C0AHFP-C		
BD00C0AWFP2-C			BD33C0AFP2-C		
BD33C0AWFP-C	BD33C0AWFP (Rev:3.00)	BD33C0AWFP	BD50C0AFP-C	BD50C0AFP (Rev:3.00)	BD50C0AFP
BD33C0AWHFP-C			BD50C0AHFP-C		
BD33C0AWFP2-C			BD50C0AFP2-C		
BD50C0AWFP-C	BD50C0AWFP (Rev:3.00)	BD50C0AWFP	BD80C0AFP-C	BD80C0AFP (Rev:3.00)	BD80C0AFP
BD50C0AWHFP-C			BD80C0AHFP-C		
BD50C0AWFP2-C			BD80C0AFP2-C		
BD80C0AWFP-C	BD80C0AWFP (Rev:3.00)	BD80C0AWFP	BD90C0AFP-C	BD90C0AFP (Rev:3.00)	BD90C0AFP
BD80C0AWHFP-C			BD90C0AHFP-C		
BD80C0AWFP2-C			BD90C0AFP2-C		
BD90C0AWFP-C	BD90C0AWFP (Rev:3.00)	BD90C0AWFP			
BD90C0AWHFP-C					
BD90C0AWFP2-C					

### BD00C0AWFP SPICE MODEL

■ Terminal Information

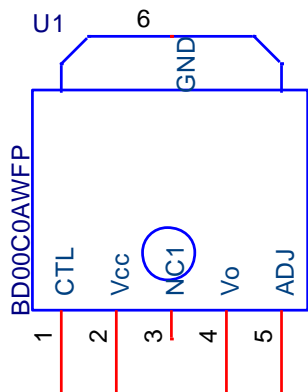


Table 2. Pin Table

Terminal No.	Terminal Name
1	CTL
2	V <sub>CC</sub>
3	NC1
4	V <sub>O</sub>
5	ADJ
6	GND

Figure 1. Symbol of BD00C0AWFP

### Verifiable Characteristics

- Electrical Characteristics (vs. Datasheet)..... 3
- Characteristics in SPICE (vs. Measured Waveform)
  - ✓ Circuit Current..... 4
  - ✓ Shutdown Current..... 5
  - ✓ Line Regulation..... 6
  - ✓ Load Regulation..... 7
  - ✓ Dropout Voltage..... 8
  - ✓ Ripple Rejection..... 9
  - ✓ Circuit Current by Load..... 10
  - ✓ CTL Current vs CTL Voltage..... 11
  - ✓ CTL Voltage vs Output Voltage..... 12

*(Note 1)* This model is not compatible with the influence of ambient temperature.

*(Note 2)* Please use the simulation results only as a design guide and the data reported herein is not a guaranteed value.

Moreover, the characteristics which are not included in the report may change depending on the actual board design and ROHM strongly recommend to double check those characteristics with actual board where the chips will be mounted on.

## Electrical Characteristics (vs. Datasheet)

Table 3. Electrical Characteristics Comparison

Unless otherwise specified,  $V_{CC}=13.5V$ ,  $I_O=0mA$ ,  $V_{CTL}=5.0V$  (With SW).  
 The resistor of between ADJ and  $V_O=56.7k\Omega$ , ADJ and GND= $10k\Omega$  ( $V_O=5V$ )

Parameter	Modeled (Note 1)	Value		Unit	Error	Condition
		Datasheet	SPICE			
Shutdown Current (With SW)	Yes	0	0.0	$\mu A$	-	$V_{CTL}=0V$
Circuit Current	Yes	0.5	0.50	mA	0.0%	
ADJ Terminal Voltage	Yes	0.750	0.7502	V	0.0%	$I_O=50mA$
Dropout Voltage	Yes	0.3	0.31	V	3.3%	$V_{CC}=4.75V$ , $I_O=500mA$
Ripple Rejection	Yes	55	54.8	dB	0.4%	$f=120Hz$ , Input Voltage Ripple=1Vrms, $I_O=100mA$
Line Regulation	Yes	20	19.6	mV	2.0%	$V_O+1.0V \leq V_{CC} \leq 26.5V$
Load Regulation	Yes	0.050	0.0482	V	3.6%	$5mA \leq I_O \leq 1A$
CTL On Mode Voltage (With SW)	Yes	-	1.75	V	-	ACTIVE MODE
CTL Off Mode Voltage (With SW)	Yes	-	1.75	V	-	OFF MODE
CTL Bias Current (With SW)	Yes	25	25.0	$\mu A$	0.0%	$V_{CTL}=5.0V$

(Note 1) Yes: Model available (supported), No: Model not available" (not supported).

Characteristics in SPICE (vs. Measured Waveform)

1. Circuit Current

**Simulation Setting**  
 Type : DC  
 Voltage Source : VCC  
 (0V to 26.5V, 0.01V step)

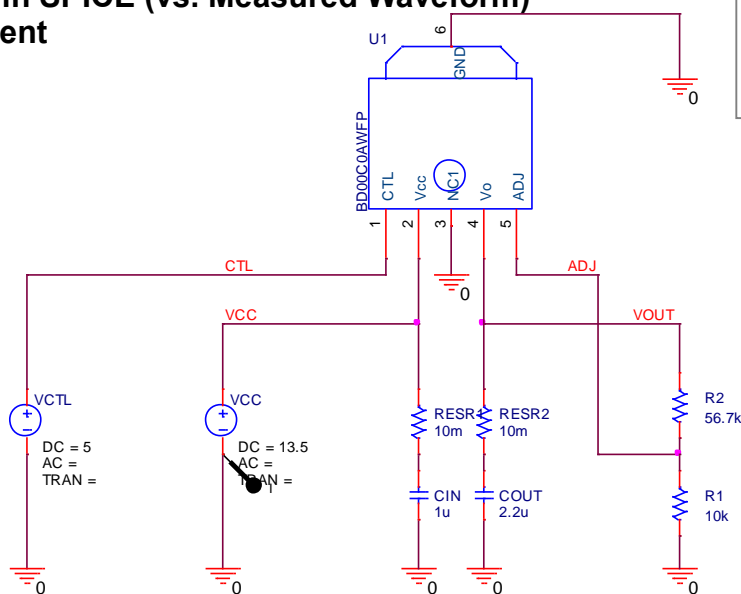


Figure 2. Simulation Schematic 1

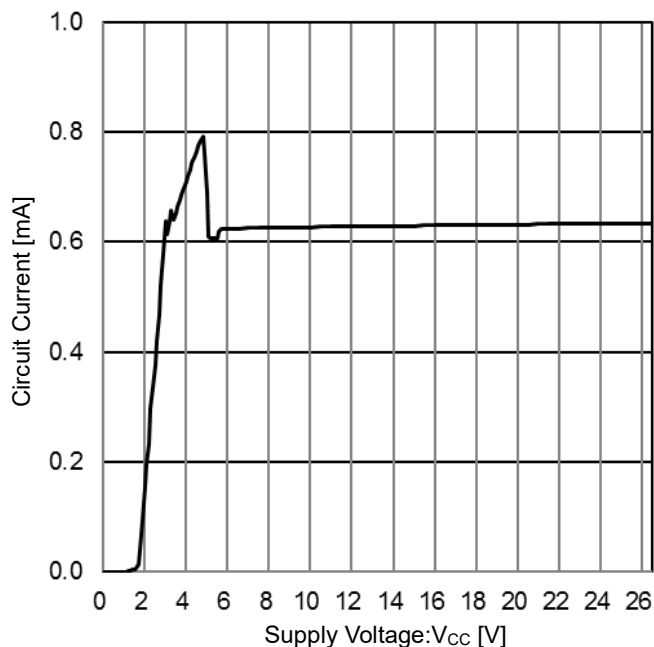


Figure 3. Circuit Current (Measured Waveform)

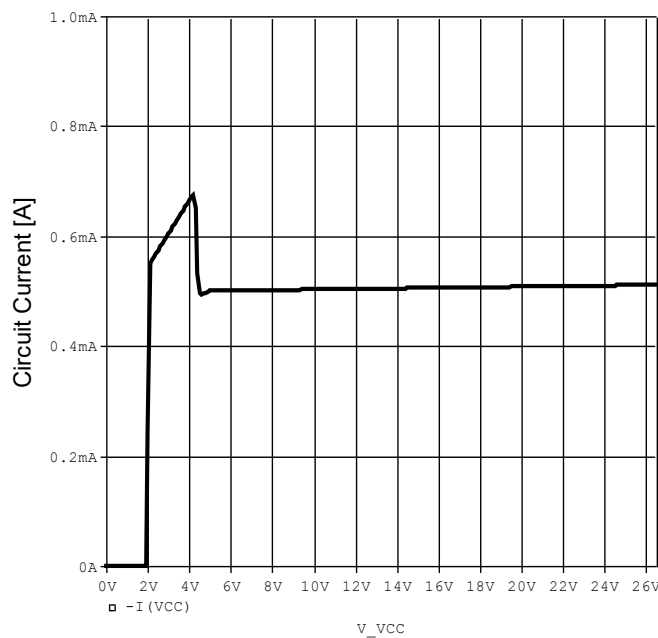


Figure 4. Circuit Current (SPICE Simulation)

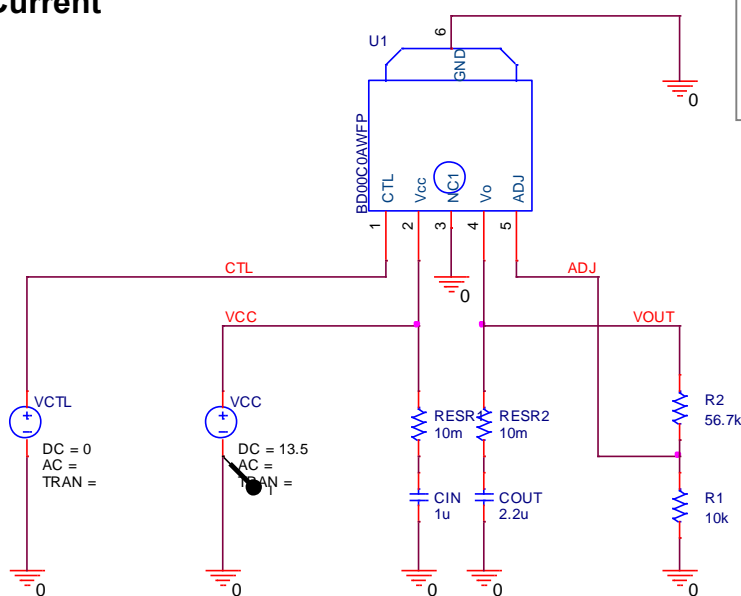
Table 4. Comparison of Characteristics

Unless otherwise specified,  $V_{CC}=13.5V$ ,  $V_{CTL}=5.0V$ ,  $I_O=0mA$ ,  $V_O=5.0V$ .  
 (The resistor of between ADJ and  $V_O=56.7k\Omega$ , ADJ and GND= $10k\Omega$ )

Parameter	Measured Result (Note 1)	SPICE Simulation Result	Unit	Error	Condition
Circuit Current	0.6	0.50	V	16.7%	-

(Note 1) The above data is based on a specific sample and it is not meant to be a guaranteed value.

2. Shutdown Current



**Simulation Setting**  
 Type : DC  
 Voltage Source : VCC  
 (0V to 26.5V, 0.01V step)

Figure 5. Simulation Schematic 2

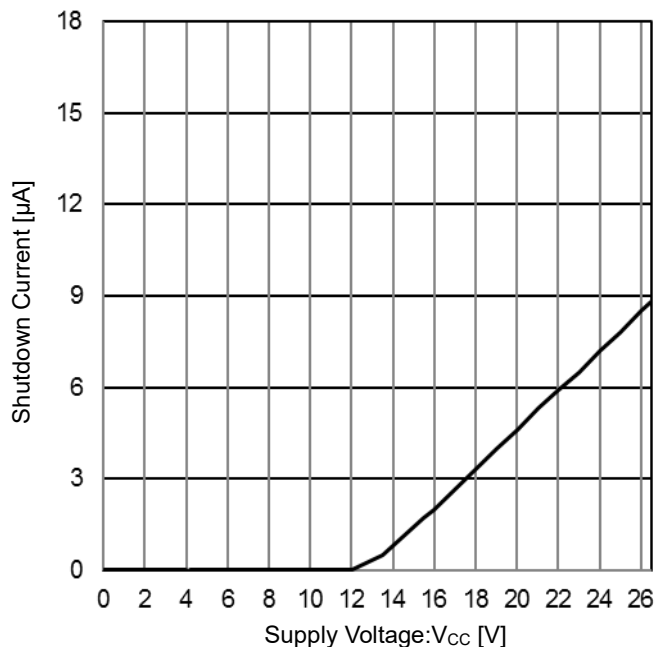


Figure 6. Shutdown Current (Measured Waveform)

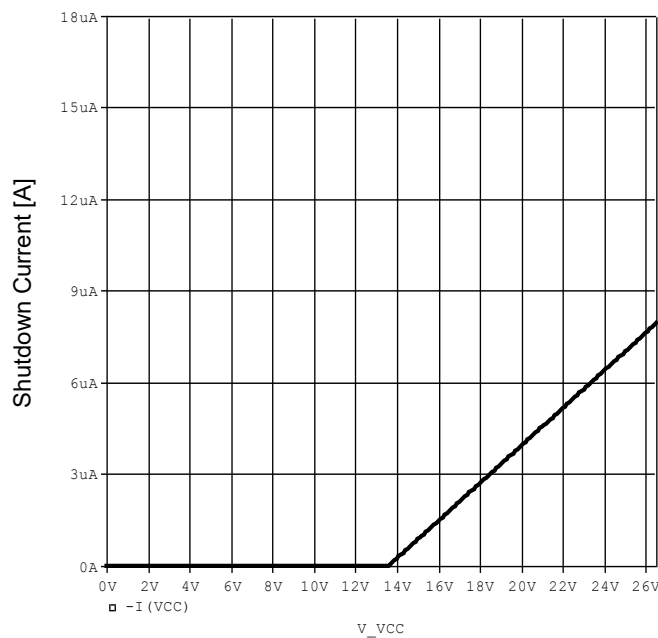


Figure 7. Shutdown Current (SPICE Simulation)

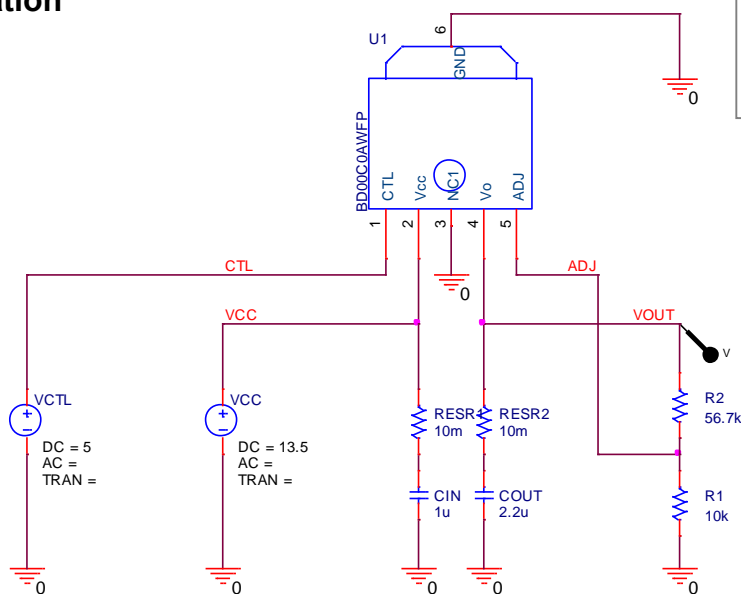
Table 5. Comparison of Characteristics

Unless otherwise specified, V<sub>CC</sub>=13.5V, V<sub>CTL</sub>=5.0V, I<sub>O</sub>=0mA, V<sub>O</sub>=5.0V.  
 (The resistor of between ADJ and V<sub>O</sub>=56.7kΩ, ADJ and GND=10kΩ)

Parameter	Measured Result (Note 1)	SPICE Simulation Result	Unit	Error	Condition
Shutdown Current	0.5	0.0	µA	-	V <sub>CTL</sub> =0V

(Note 1) The above data is based on a specific sample and it is not meant to be a guaranteed value.

### 3. Line Regulation



**Simulation Setting**  
 Type : DC  
 Voltage Source : VCC  
 (0V to 26.5V, 0.01V step)

Figure 8. Simulation Schematic 3

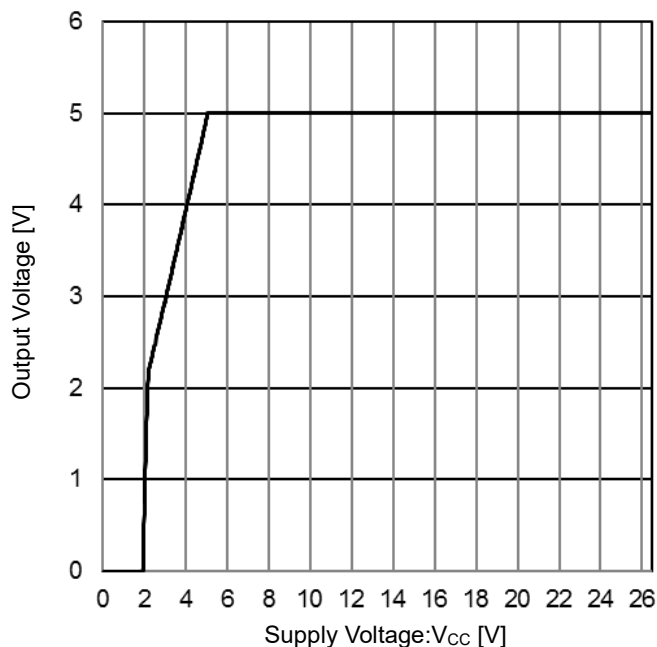


Figure 9. Line Regulation (Measured Waveform)

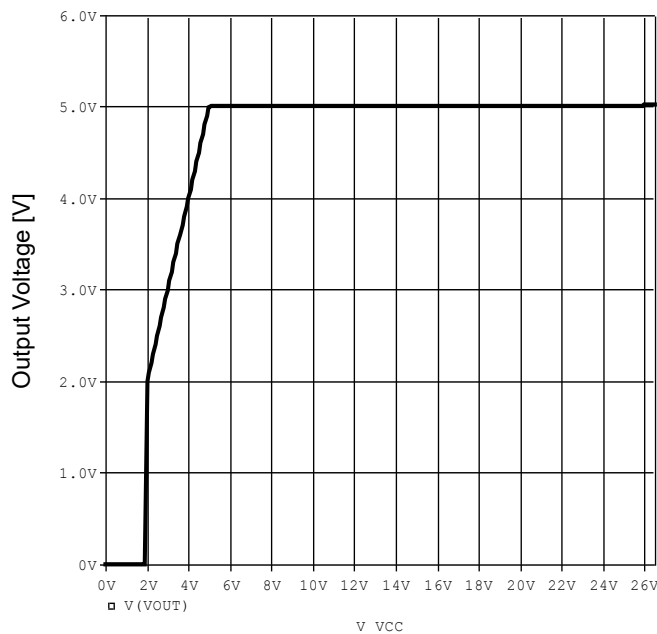


Figure 10. Line Regulation (SPICE Simulation)

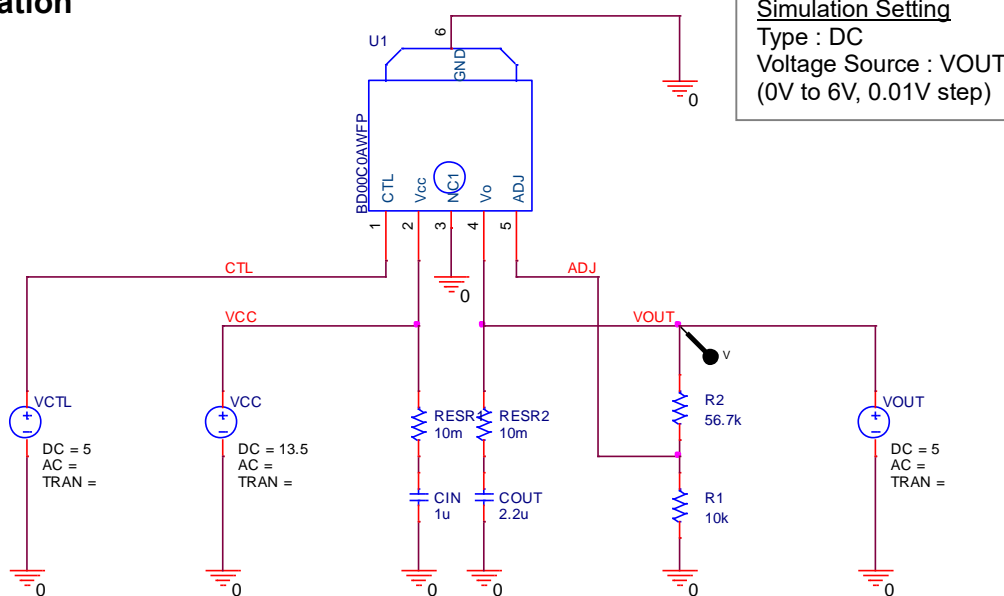
Table 6. Comparison of Characteristics

Unless otherwise specified,  $V_{CC}=13.5V$ ,  $V_{CTL}=5.0V$ ,  $I_O=0mA$ ,  $V_O=5.0V$ .  
 (The resistor of between ADJ and  $V_O=56.7k\Omega$ , ADJ and GND= $10k\Omega$ )

Parameter	Measured Result <i>(Note 1)</i>	SPICE Simulation Result	Unit	Error	Condition
Line Regulation	20	19.6	mV	2.0%	$V_O+1.0V \leq V_{CC} \leq 26.5V$

(Note 1) The above data is based on a specific sample and it is not meant to be a guaranteed value.

### 4. Load Regulation



**Simulation Setting**  
 Type : DC  
 Voltage Source : VOUT  
 (0V to 6V, 0.01V step)

Figure 11. Simulation Schematic 4

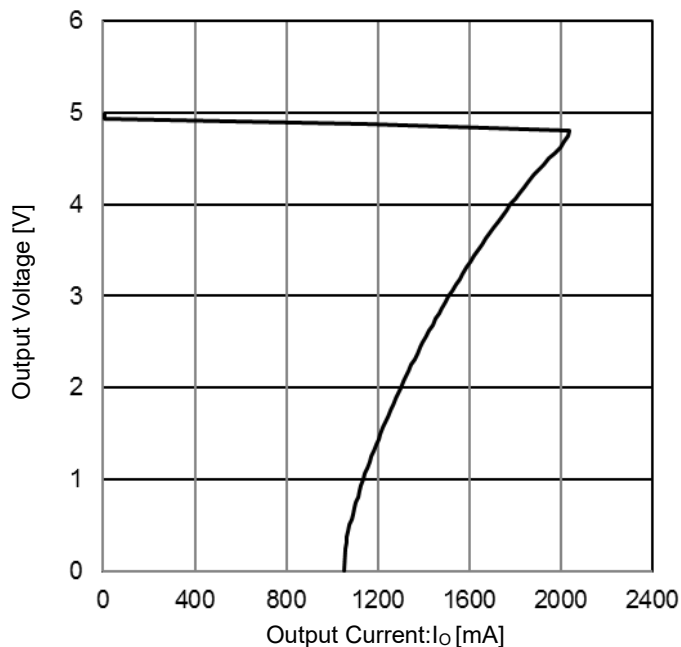


Figure 12. Load Regulation (Measured Waveform)

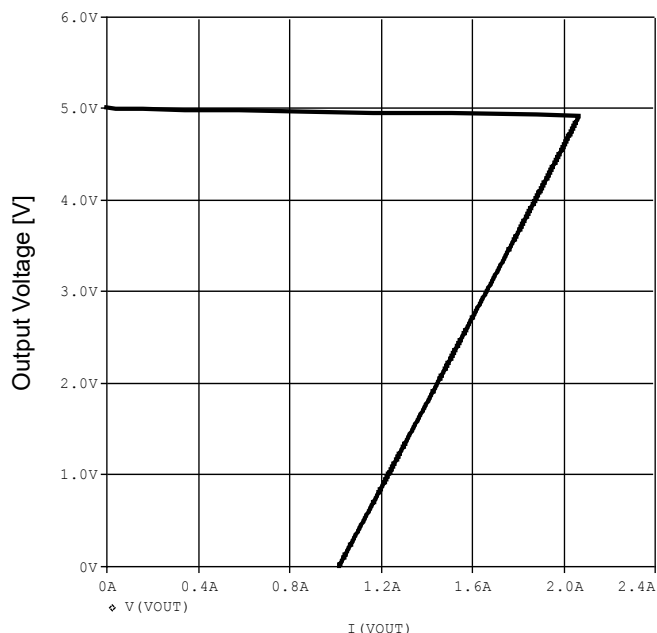


Figure 13. Load Regulation (SPICE Simulation)

Table 7. Comparison of Characteristics

Unless otherwise specified,  $V_{CC}=13.5V$ ,  $V_{CTL}=5.0V$ ,  $I_o=0mA$ ,  $V_o=5.0V$ .  
 (The resistor of between ADJ and  $V_o=56.7k\Omega$ , ADJ and GND= $10k\Omega$ )

Parameter	Measured Result <i>(Note 1)</i>	SPICE Simulation Result	Unit	Error	Condition
Load Regulation	0.050	0.0482	mV	3.6%	$5mA \leq I_o \leq 1A$

(Note 1) The above data is based on a specific sample and it is not meant to be a guaranteed value.

### 5. Dropout Voltage

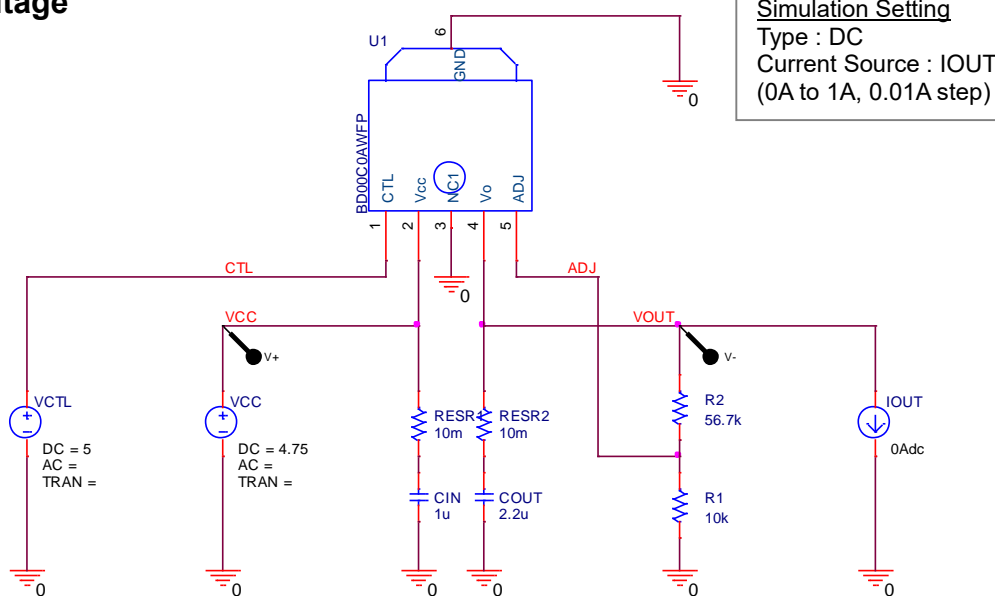


Figure 14. Simulation Schematic 5

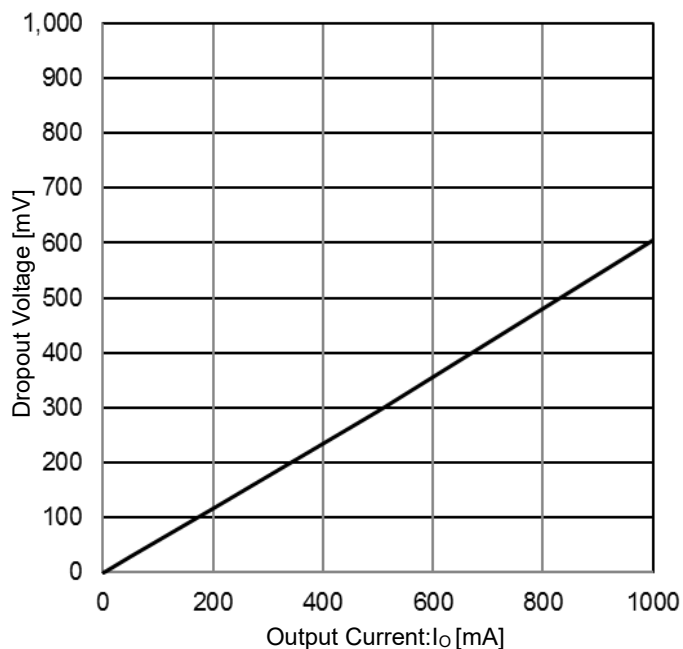


Figure 15. Dropout Voltage (Measured Waveform)

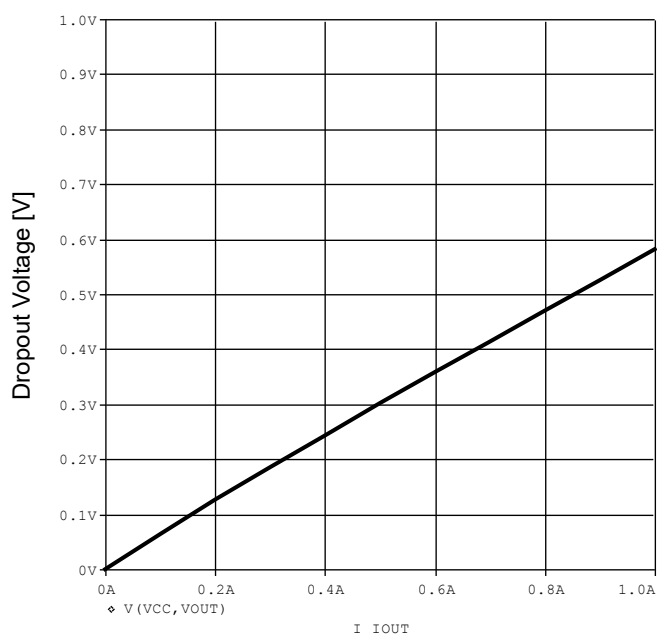


Figure 16. Dropout Voltage (SPICE Simulation)

Table 8. Comparison of Characteristics

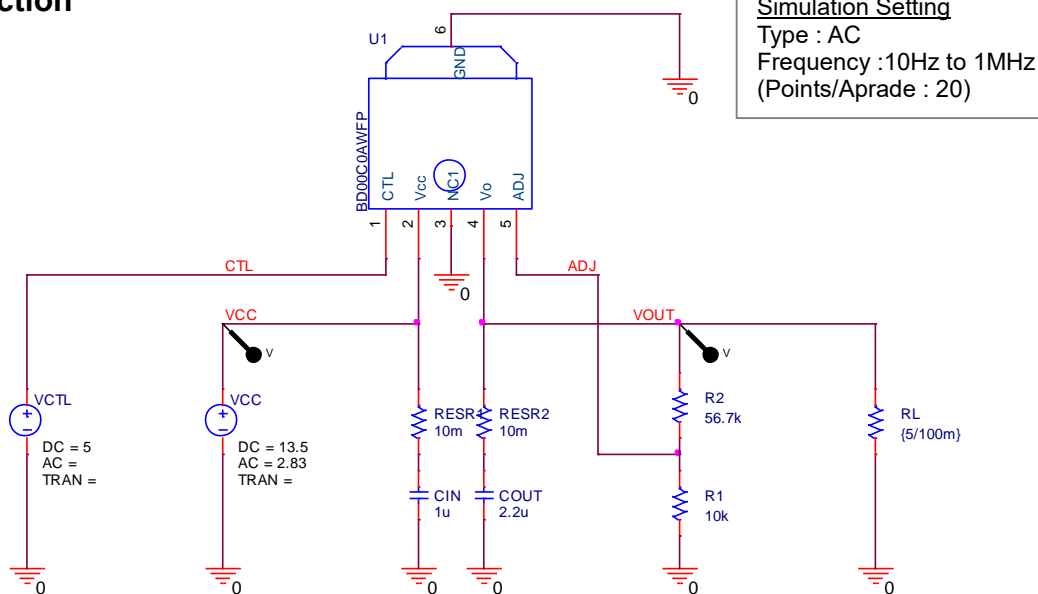
Unless otherwise specified,  $V_{CC}=13.5V$ ,  $V_{CTL}=5.0V$ ,  $I_o=0mA$ ,  $V_o=5.0V$ .  
 (The resistor of between ADJ and  $V_o=56.7k\Omega$ , ADJ and GND= $10k\Omega$ )

Parameter	Measured Result (Note 1)	SPICE Simulation Result	Unit	Error	Condition
Dropout Voltage	0.3	0.31	V	3.3%	$V_{CC}=4.75V$ , $I_o=500mA$

(Note 1) The above data is based on a specific sample and it is not meant to be a guaranteed value.



### 6. Ripple Rejection



**Simulation Setting**  
 Type : AC  
 Frequency : 10Hz to 1MHz  
 (Points/Prade : 20)

Figure 17. Simulation Schematic 6

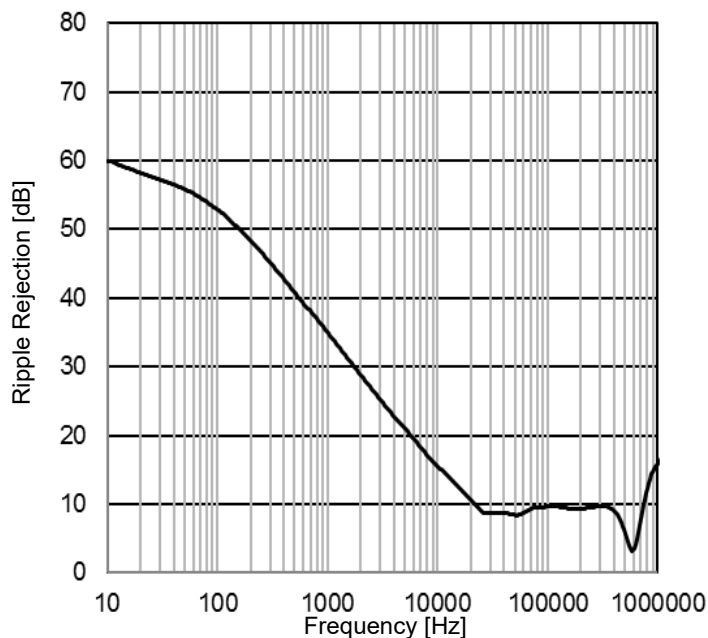


Figure 18. Ripple Rejection (Measured Waveform)

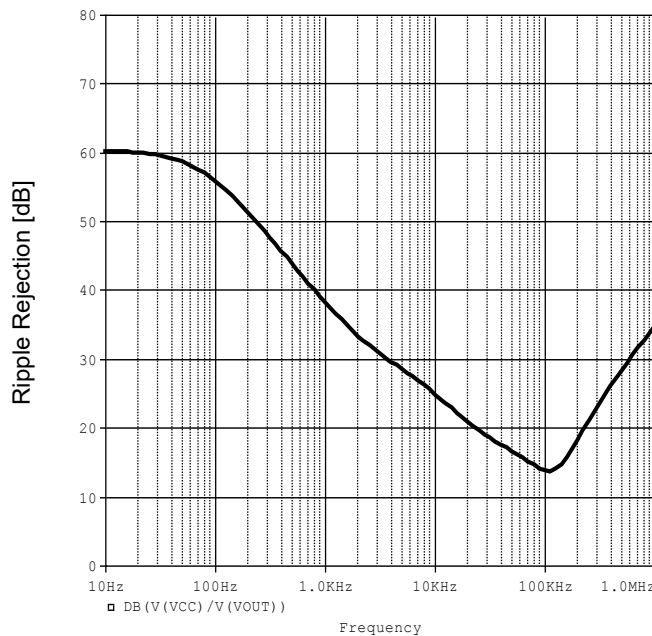


Figure 19. Ripple Rejection (SPICE Simulation)

Table 9. Comparison of Characteristics

Unless otherwise specified,  $V_{CC}=13.5V$ ,  $V_{CTL}=5.0V$ ,  $I_O=0mA$ ,  $V_O=5.0V$ .  
 (The resistor of between ADJ and  $V_O=56.7k\Omega$ , ADJ and GND=10k $\Omega$ )

Parameter	Measured Result <i>(Note 1)</i>	SPICE Simulation Result	Unit	Error	Condition
Ripple Rejection	53	54.8	dB	3.4%	f=120Hz, Input Voltage Ripple=1Vrms, $I_O=100mA$

(Note 1) The above data is based on a specific sample and it is not meant to be a guaranteed value.

7. Circuit Current by Load

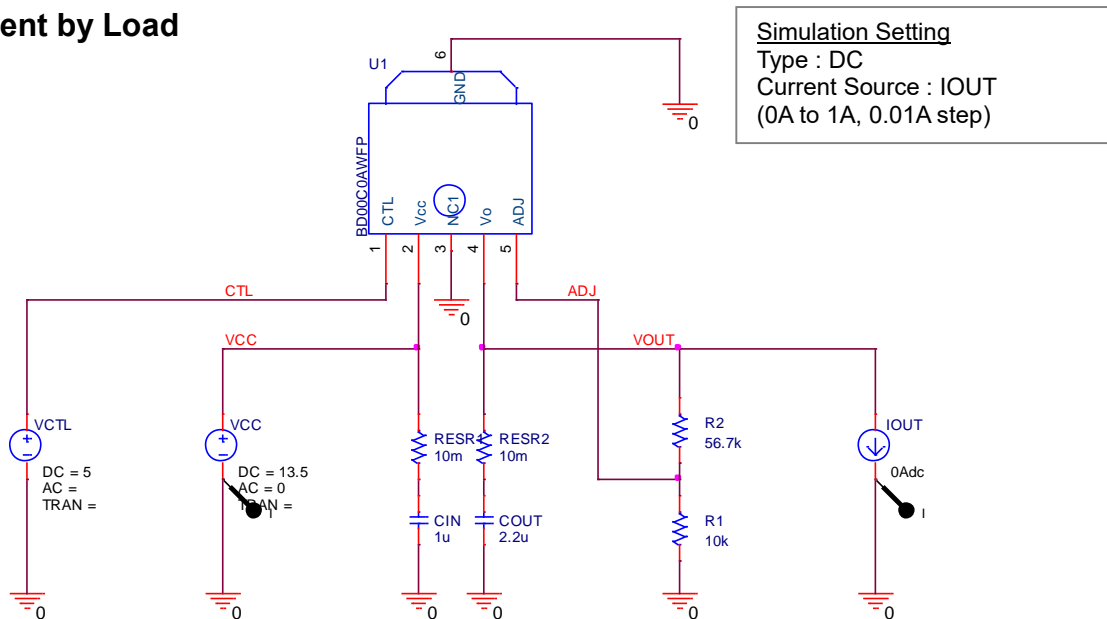


Figure 20. Simulation Schematic 7

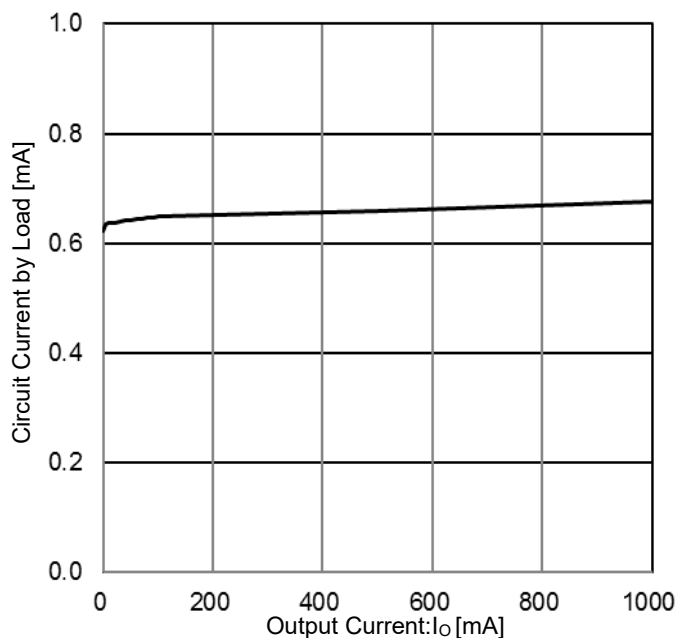


Figure 21. Circuit Current by Load (Measured Waveform)

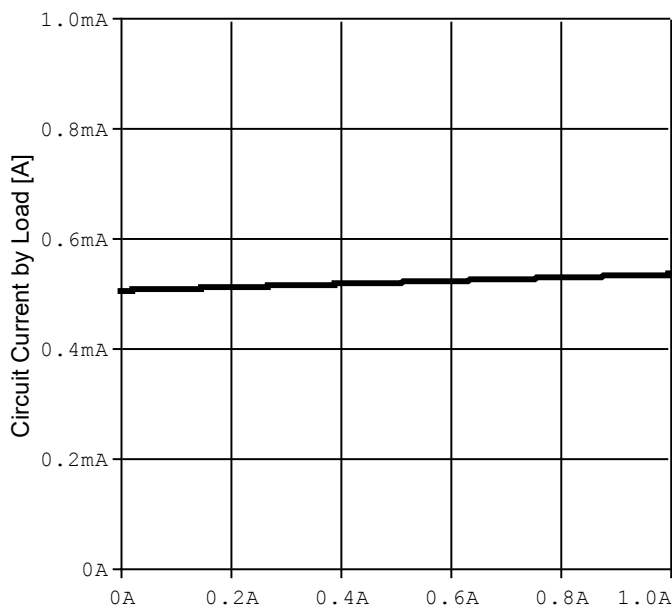


Figure 22. Circuit Current by Load (SPICE Simulation)

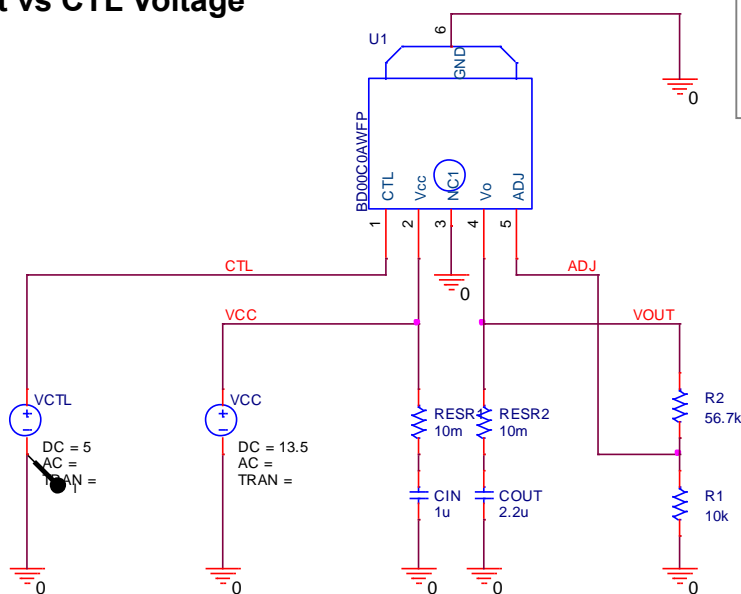
Table 10. Comparison of Characteristics

Unless otherwise specified,  $V_{CC}=13.5V$ ,  $V_{CTL}=5.0V$ ,  $I_O=0mA$ ,  $V_O=5.0V$ .  
 (The resistor of between ADJ and  $V_O=56.7k\Omega$ , ADJ and GND= $10k\Omega$ )

Parameter	Measured Result <i>(Note 1)</i>	SPICE Simulation Result	Unit	Error	Condition
Circuit Current	0.66	0.519	mA	21.4%	$I_O=500mA$

(Note 1) The above data is based on a specific sample and it is not meant to be a guaranteed value.

8. CTL Current vs CTL Voltage



**Simulation Setting**  
 Type : DC  
 Voltage Source : VCTL  
 (0V to 26.5V, 0.01V step)

Figure 23. Simulation Schematic 8

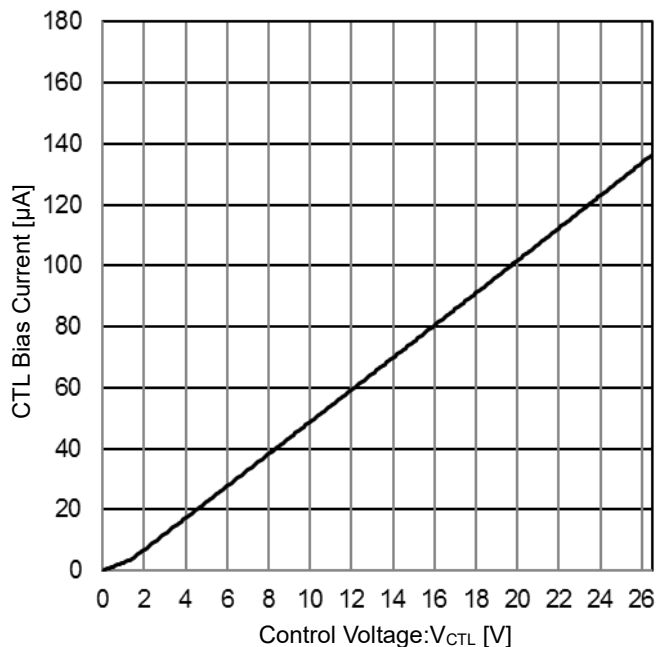


Figure 24. CTL Current vs CTL Voltage (Measured Waveform)

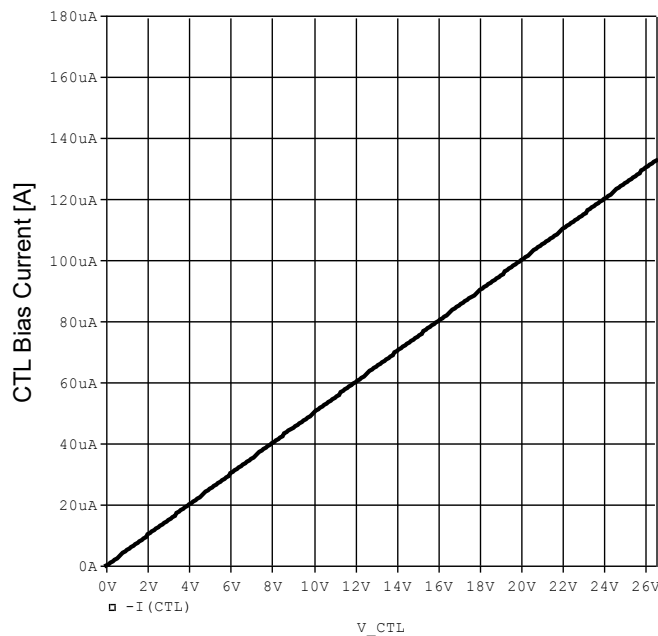


Figure 25. CTL Current vs CTL Voltage (SPICE Simulation)

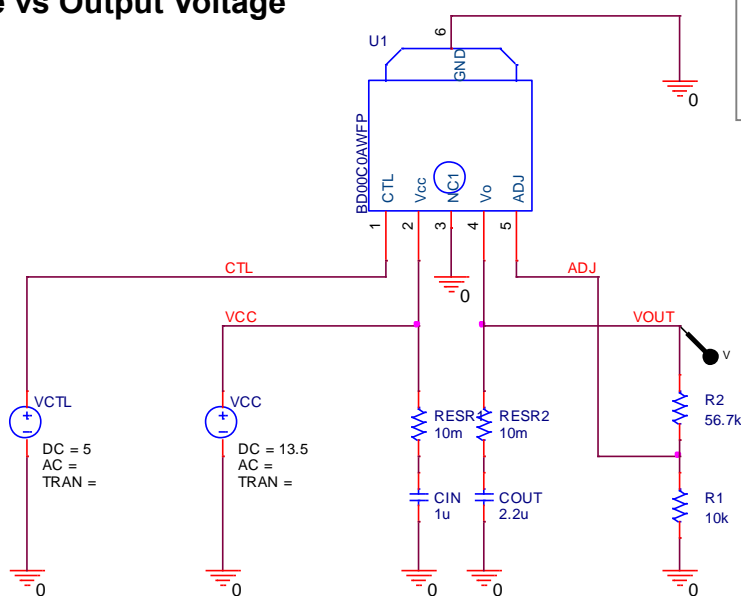
Table 11. Comparison of Characteristics

Unless otherwise specified, V<sub>CC</sub>=13.5V, V<sub>CTL</sub>=5.0V, I<sub>O</sub>=0mA, V<sub>O</sub>=5.0V.  
 (The resistor of between ADJ and V<sub>O</sub>=56.7kΩ, ADJ and GND=10kΩ)

Parameter	Measured Result (Note 1)	SPICE Simulation Result	Unit	Error	Condition
CTL Bias Current	25	25.0	μA	0.0%	-

(Note 1) The above data is based on a specific sample and it is not meant to be a guaranteed value.

### 9. CTL Voltage vs Output Voltage



**Simulation Setting**  
 Type : DC  
 Voltage Source : VCTL  
 (0V to 26.5V, 0.01V step)

Figure 26. Simulation Schematic 9

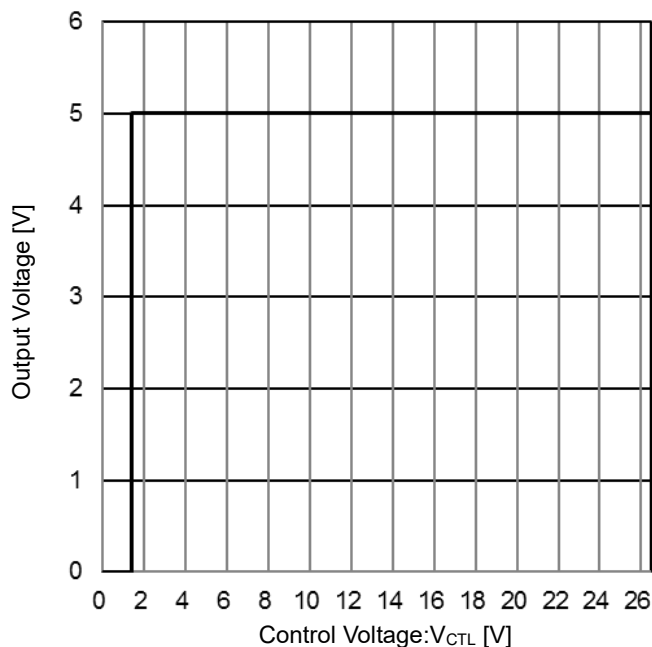


Figure 27. Output Voltage vs CTL Voltage (Measured Waveform)

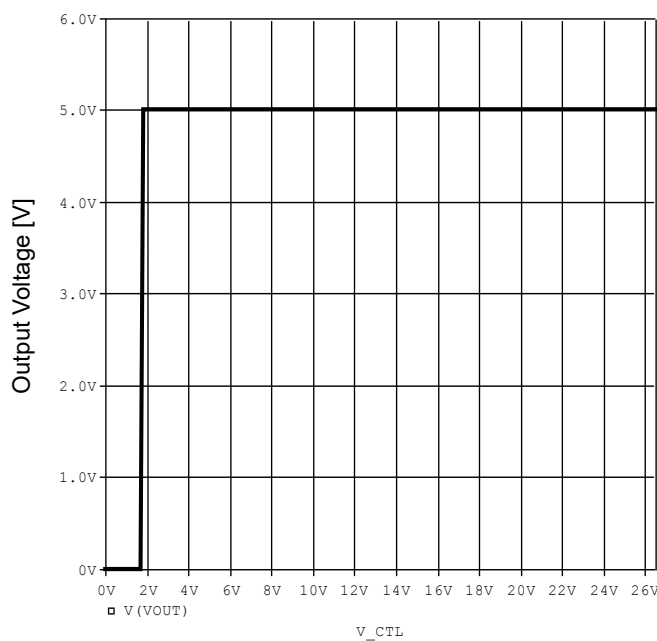


Figure 28. Output Voltage vs CTL Voltage (SPICE Simulation)

Table 12. Comparison of Characteristics

Unless otherwise specified,  $V_{CC}=13.5V$ ,  $V_{CTL}=5.0V$ ,  $I_O=0mA$ ,  $V_O=5.0V$ .  
 (The resistor of between ADJ and  $V_O=56.7k\Omega$ , ADJ and GND= $10k\Omega$ )

Parameter	Measured Result (Note 1)	SPICE Simulation Result	Unit	Error	Condition
CTL On Mode Voltage	1.7	1.70	mV	0.0%	ACTIVE MODE
CTL Off Mode Voltage	1.7	1.70	mV	0.0%	OFF MODE

(Note 1) The above data is based on a specific sample and it is not meant to be a guaranteed value.

**Revision History**

Date	Revision	Changes
Apr.2019	001	New Release

## Notes

- 1) The information contained herein is subject to change without notice.
- 2) Before you use our Products, please contact our sales representative and verify the latest specifications :
- 3) Although ROHM is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors.  
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