**ROHM Solution Simulator**

# Thermal Simulation of BD9xxN1EFJ Series Linear Regulators

This document introduces and describes the use of a simulation environment that allows simultaneous electrical and thermal simulation of BD9xxN1EFJ series linear regulators. By changing the parameters of the components, it is possible to simulate a wide range of conditions. As shown in the table below, there are four different thermal simulation circuits for the BD9xxN1EFJ series, depending on the output voltage and whether there is an enable pin. In this document, the BD933N1EFJ-C is used as a typical example.

Table 1. BD9xxN1EFJ series thermal simulation list

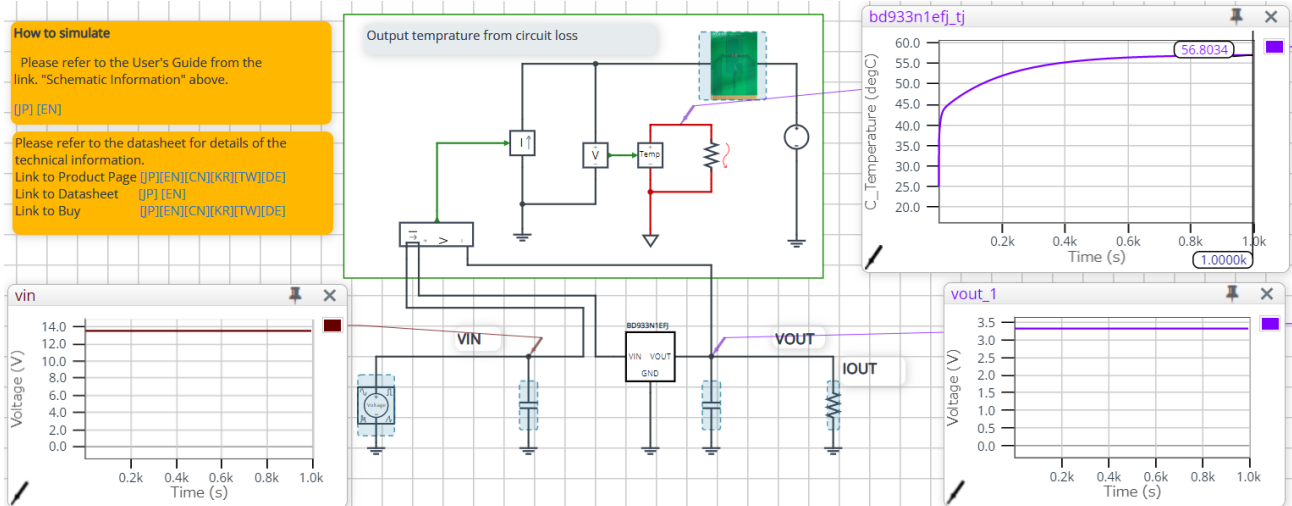| Product name | Output voltage | Enable pin | Package name | Simulation circuit |
|---|---|---|---|---|
| BD933N1EFJ-C | 3.3V | N/A | HTSOP-J8 | BD933N1EFJ-C_thermal simulation |
| BD950N1EFJ-C | 5.0V | N/A | HTSOP-J8 | BD950N1EFJ-C_thermal simulation |
| BD933N1WEFJ-C | 3.3V | ✓ | HTSOP-J8 | BD933N1WEFJ-C_thermal simulation |
| BD950N1WEFJ-C | 5.0V | ✓ | HTSOP-J8 | BD950N1WEFJ-C_thermal simulation |

# 1 Simulation circuit



Figure 1. Simulation circuit (BD933N1EFJ-C).

In Figure 1, the area within the green line shows the thermal simulation circuit and the rest of the figure shows the electrical simulation circuit.

This circuit is a step-down operation with respect to the input voltage, providing a 3.3 V or 5.0 V output for the BD9xxN1EFJ series.

The thermal simulation circuit creates a thermal simulation model of the device losses calculated in the electrical simulation and the linear regulator mounted on the board, and calculates the temperature of the linear regulator.

# 2    Simulation method

Simulation settings such as simulation time and convergence options can be set from "Simulation Settings" shown in Figure 2, and the initial simulation settings are shown in Table 2.

If you are having problems with the convergence of the simulation, you can change the advanced options to fix the problem. The simulation temperature and various parameters of the electrical circuit are defined in "Manual Options".
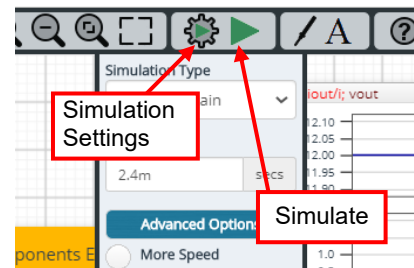


Figure 2. Simulation Settings and execution

Table 2. Initial values for Simulation Settings

| Parameters | Initial values | Remarks |
|---|---|---|
| Simulation Type | Time-Domain | Do not change the simulation type |
| End time | 1000 secs | |
| Advanced Options | More Speed | |
| Manual Options | .PARAM Ta | Set the ambient temperature |

## 3    Simulation conditions

### 3.1    Definition of parameters

The parameters for the components shown in blue in Figure 3 are defined in the manual options as the ambient temperature needs to be set.

Table 3 shows the initial values of the parameters. These values are written in a text box in the "Manual Options" section of the simulation settings, as shown in Figure 4.
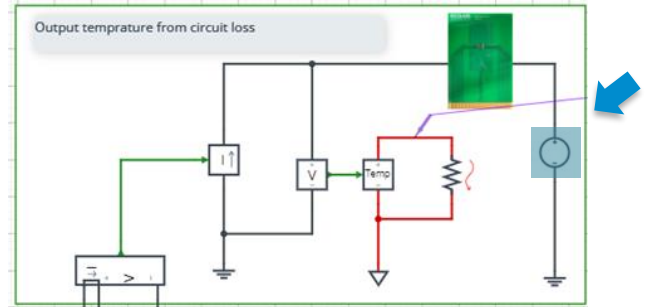


Figure 3. Definition of component parameters

Table 3. Simulation conditions

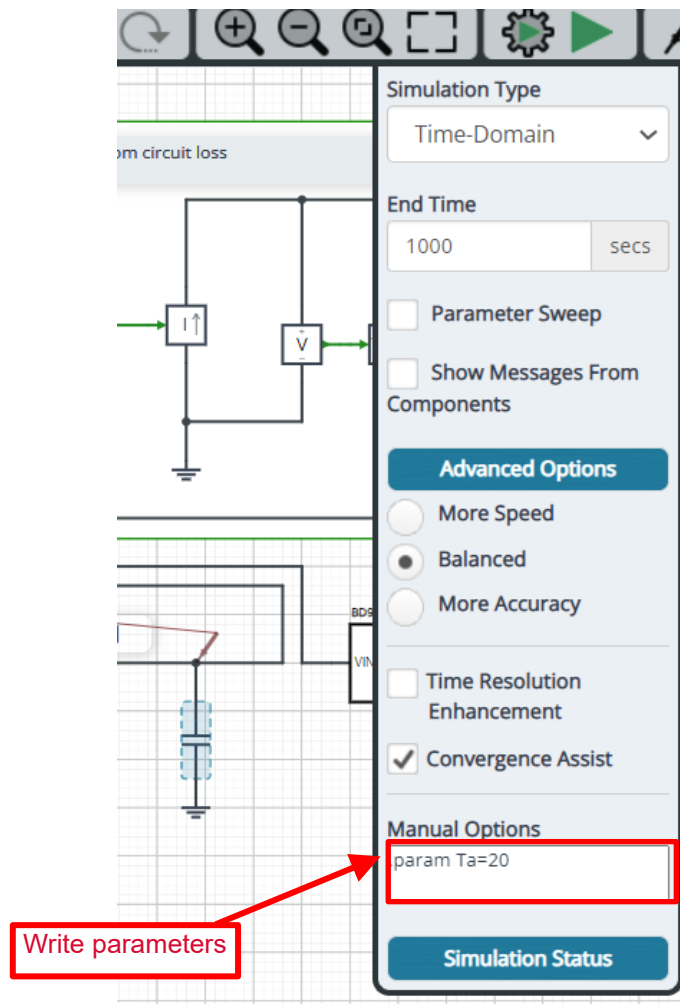| Parameters | Variable names | Initial values | Unit | Description |
|---|---|---|---|---|
| Temperature | Ta | 20 | °C | Ambient temperature |



Figure 4. Definition of parameters

## 3.2   Thermal circuit

The "BD933N1EFJ" symbol in Figure 5 is the thermal simulation model of the linear regulator. Also, Table 4 shows the terminal description for this model. The nodes shown in red in Figure 5 (BD933N1EFJ_TJ) can be used to check the temperature of the junction.
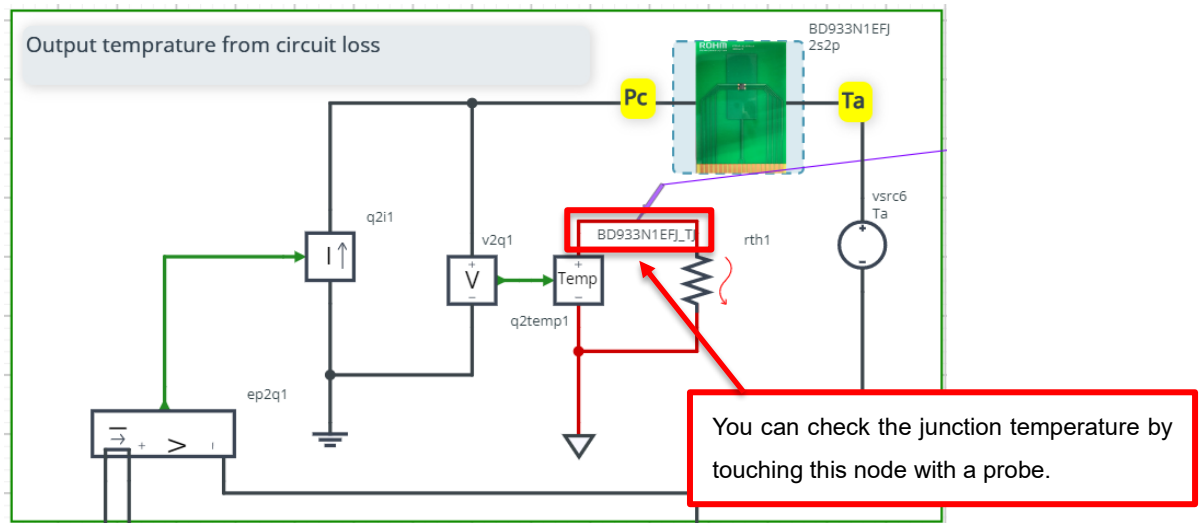


Figure 5. BD933N1EFJ-C thermal simulation model

Table 4. Terminal description of the thermal simulation model

| Terminal name | Description |
|---|---|
| Pc | Input for linear regulator loss |
| Ta | Ambient temperature |

### 3.3   Selecting a thermal simulation model

There are a number of thermal simulation models to choose from and their components are shown in Table 5. Figure 6 shows how to select one. First, right-click on the BD933N1EFJ component and select "Properties". In the "Property Editor", set the value of the "SpiceLib Part" to the name you selected from Table 5 to change the thermal simulation model. For more information on the board details for each model, see "3.4 Thermal simulation model board conditions".
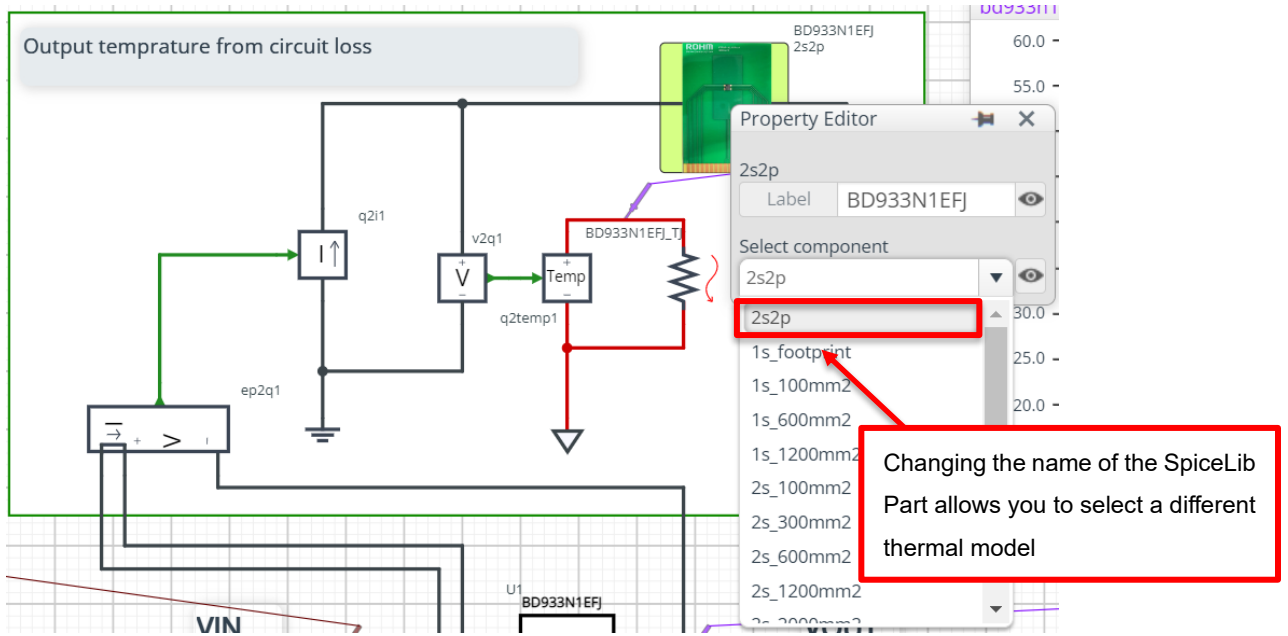


Figure 6. How to select a thermal simulation model

Table 5. List of available components

| Component name | SpiceLib Part name | Description |
|---|---|---|
| BD933N1EFJ | 1s_footprint | 1-layer board, surface layer Footprint only |
| | 1s_100mm2 | 1-layer board, surface layer copper foil surface area 100 mm$^2$ |
| | 1s_600mm2 | 1-layer board, surface layer copper foil surface area 600 mm$^2$ |
| | 1s_1200mm2 | 1-layer board, surface layer copper foil surface area 1,200 mm$^2$ |
| | 2s_100mm2 | 2-layer board, surface layer Footprint only, back layer copper foil surface area 100 mm$^2$ |
| | 2s_300mm2 | 2-layer board, surface layer Footprint only, back layer copper foil surface area 300 mm$^2$ |
| | 2s_600mm2 | 2-layer board, surface layer Footprint only, back layer copper foil surface area 600 mm$^2$ |
| | 2s_1200mm2 | 2-layer board, surface layer Footprint only, back layer copper foil surface area 1,200 mm$^2$ |
| | 2s_2000mm2 | 2-layer board, surface layer Footprint only, back layer copper foil surface area 2,000 mm$^2$ |
| | 2s_3000mm2 | 2-layer board, surface layer Footprint only, back layer copper foil surface area 3,000 mm$^2$ |
| | 2s_5500mm2 | 2-layer board, surface layer Footprint only, back layer copper foil surface area 5,500 mm$^2$ |
| | 2s2p | 4-layer board, surface layer Footprint only, other layers copper foil surface area 5,500 mm$^2$ |

### 3.4  Thermal simulation model board conditions (BD9xxN1EFJEFJ series)
### 1 layer (1s)

Conforms to JEDEC standard JESD51-3
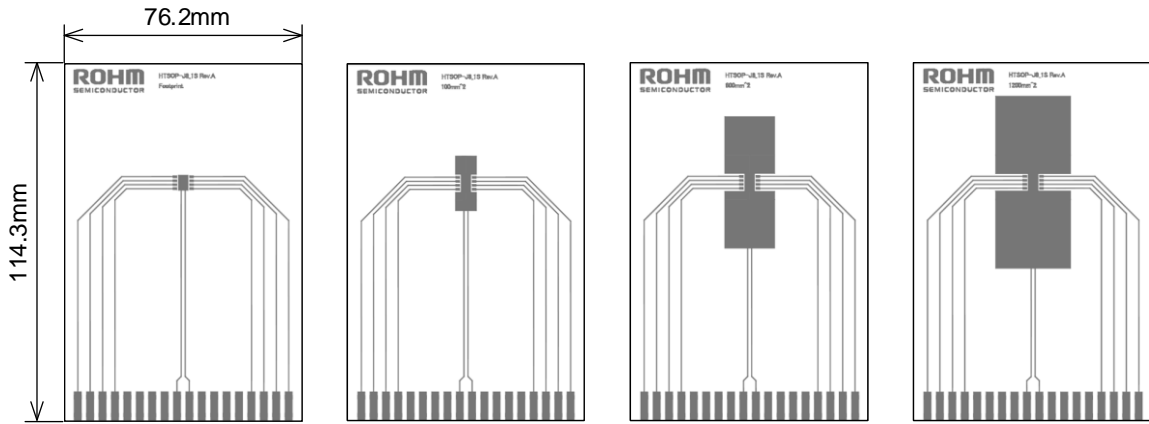


Copper foil area:  15.7mm²         100mm²            600mm²            1200mm²

(Footprint)

Figure 7. Top Layer Trace

Table 6. 1 layer PCB specifications

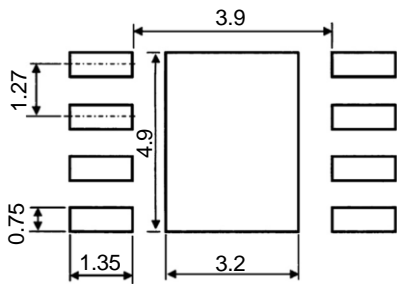| Item | Value |
|---|---|
| Board thickness | 1.57mm |
| Board outline dimensions | 76.2mm × 114.3mm |
| Board material | FR-4 |
| Trace thickness (Finished thickness) | 70µm (2 oz) |
| Lead width | 0.254mm |
| Copper foil area | Footprint, 100mm², 600mm², 1200mm² |



Figure 8. Footprint dimensions



Figure 9. Cross-section of 1 layer board

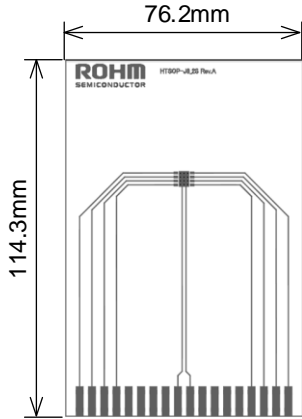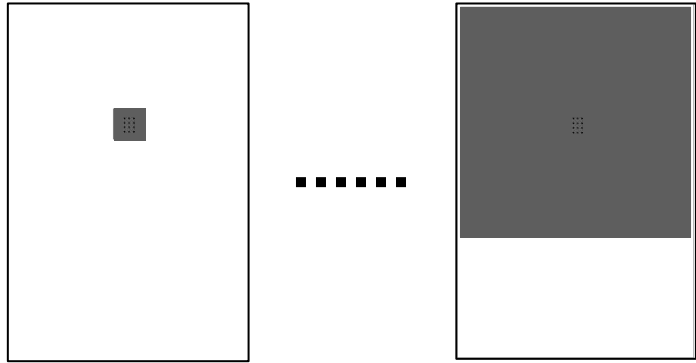## 2 layers (2s)
Conforms to JEDEC standard JESD51-5, JESD51-7



Figure 10. Top Layer Trace



Copper foil area: 100mm$^2$                5500mm$^2$

Figure 11. Bottom Layer Trace

Table 7. 2 layer PCB specifications

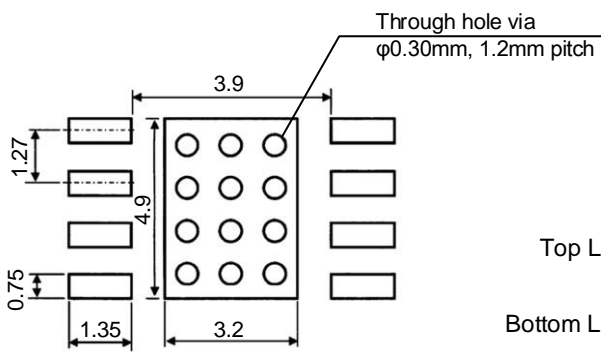| Item | | Value |
|---|---|---|
| Board thickness | | 1.60mm |
| Board outline dimensions | | 76.2mm × 114.3mm |
| Board material | | FR-4 |
| Trace thickness (Finished thickness) | Top | 70μm (2 oz) |
| | Bottom | 70μm (2 oz) |
| Lead width | | 0.254mm |
| Copper foil area | Top | Footprint |
| | Bottom | 100mm$^2$ ,300mm$^2$,  600mm$^2$,  1200mm$^2$,  2000mm$^2$,  3000mm$^2$, 5500mm$^2$ |



Figure 12. Footprint dimensions


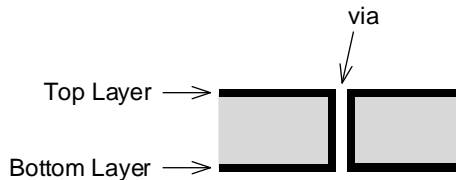
Figure 13. Cross-section of 2 layer board

## 4 layers (2s2p)

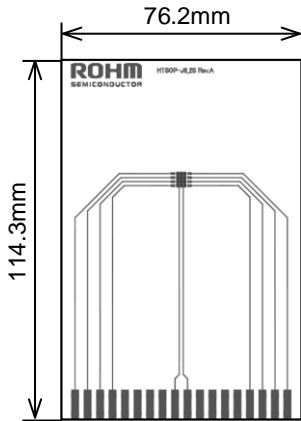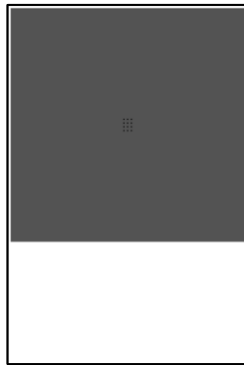Conforms to JEDEC standard JESD51-5, JESD51-7



| Figure 14. | Figure 15. | Figure 16. | Figure 17. |
|---|---|---|---|
| Top Layer Trace | Middle 1 Layer Trace | Middle 2 Layer Trace | Bottom Layer Trace |
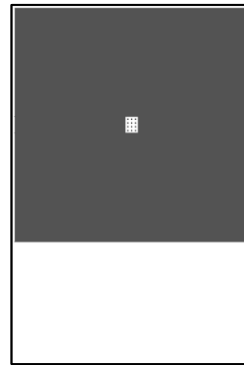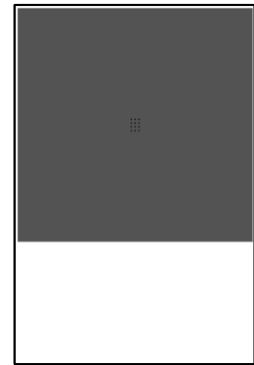
Table 8. 4 layer PCB specifications

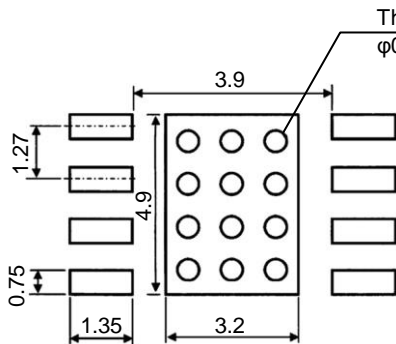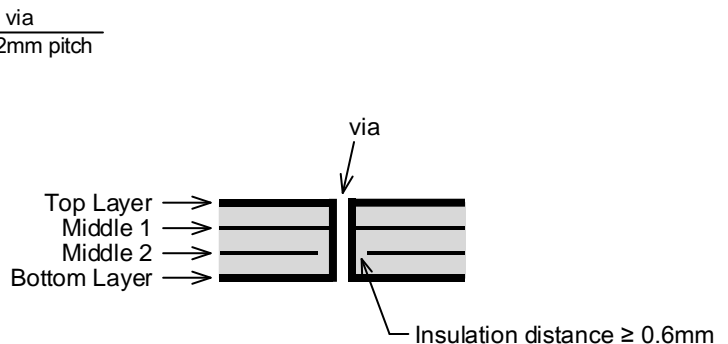| Item | | Value |
|---|---|---|
| Board thickness | | 1.60mm |
| Board outline dimensions | | 76.2mm × 114.3mm |
| Board material | | FR-4 |
| Trace thickness (Finished thickness) | Top | 70µm (2 oz) |
| | Middle 1 | 35µm (1 oz) |
| | Middle 2 | 35µm (1 oz) |
| | Bottom | 70µm (2 oz) |
| Lead width | | 0.254mm |
| Copper foil area | Top | Footprint |
| | Middle 1 | 5505mm$^2$ (74.2mm×74.2mm) |
| | Middle 2 | 5505mm$^2$ (74.2mm×74.2mm) |
| | Bottom | 5505mm$^2$ (74.2mm×74.2mm) |



Figure 18. Footprint dimensions

Figure 19. Cross-section of 4 layer board

## 4    Links to related documents

Products

BD933N1EFJ-C

BD950N1EFJ-C

BD933N1WEFJ-C

BD950N1WEFJ-C

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