Linear Regulator

EMC Measures for LDOs

Since LDOs feature low noise, they are not often focused regarding measures for electromagnetic compatibility (EMC). However, there are several points you should be aware of in order to avoid problems after mass production. This application note explains countermeasures for electromagnetic interference (EMI) and electromagnetic susceptibility (EMS) that require attention.

1. EMI

LDOs feature low noise and the IC itself produces no effective noise in terms of the EMI standards. As a result, EMI countermeasures tend to attract less attention. For example, when a digital circuit, such as a microcontroller unit (MCU), is connected as a load, the wiring of the power supply circuit may act as an antenna for radiation noise and the apparent LDO power block can be considered a noise source.

1-1. EMI source

The gate number of digital circuits varies from several tens of thousands of gates for microcontrollers to several tens of millions of gates for FPGAs. Every time a logic circuit is turned ON/OFF, the charge/discharge current flows to and from the gate capacitor (Figure 1). In addition, the through current flows transiently when the circuit is switched ON/OFF (Figure 2). The charge/discharge current and the through current flowing through each logic gate circuit are minute. However, since most logic circuits are configured as synchronized circuits, the currents are converged on the same time in synchronization with the clock. As a result, a large switching current appears in the power supply circuit (Figure 3).

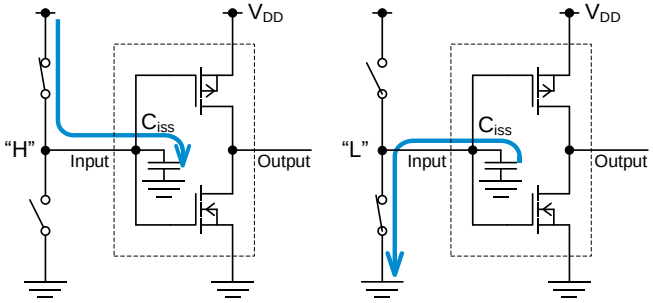

Figure 1. Charge/discharge current flows to and from the gate capacitor every time the logic gate circuit is turned ON/OFF.

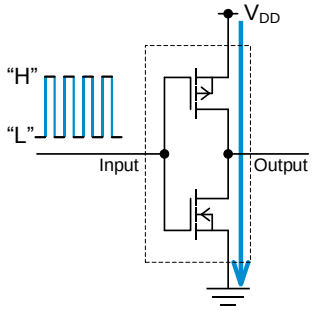

Figure 2. Through current flows transiently when the circuit is switched ON/OFF.

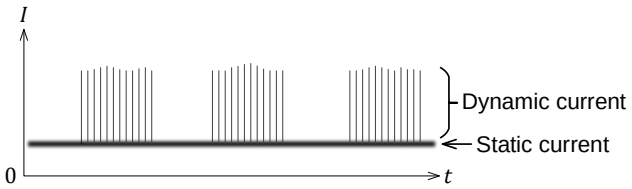

Figure 3. Image of current consumption waveform of digital circuit

This switching current is a high-frequency spike current that cannot be followed with the response speed of generic LDOs. Therefore, current is temporarily supplied from the output capacitor of the LDO (Figure 4). If the instantaneous current cannot be supplied from the output capacitor, the voltage supplied to the digital IC could drop momentarily, causing a malfunction. In addition, the static current flowing constantly is supplied from the power supply circuit in the previous stage through the LDO.

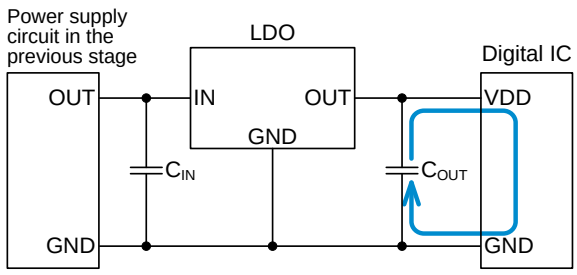

Figure 4. Current is temporarily supplied from the output capacitor of the LDO because the high-frequency switching current of the digital IC cannot be followed with the response speed of the LDO.

1-2. EMI countermeasures

In the circuit shown in Figure 4, the loop current is supplied from the output capacitor to the digital IC and then returned to the ground. Since the frequency of the loop current is high, the risk of EMI becomes higher as the area of the current loop is increased. Therefore, the circuit configuration and the PCB layout are designed with the main focus on decreasing the current loop.

Next, several possible EMI countermeasures are introduced.

1. Point of load (POL) configuration

Figure 5 shows an example of PCB layout. The loop of high-frequency current is decreased by placing the LDO immediately next to the digital IC in order to reduce the radiated emission due to the wiring acting as a loop antenna. By placing the LDO close to the load, the output capacitor of the LDO also serves as the decoupling capacitor of the digital IC.

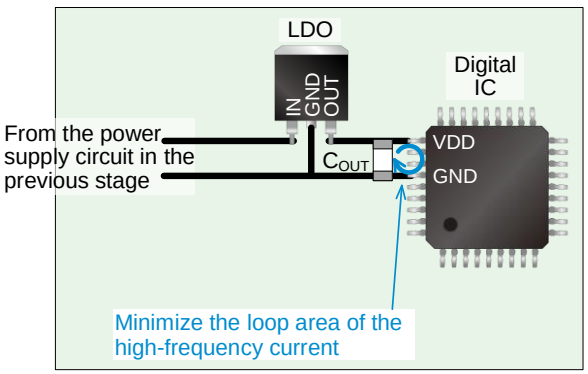

Figure 5. POL configuration with LDO placed immediately next to load

Since the capacitor used here must be able to follow the discharge of high-frequency current, a multi-layer ceramic capacitor (MLCC) with a low equivalent series resistance (ESR) less than several tens of mΩ is recommended. For electrolytic capacitors with a high ESR, the current could be limited due to the ESR, making it impossible to follow the discharge current. Therefore, the low ESR type must be selected.

For the capacitance of the capacitor, the amount of electric charge must be sufficient to supply the high-frequency current (dynamic current) of the digital IC. Care must be taken because EMI could exceed the limit values of the standards if only the capacitance values listed in the LDO data sheet are used in designing in order to reduce costs. The high-frequency spike current is affected by the parasitic inductance and varies with the PCB conditions. Therefore, it is difficult to determine the capacitance values with calculations. Refer to the capacitance values listed in the data sheet of the digital IC.

Figure 6 shows an example in which the capacitors with the best capacitance values for different frequency bandwidths are placed in parallel. Although capacitors with a smaller capacitance value are more effective at a higher frequency, they are more susceptible to the parasitic inductance. Therefore, minimize the loop area of the high-frequency current by placing the capacitors immediately next to the digital IC in such an order that a capacitor with a smaller value is placed closer to the digital IC.

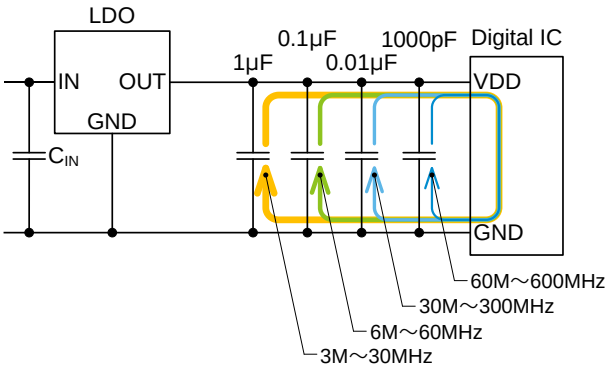

Figure 6. Example in which the capacitors with the best capacitances for different frequency bandwidths are placed in parallel
The frequency bandwidths are shown as a rough guide.

While the copper foil thickness has little influence on the wiring inductance, its length and width affect the inductance (see Appendix A). To reduce the influence of the parasitic inductance, possible countermeasures include decreasing the wiring length between the digital IC and the capacitors as well as increasing the wiring width.

There is also an inductance for vias (see Appendix B). Although the value is small at around 1 nH, the wiring bending at a right angle changes the impedance, disturbing the current waveforms and causing reflections. Since the inductance affects frequencies in the UHF band (approximately 300 MHz) and higher, place the capacitors on the same plane as the digital IC without passing through vias.

In addition, be sure to check the effect of countermeasures with simulations and actual equipment.

2. If the LDO and the digital IC are placed apart

It may be impossible to place the LDO close to the digital IC due to constraints of the PCB layout. As shown in the circuit diagram in Figure 7, if decoupling capacitor C1 of the digital IC does not have a capacitance (amount of electric charge) sufficient to supply the high-frequency current, the current is supplied from the output capacitor of the LDO, producing a large loop of high-frequency current. This loop wiring can act as an antenna, increasing the radiated emission.

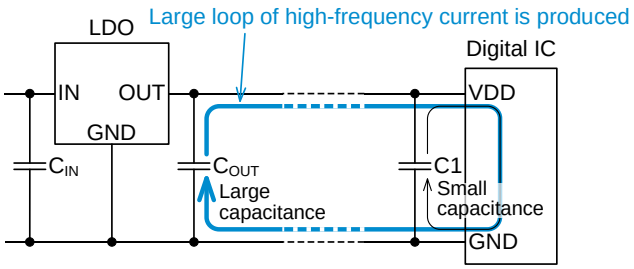

Figure 7. Large current loop is produced if the LDO and the digital IC are placed apart and the decoupling capacitor of the digital IC has an insufficient capacitance.

Figure 8 shows a countermeasure. Similarly to the POL configuration described above, the radiated emission due to the wiring acting as a loop antenna can be reduced by placing low ESR capacitor C1 with an amount of electric charge sufficient to supply the high-frequency current of the digital IC immediately next to the digital IC to minimize the loop area of the high-frequency current. In this case, since C_{OUT} is the phase compensation capacitor of the LDO, comply with the minimum value recommended in the data sheet for the capacitance value and place the capacitor immediately next to the LDO.

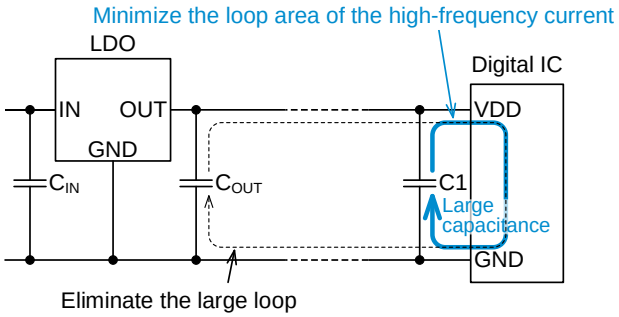

Figure 8. Loop area of the high-frequency current is minimized by placing a low ESR capacitor with an amount of electric charge sufficient to supply the high-frequency current of the digital IC immediately next to the digital IC.

3. LDOs with excellent load response characteristics

For LDOs with excellent load response characteristics, the capacitance of the output capacitor can be decreased compared with conventional LDOs. In addition, since their load response performance is improved, they can follow the high-frequency current of the digital IC as well. As a result, there is a point to pay attention to in terms of EMI.

Figure 9 shows a circuit diagram in which an LDO with excellent load response characteristics is placed in the POL configuration against the digital IC. In this example, an output capacitor with 0.1 µF is connected and the LDO will operate correctly as a voltage regulator.

The flow of the high-frequency current of the digital IC here shows that the current loop is extended to the input side of the LDO as indicated with a blue arrow because the LDO follows the load response. As a result, there is a concern that the radiated emission may be exacerbated due to this loop wiring acting as an antenna. If the amount of electric charge of the input capacitor of the LDO is insufficient against the high-frequency current, the current loop area is further increased because the current is supplied from the capacitor of the power supply circuit in the previous stage.

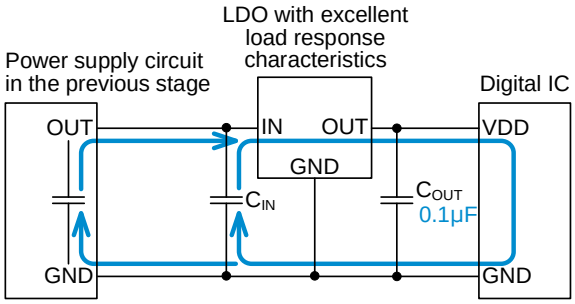

Figure 9. Circuit diagram in which LDO with excellent load response characteristics is placed in POL configuration against digital IC

If the capacitance of the output capacitor is small, there is a concern that EMI may be exacerbated because the high-frequency current is propagated to the input side.

As a countermeasure, similarly to the POL configuration described above, the radiated emission due to the wiring acting as a loop antenna can be reduced by placing a low ESR capacitor with an amount of electric charge sufficient to supply the high-frequency current of the digital IC immediately next to the digital IC to minimize the loop area of the high-frequency current (Figure 10).

If you prefer not to increase the capacitance of C_{OUT}, depending on the frequency bandwidth of the digital noise, it may also be possible to cut the bandwidth of the supply current from the power supply circuit in the previous stage by inserting a ferrite bead or inductor as shown in Figure 11. In this case, the input capacitor serves as a temporary power supply that can compensate for the shortage if the power supply circuit in the previous stage cannot supply a large transient current in time. Therefore, connect a capacitor with an amount of electric charge sufficient to supply the temporary load current.

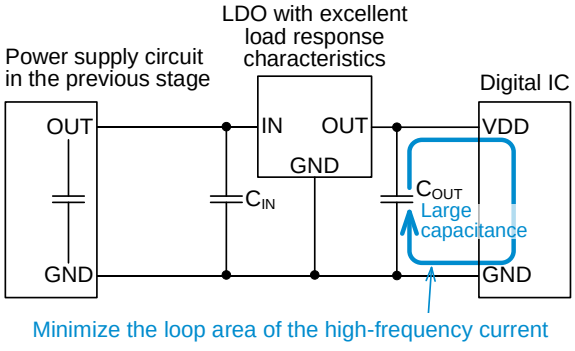

Figure 10. Loop area of the high-frequency current is minimized by placing a low ESR capacitor with an amount of electric charge sufficient to supply the high-frequency current of the digital IC immediately next to the digital IC.

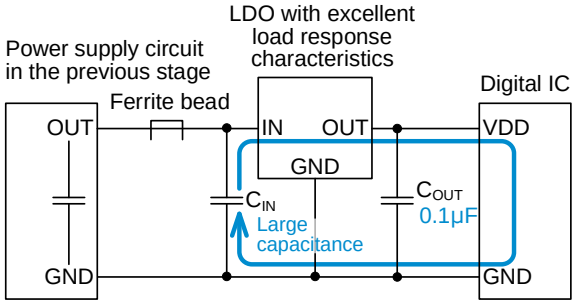

Figure 11. Depending on the frequency bandwidth of the digital noise, it may also be possible to cut the bandwidth of the supply current from the power supply circuit in the previous stage with a ferrite bead as an EMI countermeasure for the current loop from the input capacitor.

As described above, the LDO products with excellent load response characteristics can maintain the stable operation and the load responsiveness even if the capacitance of the output capacitor is decreased. However, it may be necessary to adjust the input and output capacitances depending on the load requirement. It is also effective to provide the PCB with lands for adjusting the capacitance in advance.

2. EMS countermeasures

For EMS, it is difficult to determine what kind of noise enters from where. Therefore, first predict or check the type of electromagnetic noise and the location it enters before taking countermeasures. The following two cases are possible for LDOs.

2-1. Electrostatic discharge (ESD)

If the LDO output is directly connected with the plug, such as in AC adapters, or if the power supply jack of an electronic device is directly connected to the LDO input, static electricity enters the LDO because it is touched by the human body. The electrostatic testing must be passed according to the EMS standards, including IEC 61000-4-2 and ISO 10605.

Figure 12 shows an example of EMS countermeasures for the AC adapter output and the power supply jack of an electronic device. Generally, ESD is prevented from entering the PCB by placing TVS diodes on the input and output parts of the devices to clamp the surge pulse voltage.

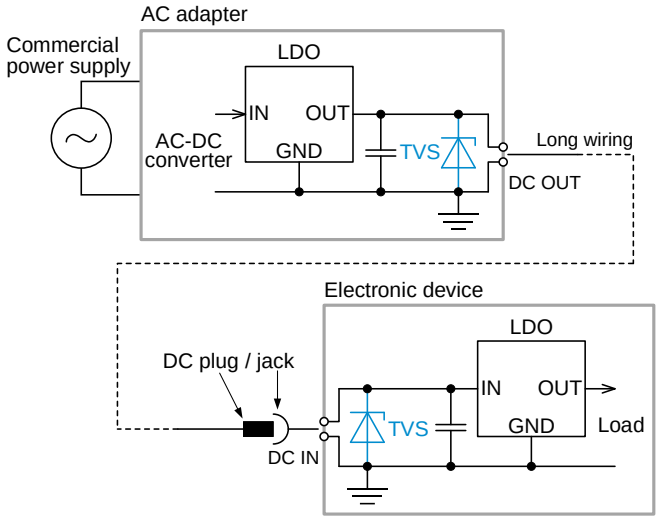

Figure 12. Example of EMS countermeasures for AC adapter output and power supply jack of electronic device

Figure 13 shows an example of PCB layout for the TVS diode. This PCB layout is important. Since ESD enters through the I/O connector in many applications, the TVS diode is placed immediately next to the entry source to prevent ESD from entering the PCB. In addition, it is necessary to minimize the parasitic inductance component by decreasing the wiring length between the anode (ground) and cathode (hot) sides of the diode. If the parasitic inductance is large, the performance of the TVS diode cannot be delivered because the ESD clamping voltage is increased.

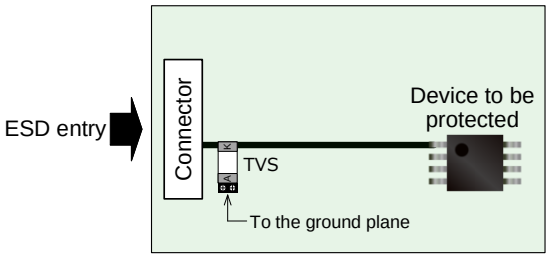

Figure 13. Example of PCB layout for TVS diode
Place the TVS diode immediately next to the ESD entry source to prevent ESD from entering the PCB. In addition, minimize the parasitic inductance component by decreasing the wiring length between the anode (ground) and cathode (hot) sides.

For details on TVS diodes, refer to the following application notes.

[Application Note]

- Selection Method and Usage of TVS Diodes
- PCB Layout for TVS Diodes

2-2. Radiated electromagnetic field

As a consequence of an electronic device being exposed to an electromagnetic wave, such as communication and broadcast waves, the electromagnetic wave may directly reach the PCB wiring. When the LDO input is directly connected with an automotive battery, the electromagnetic wave may also reach the long cable between them. If the length of the PCB wiring or the cable is equal to, a half of, or a quarter of the wavelength of the electromagnetic wave, the wiring or the cable serves as an antenna to receive the neighborhood frequency. In addition, the wiring impedance of specific parts is increased at a frequency where a parallel resonance occurs between the wiring inductance and the parasitic capacitance, making such parts susceptible to the electromagnetic wave. Since such parts exist innumerably on a PCB and inside an electronic device, there is no way other than using an electromagnetic field simulator to find the susceptible parts.

However, in most cases, if EMI countermeasures are taken to suppress the exiting electromagnetic field noise for a finished product with a built-in power supply, it can also be expected that the entering electromagnetic field noise is also suppressed.

To avoid the effects of an unexpected radiated electromagnetic field, it is recommended to add land patterns so that capacitors can be added on the input and output sides of the LDO. This addition could solve the problem by shifting the resonance frequency. As indicated by the example in Figure 14, for electromagnetic waves in the GHz band, place MLCCs with several tens of pF immediately next to the IC pins to minimize the influence of the wiring inductance. Then, place capacitors farther from the IC as the capacitance is increased (against a lower frequency).

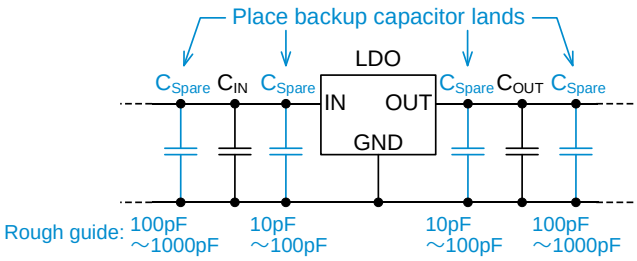

Figure 14. Prepare for EMS countermeasures by placing backup capacitor lands on the input and output sides of the LDO.

Appendix A. Inductance of copper foil wiring

The inductance of the copper foil wiring can be expressed with Equation (A-1). Figures A-1 and A-2 show calculation examples. For the PCB wiring, the copper foil thickness is small and has little influence on the inductance value. The wiring inductance can be decreased by decreasing the wiring length or increasing the wiring width. However, decreasing the length is more effective than increasing the width.

$$L = 0.2\,l\left(\ln\frac{2\,l}{w+t} + 0.2235\frac{w+t}{l} + 0.5\right) \quad [nH] \qquad \text{(A-1)}$$

l : Conductor length $[mm]$

w : Conductor width $[mm]$

t : Copper foil thickness $[mm]$

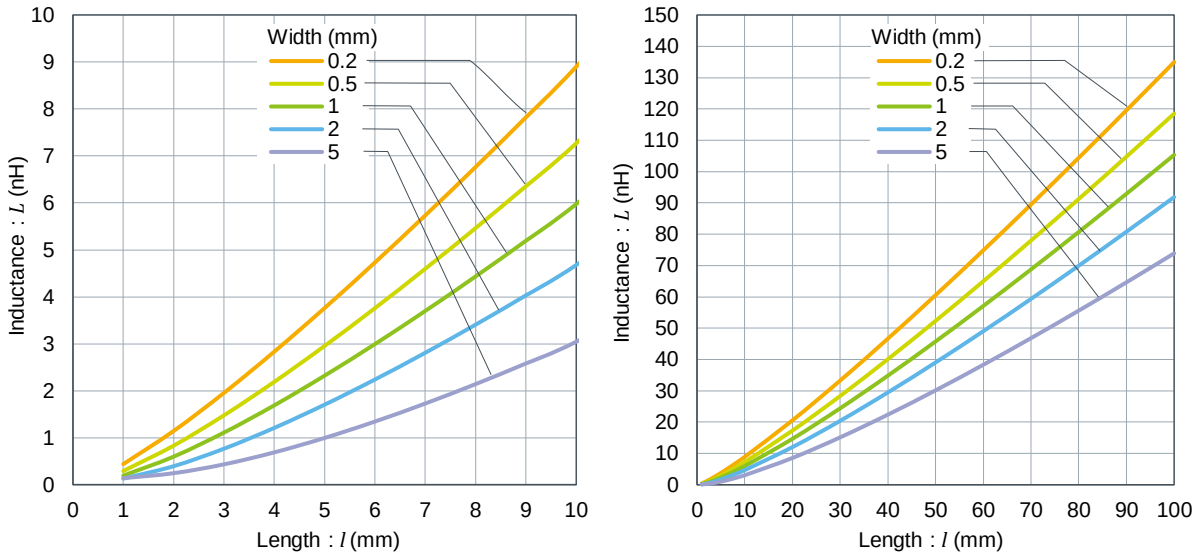

Figure A-1. Inductance of copper foil wiring: t = 0.035 mm

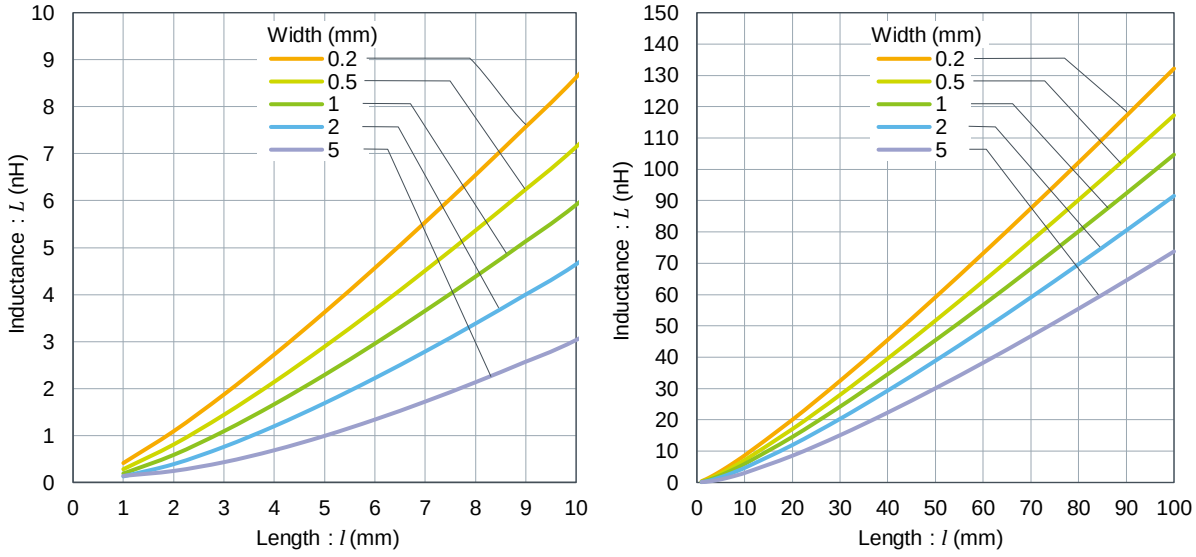

Figure A-2. Inductance of copper foil wiring: t = 0.07 mm

Appendix B. Via inductance

According to Howard W. Johnson[1], the via inductance can be expressed with Equation (B-1). Figure B-1 shows the calculation results. The via height can be estimated as the board thickness.

$$L = 0.2\,h\left(\ln\frac{4\,h}{d}+1\right)\quad [nH] \qquad \text{(B-1)}$$

h : Via height $[mm]$
d : Via diameter $[mm]$

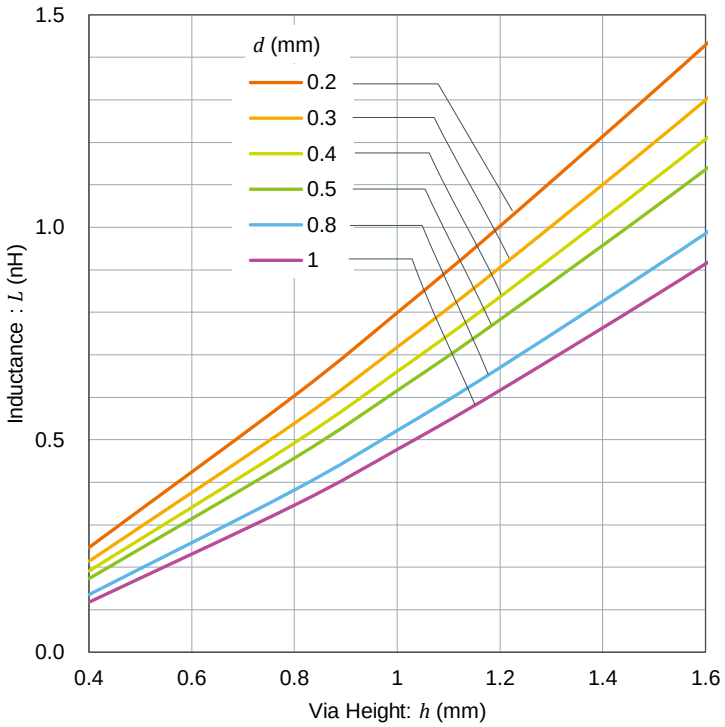

Figure B-1. Via inductance

References:

[1] Howard W. Johnson, Martin Graham, High-Speed Digital Design: A Handbook of Black Magic (1993)

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