Linear Regulator Series

Thermal Calculation for Linear Regulator

The loss in linear regulators increases as the difference between the input and output voltages increases. Since most of the loss is converted to heat, a very large amount of heat may be generated in some conditions. To utilize linear regulators effectively at several watts or more, it is always necessary to consider the issue of heat. The temperature increases above the maximum rating for the junction temperature of the IC chip, making it impossible to achieve the target output current. This application note explains how to estimate the junction temperature of the IC chip, and provides calculation examples for the ROHM's standard circuit boards.

Thermal calculation requires information on the IC loss power, the thermal resistance or thermal characteristics parameter of the package, the ambient temperature, and the temperature at the center of the package surface. From these values, the junction temperature of the IC chip is estimated to confirm that the temperature is below the absolute maximum rating.

IC power loss P

Figure 1 shows the circuit diagram of a linear regulator. Under this condition, the IC power loss can be calculated with the following equation.

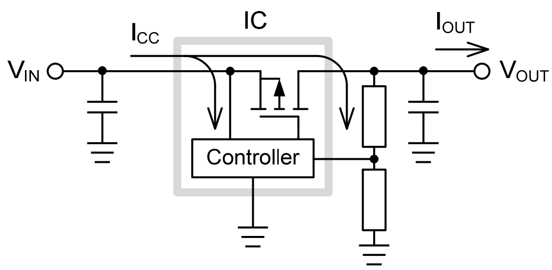

Figure 1. Circuit diagram of linear regulator

$$P = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{CC} \quad [W] \qquad (1)$$

V_{IN} : Input voltage [V]
V_{OUT} : Output voltage [V]
I_{OUT} : Output current [A]
I_{CC} : Circuit current [A]

The power loss is the sum of the product of the difference between the input and output voltage multiplied by the output current and the consumption power of the IC.

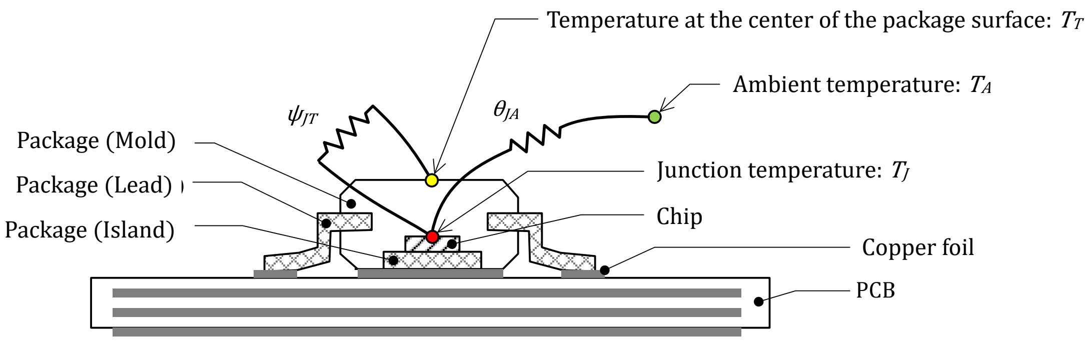

Figure 2. Definitions of thermal resistance θ_{JA} and thermal characteristics parameter Ψ_{JT}

Thermal resistance θ_{JA} and thermal characteristics parameter Ψ_{JT}

Figure 2 shows the definitions of the thermal resistance θ_{JA} and the thermal characteristics parameter Ψ_{JT}. θ_{JA} is the thermal resistance between the junction temperature T_J and the ambient temperature T_A. The JEDEC JESD51 standard specifies that the ambient temperature T_A is the atmospheric temperature at a location where the measuring part has no effect and that is outside the boundary layer of the heat generating source. Since heat radiation occurs via multiple thermal pathways, θ_{JA} is subject to the surrounding conditions, including the structure of the circuit board and other heat generating sources. In addition, it is difficult to define T_A in an equipment chassis with little space. Therefore, it is desirable to use θ_{JA} for the comparative assessment of the heat radiation performance among packages with different shapes.

ψ_{JT} is the thermal characteristics parameter describing the difference between the junction temperature T_J and the temperature at the center of the package surface T_T for the loss power P of the entire device. Although ψ_{JT} is also affected by the structure of the circuit board, you can use a representative value for similar conditions since the change is smaller compared with θ_{JA}. JEDEC recommends that T_J be estimated with a ψ_{JT} value that uses the total heat flow (power loss) as a parameter.
The values of θ_{JA} and ψ_{JT} can be referenced from the data sheet or obtained from the manufacturer.

Ambient temperature T_A and the temperature at the center of the package surface T_T

As mentioned above, the JEDEC JESD51 standard specifies that the ambient temperature T_A is the atmospheric temperature at a location where the measuring part has no effect and that is outside the boundary layer of the heat generating source. The measurement environments specified in JESD51 are shown in Figures 3 to 5.

Two methods are available for measuring the temperature at the center of the package surface T_T: measurement with the thermocouple in contact with the IC and non-contact measurement with a radiation thermometer (thermography). Although radiation thermometers provide a convenient measurement method, the measured values may vary depending on the emissivity setting. The measurement error may also become larger for small shaped objects like ICs since the measurement circle of the radiation thermometer is large (making the measured temperature lower).

The measurement error in the thermocouple measurement may also be large depending on the fixing method. However, the temperature can be measured precisely by fixing the thermocouple correctly.

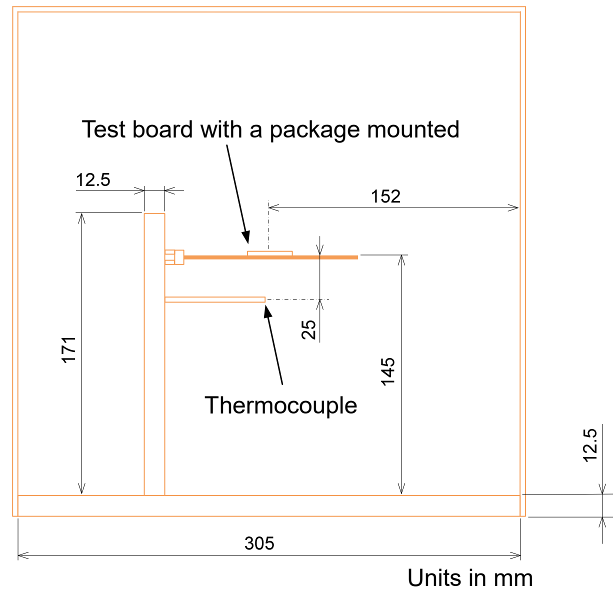

Figure 3. Side view of test equipment and chassis (JESD51-2A)

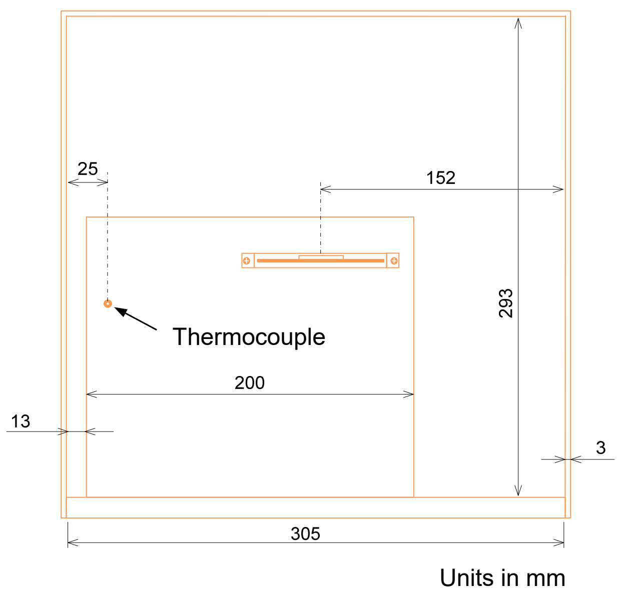

Figure 4. End view of test equipment and chassis (JESD51-2A)

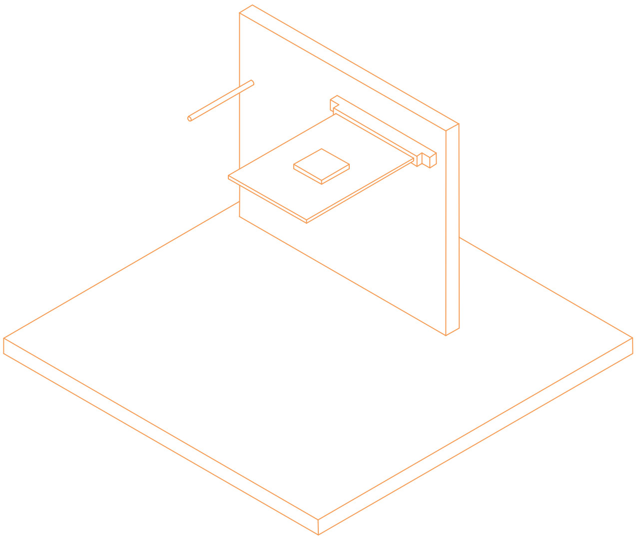

Figure 5. Isometric view of fixture and test board without chassis (JESD51-2A)

Estimation of junction temperature T_J

The major premise of the IC design is that the junction temperature T_J must be no more than the absolute maximum rating for the junction temperature T_{Jmax}. Any operation above this value results in deterioration of the IC lifetime, performance, and reliability. For the absolute maximum rating for the junction temperature T_{Jmax} refer to the IC data sheet.

The junction temperature T_J can be estimated with the following two methods.

1. Determined from the ambient temperature T_A and the thermal resistance θ_{JA} with the following equation.

$$T_J = T_A + \theta_{JA} \times P \quad [°C] \qquad (2)$$

T_A : Ambient temperature [°C]

θ_{JA} : Thermal resistance between T_J and T_A [°C/W]

P : IC power loss [W]

Calculation example 1

Conditions:

Input voltage V_{IN}: 12 V

Output voltage V_{OUT}: 5 V

Output current I_{OUT}: 0.3 A

Circuit current I_{CC}: 0.6 mA

Package: TO252-3

Circuit board: FR-4, 4 layers

Ambient temperature T_A: 60°C

Result:

From Equation (1), the IC loss power *P* is calculated as follows:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{CC}$$
$$= (12 - 5) \times 0.3 + 12 \times 0.6 \times 10^{-3} = 2.107 \ [W]$$

The TO252-3 package has a θ_{JA} value of 23.3°C/W.

From Equation (2), the junction temperature T_J is calculated as follows:

$$T_J = T_A + \theta_{JA} \times P = 60 + 23.3 \times 2.107 = 109.1 \ [°C]$$

2. Determined from the temperature at the center of the IC package surface during actual use T_T and the thermal characteristics parameter ψ_{JT} with the following equation.

$$T_J = T_T + \psi_{JT} \times P \quad [°C] \qquad (3)$$

T_T : Temperature at the center of the package surface [°C]

ψ_{JT} : Thermal characteristics parameter between T_J and T_T [°C/W]

P : IC power loss [W]

Calculation example 2

Conditions:

Input voltage V_{IN}: 12 V

Output voltage V_{OUT}: 5 V

Output current I_{OUT}: 0.3 A

Circuit current I_{CC}: 0.6 mA

Package: TO252-3

Circuit board: FR-4, 4 layers

Measured T_T during actual use: 105°C

Result:

From Equation (1), the IC loss power *P* is calculated as follows:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{CC}$$
$$= (12 - 5) \times 0.3 + 12 \times 0.6 \times 10^{-3} = 2.107 \ [W]$$

The TO252-3 package has a ψ_{JT} value of 2°C/W.

From Equation (3), the junction temperature T_J is calculated as follows:

$$T_J = T_T + \psi_{JT} \times P = 105 + 2 \times 2.107 = 109.2\ [°C]$$

Estimation of T_J on inrush current occurs

At startup, an inrush current flows into the output capacitor. For example, suppose that an inrush current of 1 A flows for 1 ms under the conditions of calculation example 1. If Equation (1) is used in this case, the loss power is determined as follows:

$$P = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{CC}$$
$$= (12 - 5) \times 1 + 12 \times 0.6 \times 10^{-3} = 7.007\ [W]$$

The junction temperature is calculated as follows:

$$T_J = T_A + \theta_{JA} \times P = 60 + 23.3 \times 7.007 = 223.3\ [°C]$$

This calculation result shows that the junction temperature will exceed the absolute maximum rating of 150°C, and therefore, the linear regulator will not be usable. However, this calculation method is applicable to a steady state only.

When an inrush current occurs or the loss power increases transiently, the temperature increase is calculated with the transient thermal resistance Z_{TH}. Figure 6 shows the transient thermal resistance data of the TO252-3 package. For the example above, to calculate the temperature within 1 ms, the transient thermal resistance Z_{TH} is read to be 2.2 $°C/W$ at 1 ms from Figure 6. Using this value, the junction temperature is calculated as follows:

$$T_J = T_A + Z_{TH} \times P = 60 + 2.2 \times 7.007 = 75.4\ [°C]$$

This calculation result indicates no problem with the junction temperature.

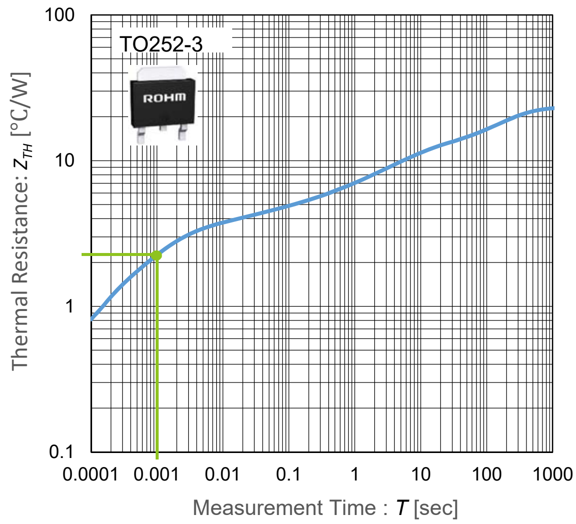

Figure 6. Transient thermal resistance of the TO252-3 package

Tips for better heat radiation efficiency

Figure 7 shows the result of the simulation for the thermal resistance θ_{JA} while varying the thickness of the copper foil of the circuit board. It is found that the thermal resistance is reduced as the thickness of the copper foil is increased. The effect of increasing the thickness of the copper foil diminishes if the thickness is 70 µm (= 2 oz) or more.

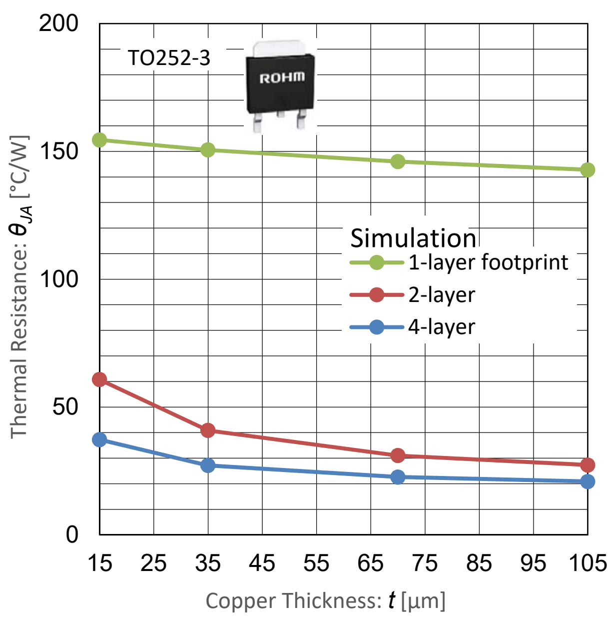

Figure 7. Thermal resistance vs. the thickness of the copper foil

Figure 8 shows the result of the simulation for the thermal resistance θ_{JA} while varying the number of layers of the circuit board. The thermal resistance tends to be smaller with a larger number of layers. When a via contact is placed directly under the exposed pad, the effect of reducing the thermal resistance is found to be large.

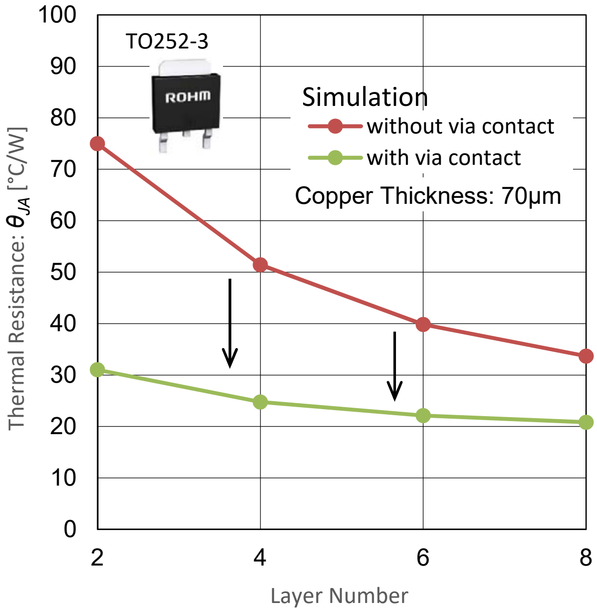

Figure 8. Thermal resistance vs. the number of layers of the circuit board

Notes for PCB layout

To improve the heat radiation of the IC, it is necessary to decrease the thermal resistance of the package. For this purpose, the required area for heat radiation is estimated and used as a reference for the layout.

The required area for heat radiation is estimated from the plot of θ_{JA} versus the thickness of the copper foil. Figure 9 shows an example for the TO252-3 package.

Calculation example 3

Conditions:

IC loss power P: 1.5 W

Package: TO252-3

Circuit board: FR-4, 2 layers

Ambient temperature T_A: 60°C

Target junction temperature T_J: 120°C

Result

The following result is obtained by transforming Equation (2) to express θ_{JA} and assigning the above conditions.

$$T_J = T_A + \theta_{JA} \times P \quad [°\mathrm{C}]$$

$$\theta_{JA} = \frac{T_J - T_A}{P} \quad [°\mathrm{C}/W]$$

$$= \frac{120-60}{1.5} = 40.0 \quad [°\mathrm{C}/W]$$

From Figure 9, the area of the copper foil is read to be approximately 1,500 mm^2 at the thermal resistance of 40°C/W. Design the layout based on the estimated minimum value of the required area for heat radiation.

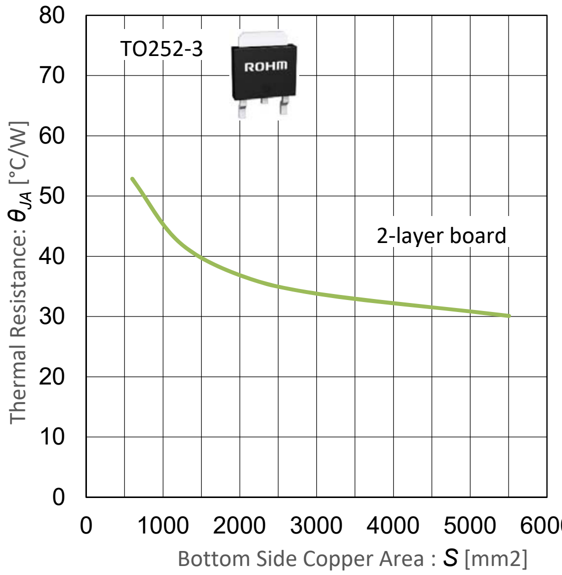

Figure 9. Thermal resistance vs. the area of the copper foil

For the packages that require the back surface heat radiation, the thermal resistance can be minimized by providing a via contact directly under the exposed pad and releasing heat to the back surface of the circuit board (Figure 10, lower left). If the limitations of the mount specifications prevent the arrangement of a via contact directly under the exposed pad during mass production, a via contact can be placed on a location adjacent to the IC. In this case, the thermal resistance is higher compared to the former arrangement (Figure 10, lower right).

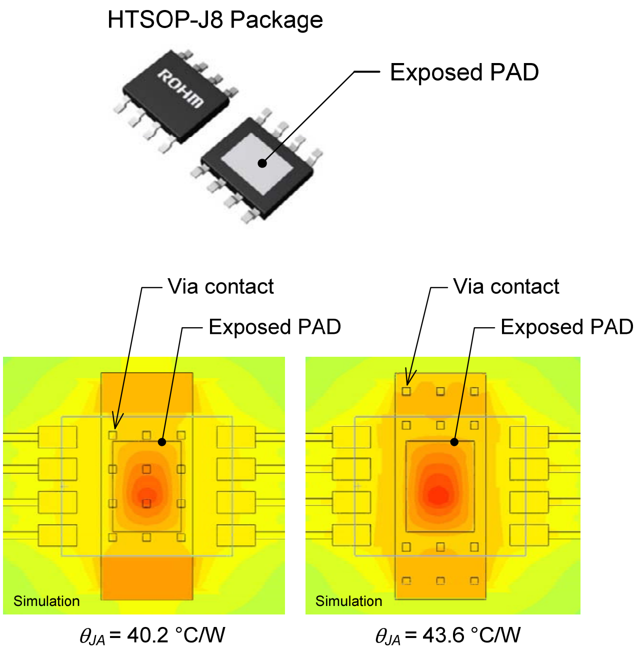

Figure 10. Difference in thermal resistance between different locations of the via contact

Accurate thermal evaluation

The thermal resistance, the thermal characteristics parameter, and the simulation values described in this application note are examples used under specific conditions. These values are only intended as data for explaining the thermal estimation methods. The thermal characteristics are affected by many parameters including the type of the circuit board, the layout arrangement, and the chassis shape. Please recognize that the thermal resistance and thermal characteristics parameter in the finished product state are required to obtain an accurate thermal evaluation.

References

(1) EIA/JESD51-1, Integrated Circuits Thermal Measurement Method – Electrical Test Method (Single Semiconductor Device), 1995

(2) JESD51-2A, Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air), 1995-2008

(3) EIA/JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages, 1996

(4) JESD51-5, Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms, 1999

(5) JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages, 1999

(6) JESD51-9, Test Boards for Area Array Surface Mount Package Thermal Measurements, 2000

(7) JESD51-10, Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements, 2000

(8) JESD51-13, Glossary of Thermal Measurement Terms and Definitions, 2009

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