

Linear Regulator Series

Thermal Resistance Data: SSOP5

BUxxJA2DG-C, BUxxJA2VG-C Series

This application note provides the thermal resistance data of the SSOP5 package used for the thermal design of the BUxxJA2DG-C and BUxxJA2VG-C series linear regulator IC.

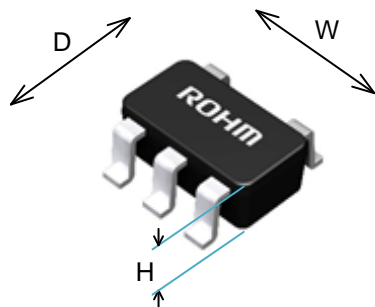
IC summary

The BUxxJA2DG-C and BUxxJA2VG-C series are high-performance CMOS LDO regulators with output current ability of up to 200mA. The SSOP5 package can contribute to the downsizing of the set. These devices have excellent noise and load response characteristics despite of its low circuit current consumption of 33 μ A. They are most appropriate for various applications such as power supplies for radar modules and camera modules.

- Operating temperature range: -40°C to +125°C
- Input voltage range: 1.7 V to 6.0 V
- Quiescent current: 33 μ A
- Output current: 200 mA
- Output voltage lineup: 1.0 V to 3.3 V
- Output voltage precision: \pm 2%

See Datasheet for more details.

Package



SSOP5

W (typ) D (typ) H (max)

2.9 mm x 2.8 mm x 1.25 mm

Measurement environment

| Content | Standard |
|----------------------------|---|
| Measurement environment | JEDEC STANDARD JESD51-2A (Still Air) |
| Measurement board standard | JEDEC STANDARD JESD51-3 JESD51-5 |

Thermal resistance

| Configuration | θ_{JA} (°C/W) | Ψ_{JT} (°C/W) |
|---------------|----------------------|--------------------|
| 1 layer | 260.7 | 44 |
| 2 layers | 178.8 | 32 |
| 4 layers | 135.1 | 30 |

θ_{JA} : Thermal resistance between
junction T_J - ambient temperature T_A

Ψ_{JT} : Thermal characteristics parameter between
junction T_J - package surface center temperature T_T

Note: The thermal resistances and thermal characteristics parameters in this application note are based on measurement under a JEDEC environment and may not always be consistent with the values for actual equipment. It is necessary to consider variations in the values due to the PCB characteristics, PCB layout, parts layout, chassis shape, surrounding environment, and so on.

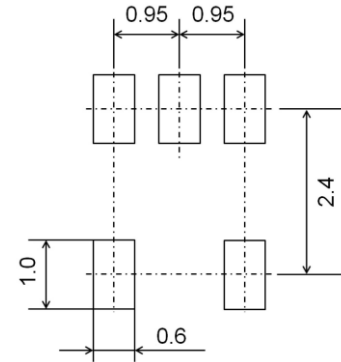
PCB specifications, 1 layer (1s)

Conforms to JEDEC standard JESD51-3

| Item | Value |
|--------------------------|--|
| Board thickness | 1.57 mm |
| Board outline dimensions | 76.2 mm x 114.3 mm |
| Board material | FR-4 |
| Copper foil thickness | 70 μm (2 oz copper foil) |
| Lead width | 0.254 mm |
| Copper foil area | Footprint (1.2 mm ²) [50 mm ² , 100 mm ² , 300 mm ² , 600 mm ²] |



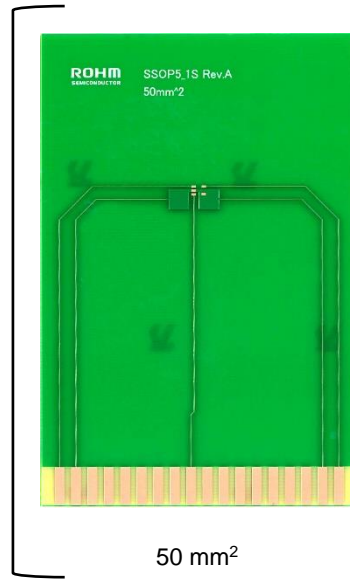
1 layer board sectional view



Footprint dimensions



Copper foil surface area: Footprint (1.2 mm²)



50 mm²



100 mm²



300 mm²

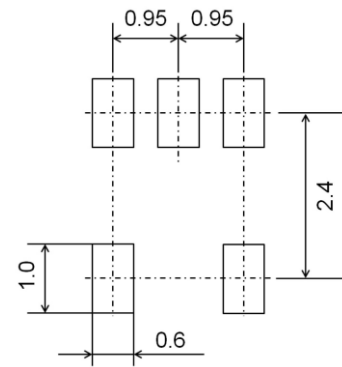
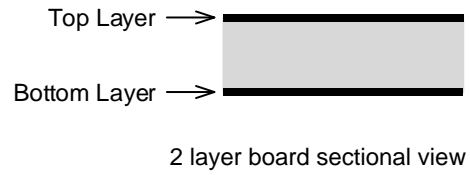


600 mm²

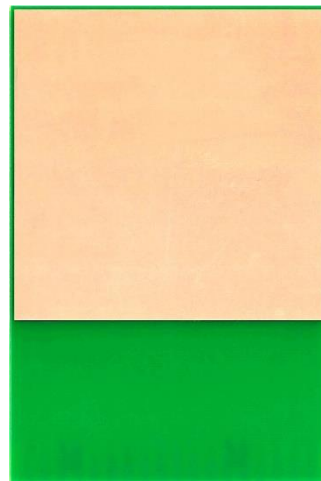
PCB specifications, 2 layers (2s)

Conforms to JEDEC standard JESD51-5

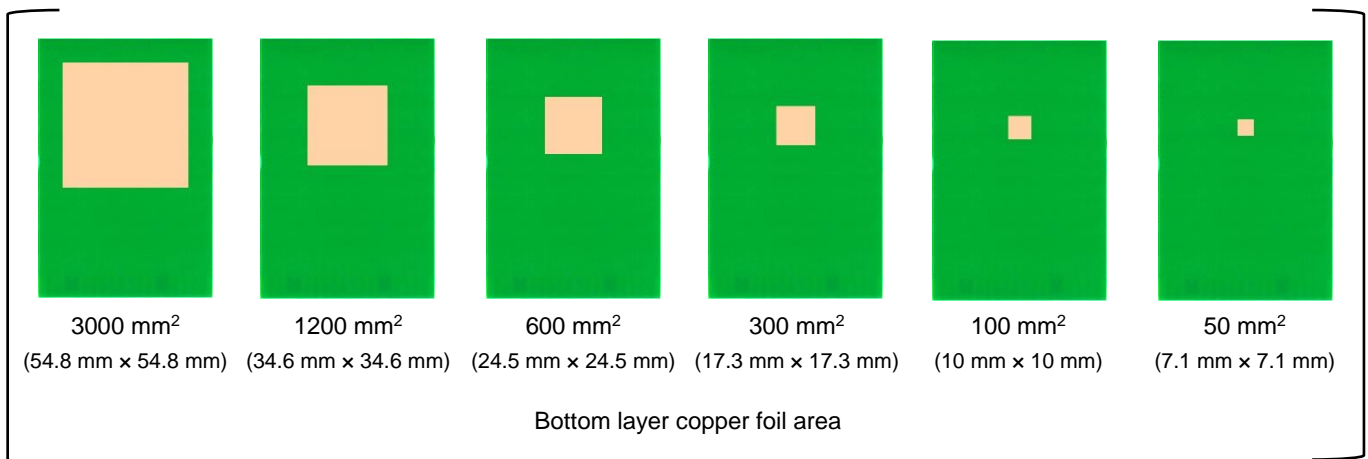
| Item | | Value |
|--------------------------|--------|---|
| Board thickness | | 1.60 mm |
| Board outline dimensions | | 76.2 mm × 114.3 mm |
| Board material | | FR-4 |
| Copper foil thickness | Top | 70 μm (1 oz copper foil + plating) |
| | Bottom | 70 μm (1 oz copper foil + plating) |
| Lead width | | 0.254 mm |
| Copper foil area | Top | Footprint (1.2 mm ²) |
| | Bottom | 5505 mm ² [50 mm ² , 100 mm ² , 300 mm ² , 600 mm ² , 1200 mm ² , 3000 mm ²] |



Top layer copper foil area
Footprint (1.2 mm²)



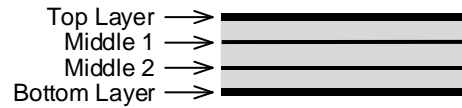
Bottom layer copper foil area
5505 mm²
(74.2 mm × 74.2 mm)



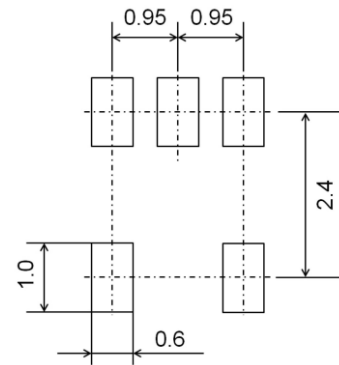
PCB specifications, 4 layers (2s2p)

Conforms to JEDEC standard JESD51-5

| Item | | Value |
|--------------------------|----------|--|
| Board thickness | | 1.60 mm |
| Board outline dimensions | | 76.2 mm × 114.3 mm |
| Board material | | FR-4 |
| Copper foil thickness | Top | 70 μm (1 oz copper foil + plating) |
| | Middle 1 | 35 μm (oz copper foil) |
| | Middle 2 | 35 μm (oz copper foil) |
| | Bottom | 70 μm (1 oz copper foil + plating) |
| Lead width | | 0.254 mm |
| Copper foil area | Top | Footprint (1.2 mm ²) |
| | Middle 1 | 5505 mm ² (74.2 mm × 74.2 mm) |
| | Middle 2 | 5505 mm ² (74.2 mm × 74.2 mm) |
| | Bottom | 5505 mm ² (74.2 mm × 74.2 mm) |



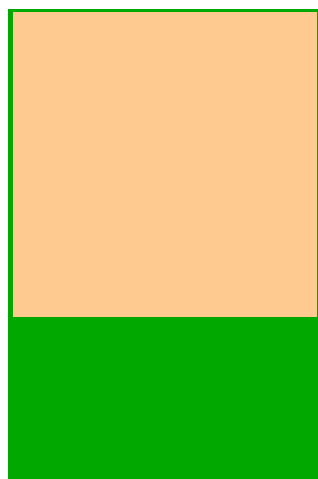
4 layer board sectional view



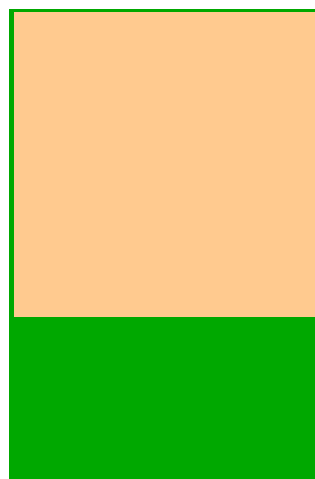
Footprint dimensions



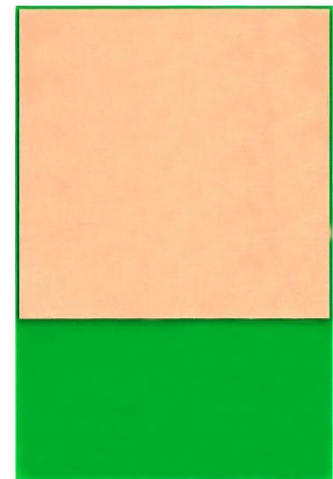
Top Layer Trace



Middle 1 Layer Trace



Middle 2 Layer Trace



Bottom Layer Trace

Thermal resistance data, 1 layer (1s)

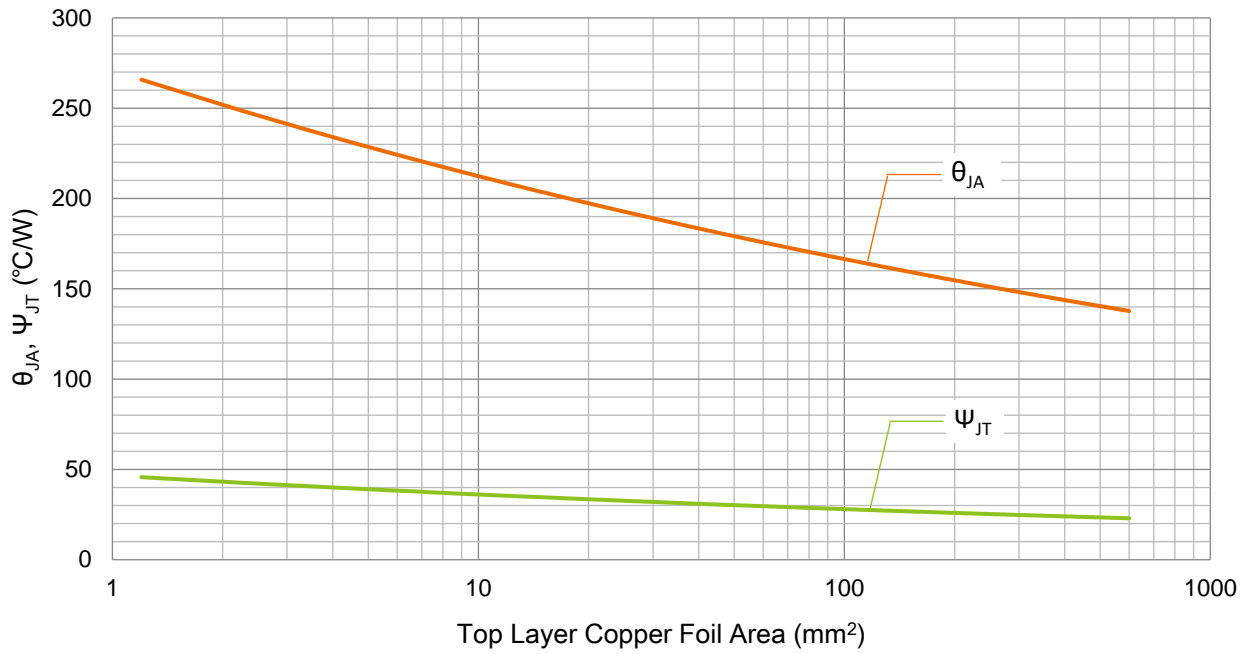


Figure 1. θ_{JA} , ψ_{JT} vs. copper foil surface area

Thermal resistance data, 2 layers (2s)

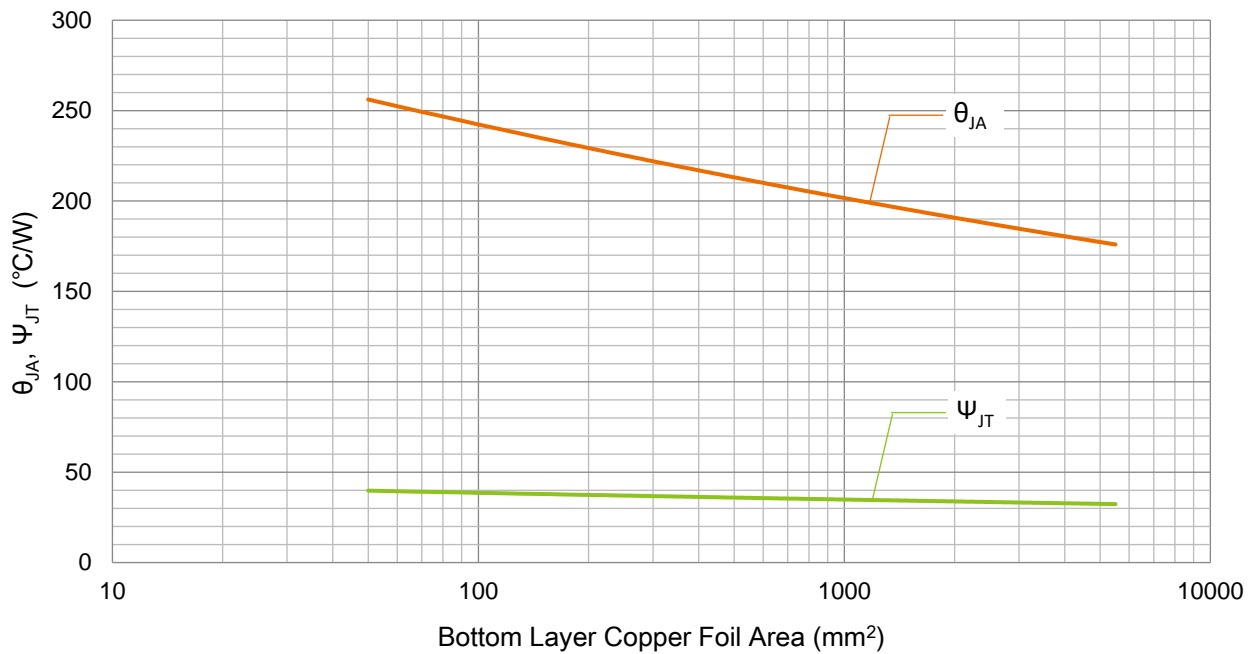
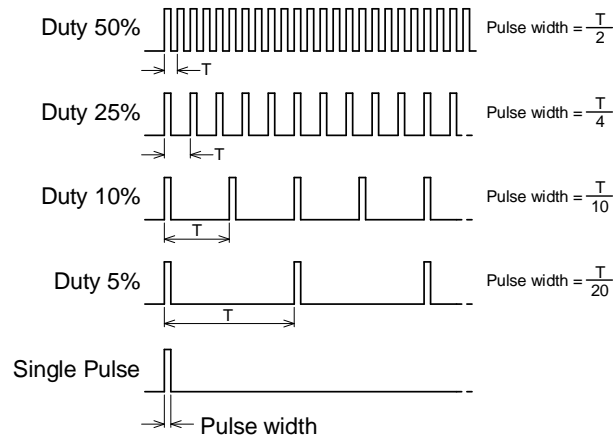


Figure 2. θ_{JA} , ψ_{JT} vs. Bottom layer copper foil area

Transient thermal resistance

Conforms to JEDEC standard JESD51

X axis: Pulse width is the time to apply power to the device



Y axis: Transient thermal resistance

Transient thermal resistance data, 1 layer (1s)

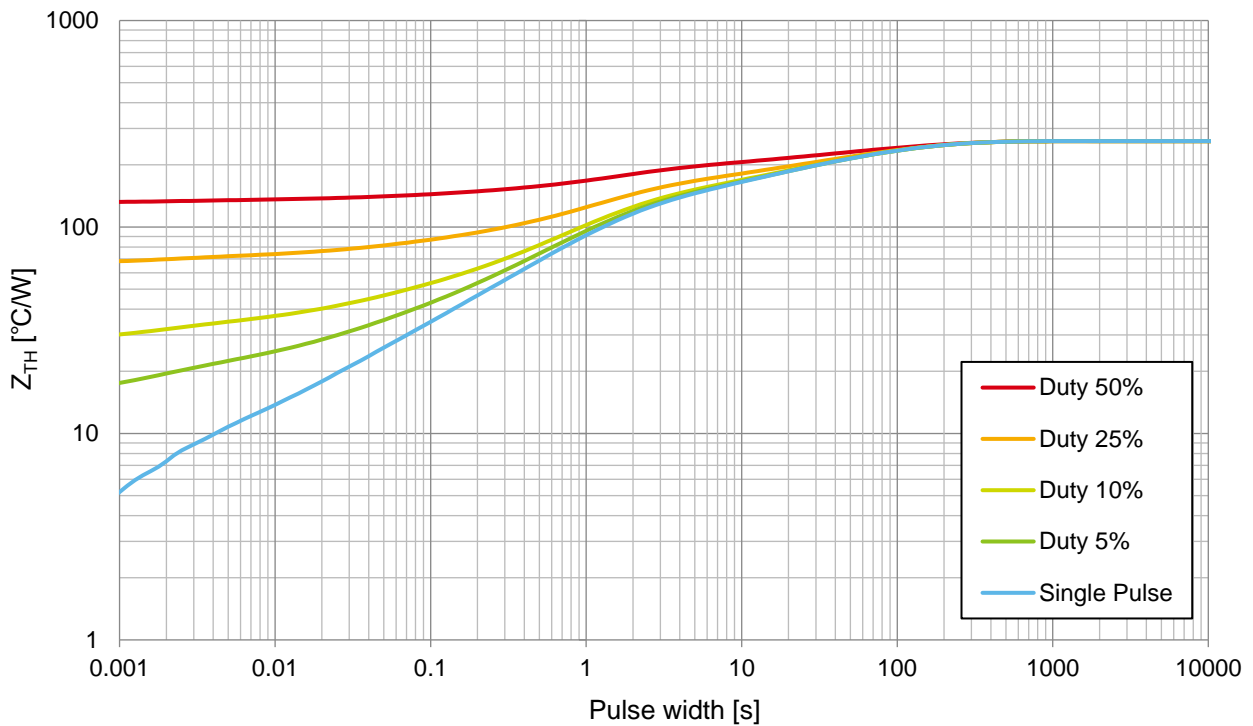


Figure 3. Transient thermal resistance, 1 layer, Copper foil surface area 1.2 mm² (Footprint)

Transient thermal resistance data, 1 layer (1s), continued

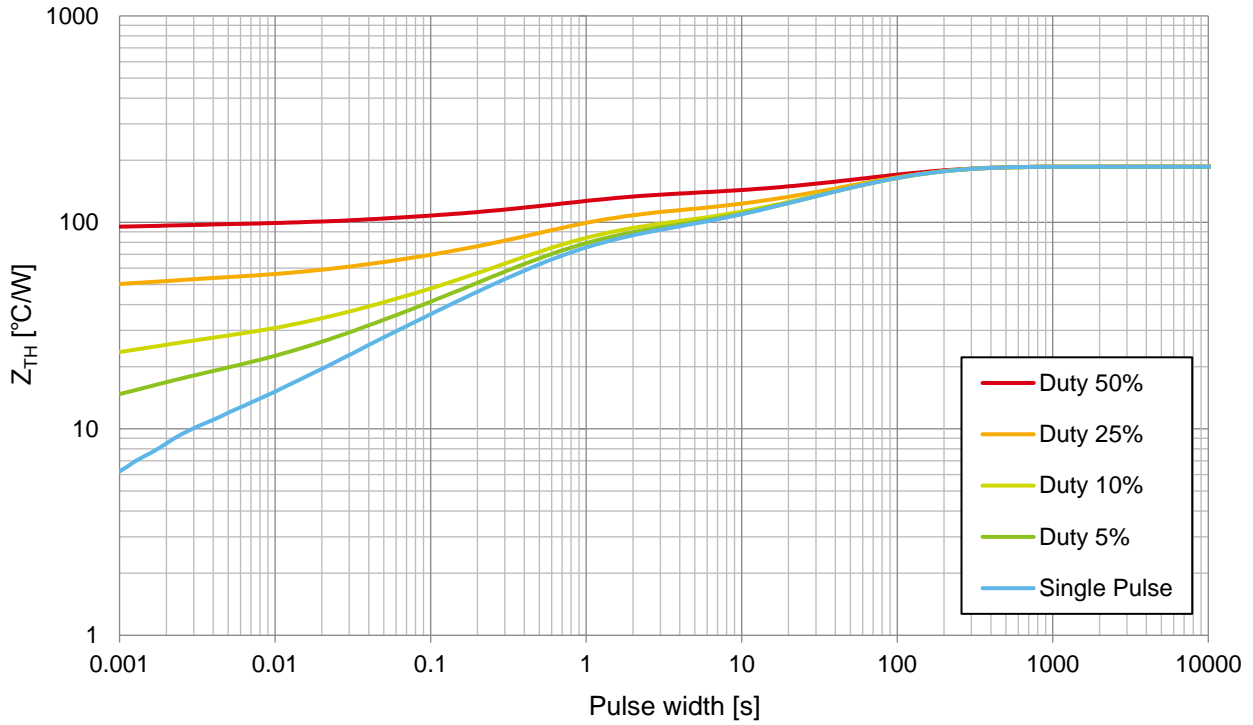


Figure 4. Transient thermal resistance, 1 layer, Copper foil surface area 50 mm²

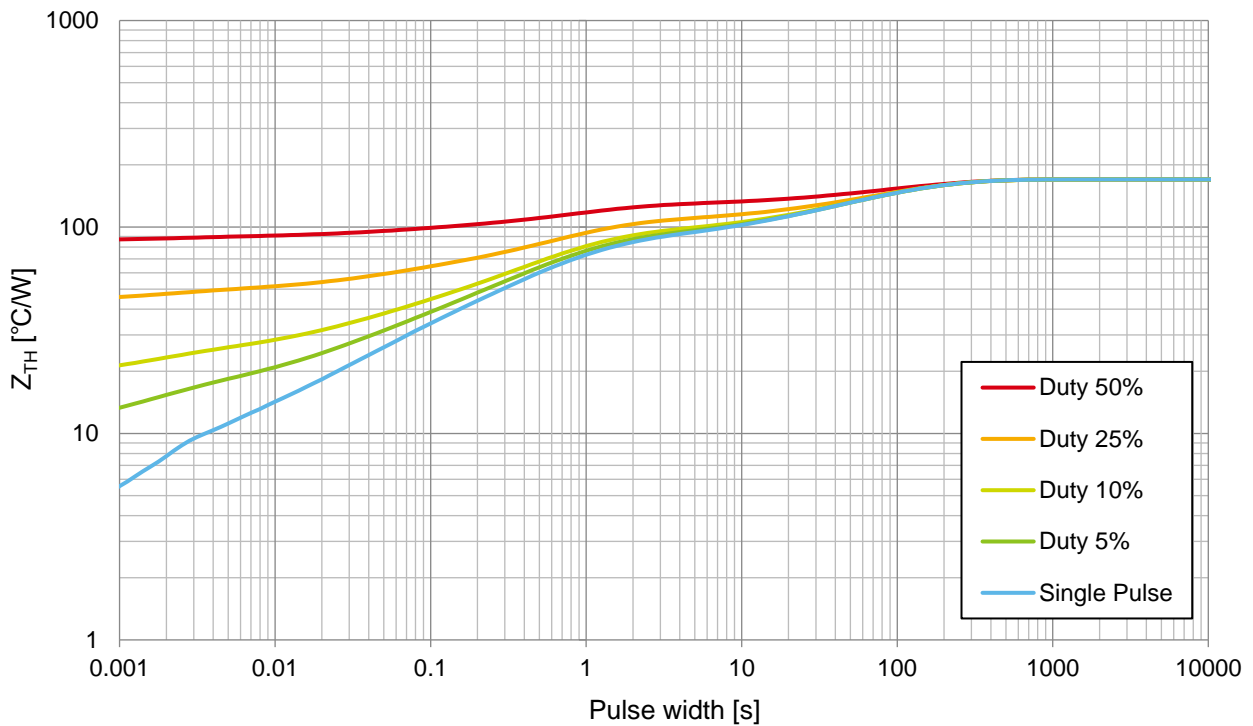


Figure 5. Transient thermal resistance, 1 layer, Copper foil surface area 100 mm²

Transient thermal resistance data, 1 layer (1s), continued

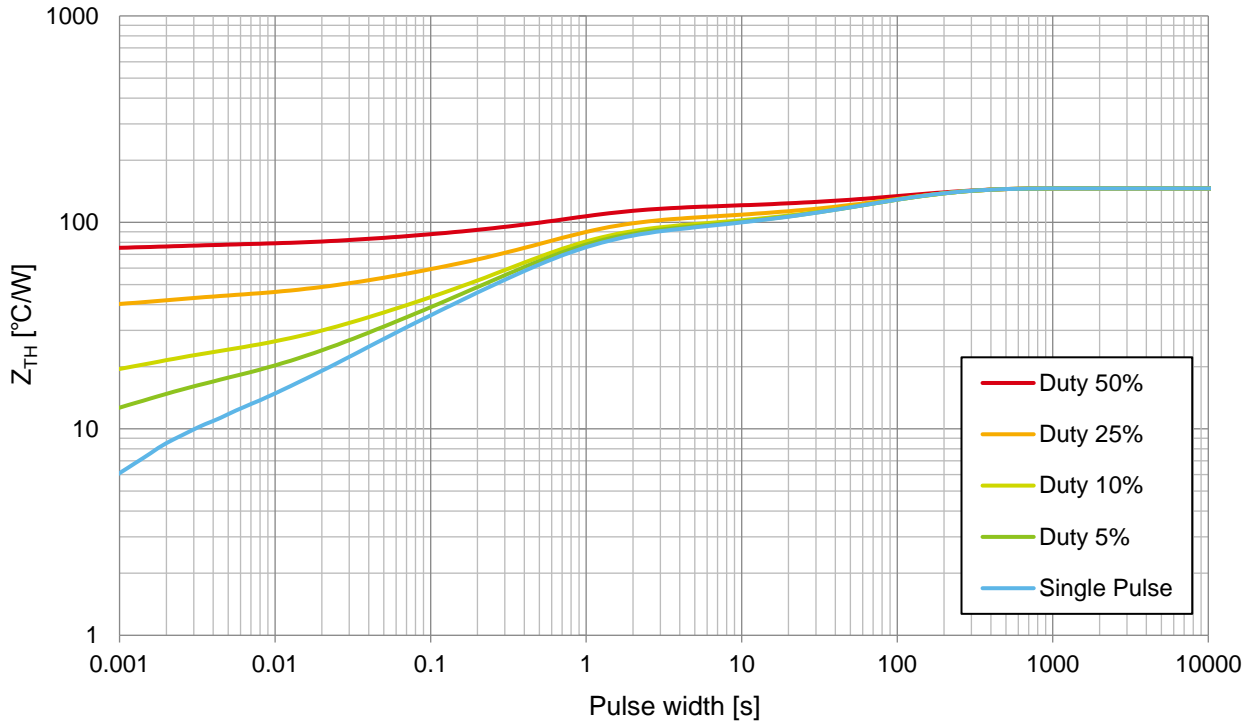


Figure 6. Transient thermal resistance, 1 layer, Copper foil surface area 300 mm²

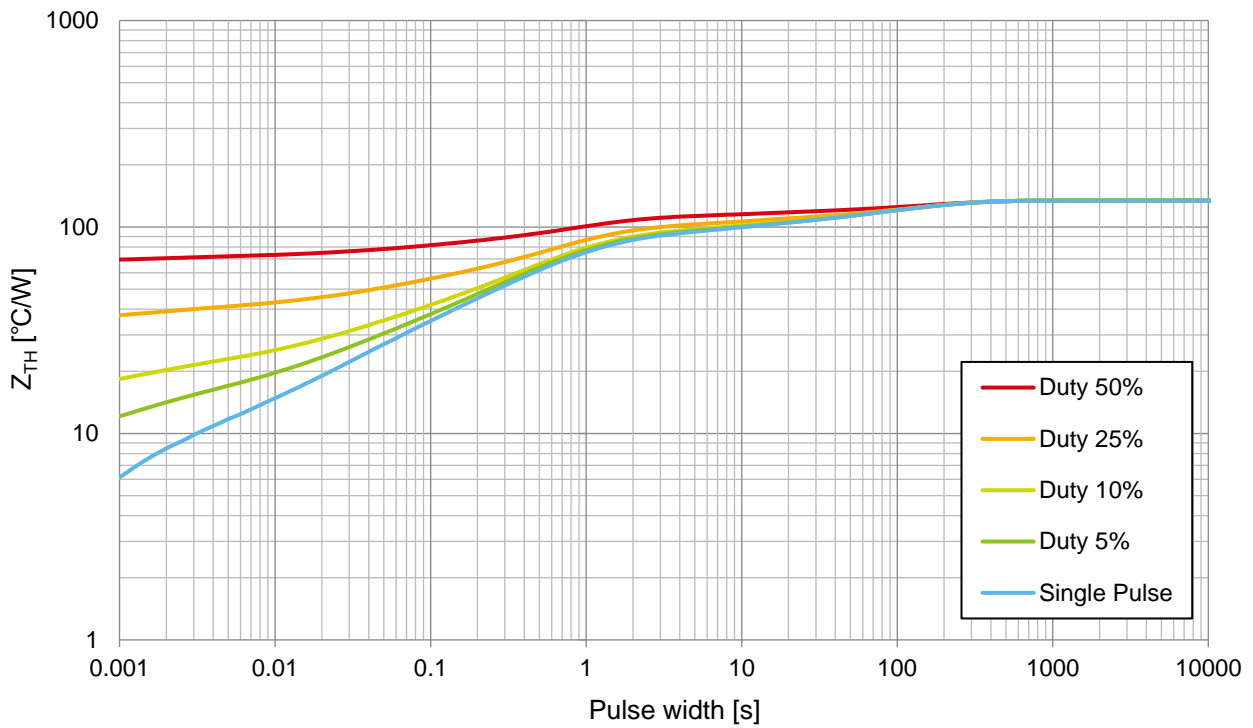


Figure 7. Transient thermal resistance, 1 layer, Copper foil surface area 600 mm²

Transient thermal resistance data, 2 layers (2s)

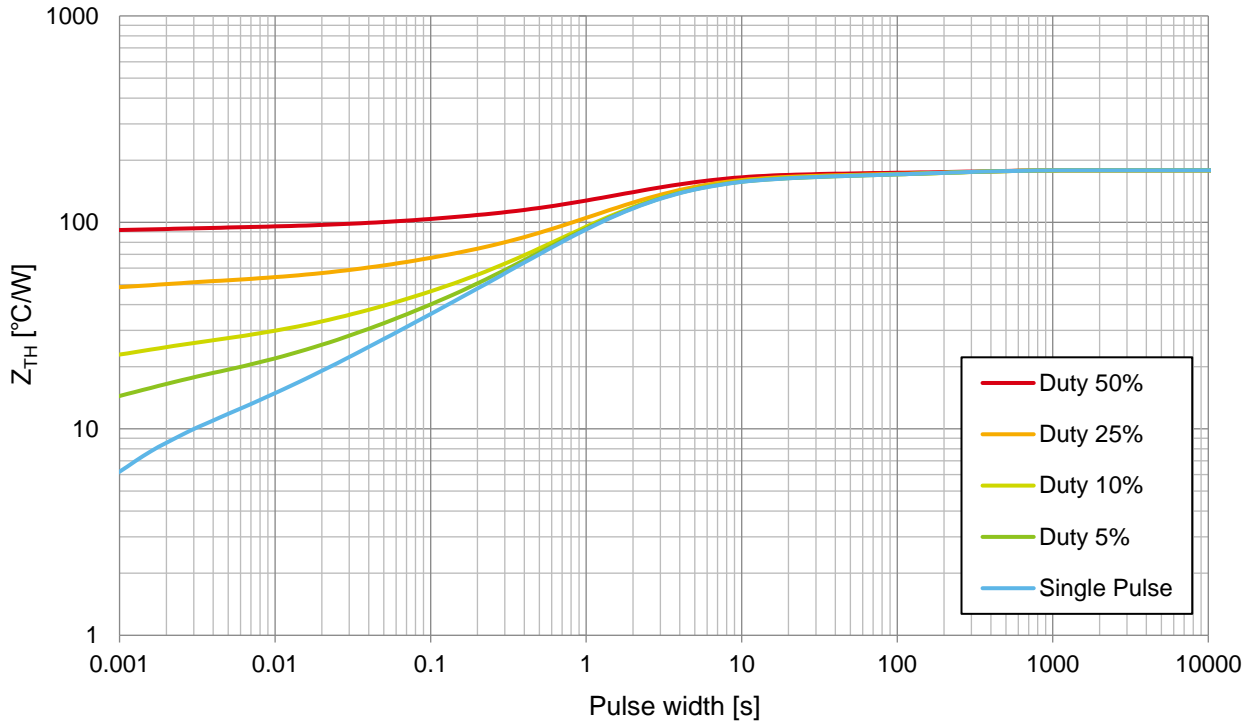


Figure 8. Transient thermal resistance, 2 layers, Copper foil bottom area 5505 mm²

Transient thermal resistance data, 4 layers (2s2p)

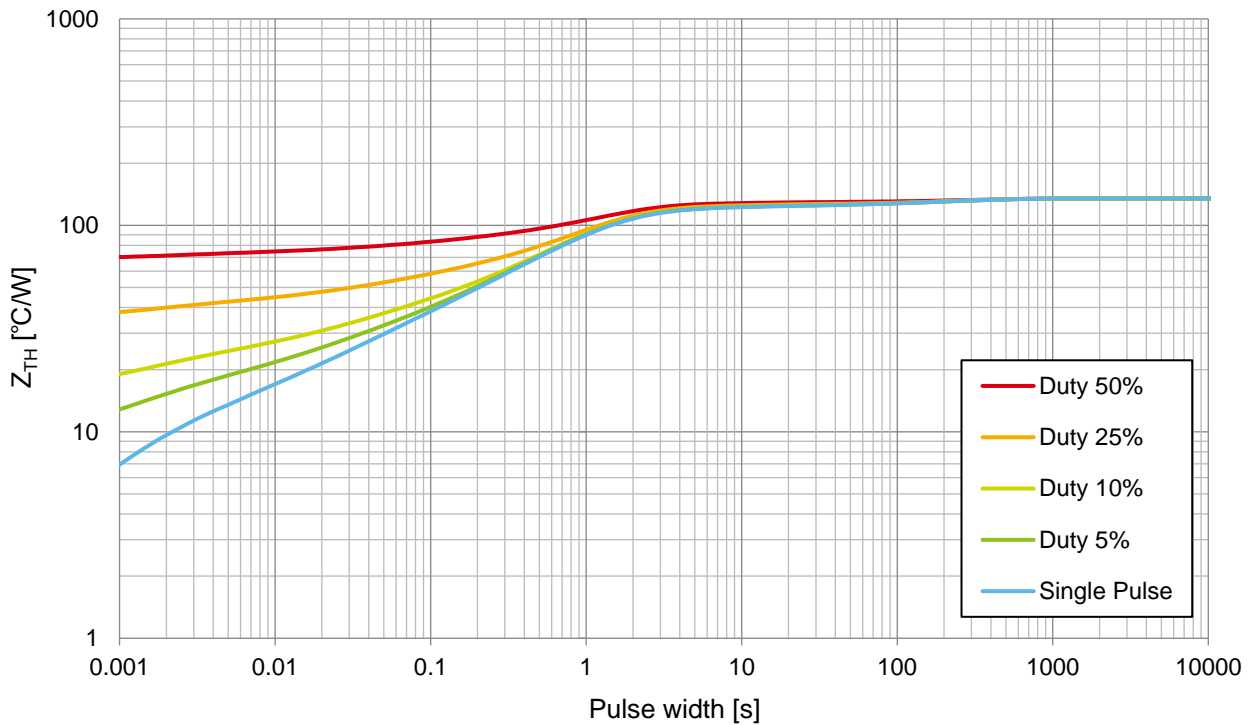


Figure 9. Transient thermal resistance, 4 layers

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