

Linear Regulator Series

Thermal Resistance Data: SSOP5

BUxxJA2DG-C, BUxxJA2VG-C Series

This application note provides the thermal resistance data of the SSOP5 package used for the thermal design of the BUxxJA2DG-C and BUxxJA2VG-C series linear regulator IC.

Product Summary

Model name: [BUxxJA2DG-C series](#)
[BUxxJA2VG-C series](#)

Package name: SSOP5

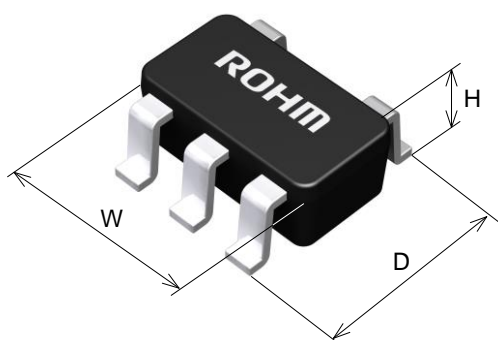
Function: Linear regulator (LDO) IC

See Datasheet for more details.

[Datasheet: BUxxJA2DG-C series](#)

[Datasheet: BUxxJA2VG-C series](#)

Package



SSOP5

W (typ) D (typ) H (max)
 2.9 mm × 2.8 mm × 1.25 mm

Measurement environment

Content	Standard
Measurement environment	JEDEC STANDARD JESD51-2A (Still Air)
Measurement board standard	JEDEC STANDARD JESD51-3 JESD51-5

Thermal resistance

Configuration	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)
1 layer	260.7	44
2 layers	178.8	32
4 layers	135.1	30

θ_{JA} : Thermal resistance between
 junction temperature T_J - ambient temperature T_A

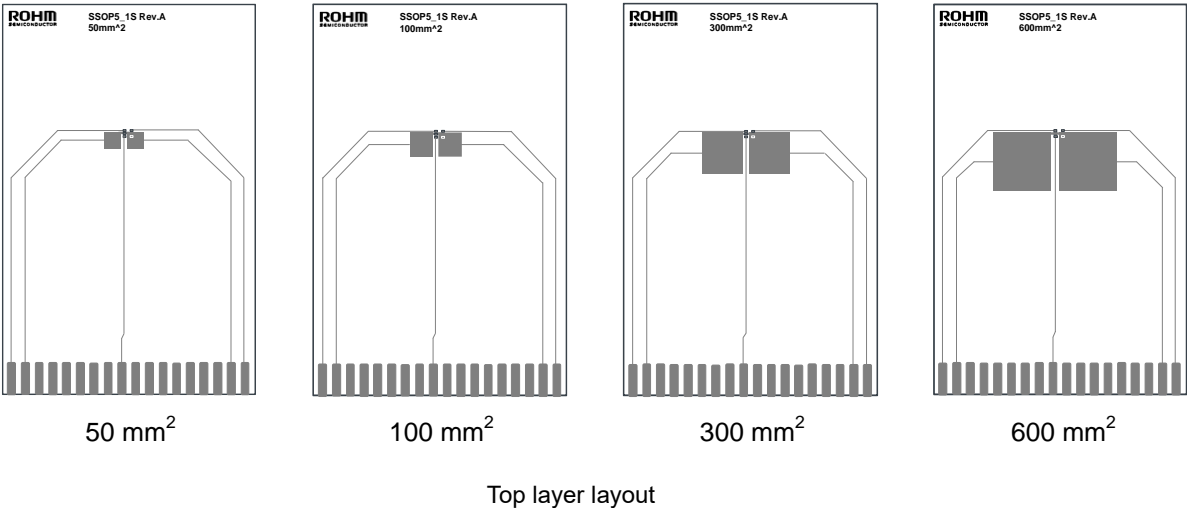
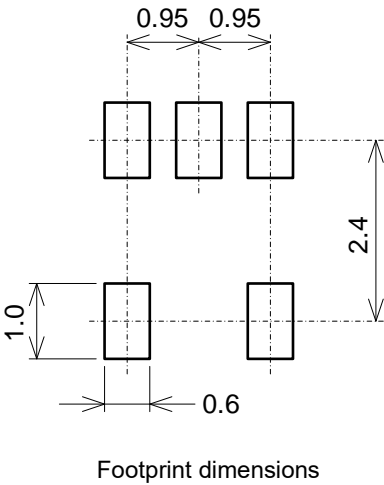
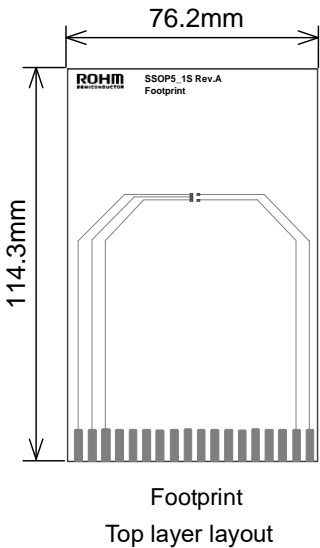
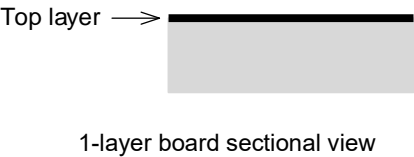
Ψ_{JT} : Thermal characteristics parameter between
 junction temperature T_J - package surface center temperature T_T

Note: The thermal resistances and thermal characteristics parameters in this application note are based on measurement under a JEDEC environment and may not always be consistent with the values for actual equipment. It is necessary to consider variations in the values due to the PCB characteristics, PCB layout, parts layout, chassis shape, surrounding environment, and so on.

PCB specifications, 1 layer (1s)

Conforms to JEDEC standard JESD51-3

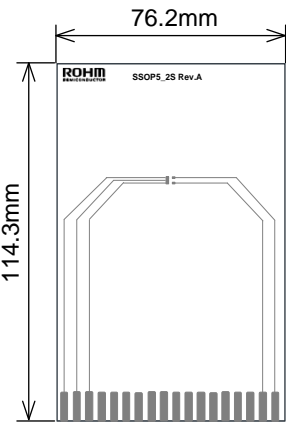
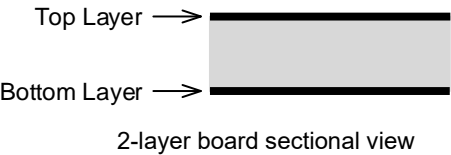
Item	Value
Board thickness	1.57 mm
Board outline dimensions	76.2 mm × 114.3 mm
Board material	FR-4
Trace thickness (Finished thickness)	70 μm (2 oz)
Lead width	0.254 mm
Copper foil area	Footprint [50 mm ² to 600 mm ²]



PCB specifications, 2 layers

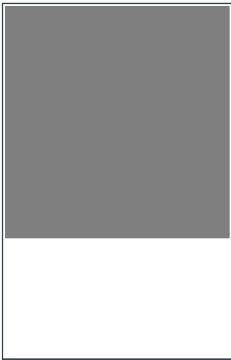
Conforms to JEDEC standard JESD51-7

Item		Value
Board thickness		1.60 mm
Board outline dimensions		76.2 mm × 114.3 mm
Board material		FR-4
Trace thickness (Finished thickness)	Top	70 μm (2 oz)
	Bottom	70 μm (2 oz)
Lead width		0.254 mm
Copper foil area	Top	Footprint 5505 mm ² (74.2 mm × 74.2 mm) [50 mm ² to 3000 mm ²]
	Bottom	



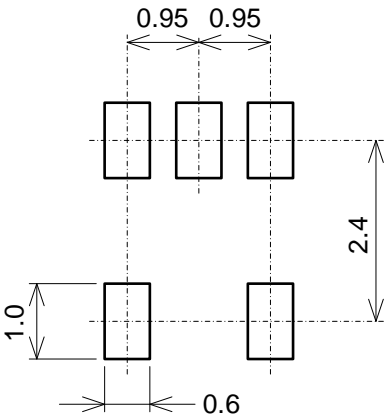
Footprint

Top layer layout

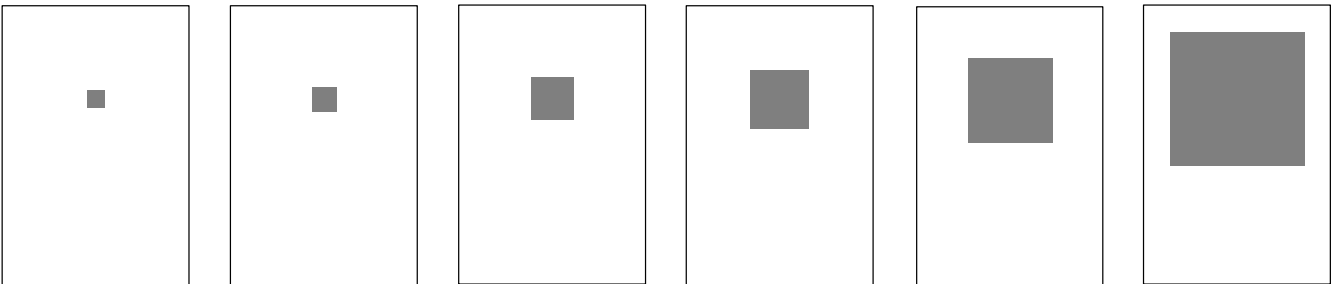


5505 mm²
(74.2 mm × 74.2 mm)

Bottom layer layout



Footprint dimensions



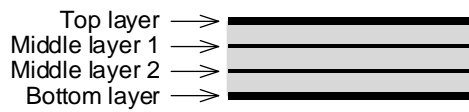
50 mm² (7.1 mm × 7.1 mm) 100 mm² (10 mm × 10 mm) 300 mm² (17.3 mm × 17.3 mm) 600 mm² (24.5 mm × 24.5 mm) 1200 mm² (34.6 mm × 34.6 mm) 3000 mm² (54.8 mm × 54.8 mm)

Bottom layer layout

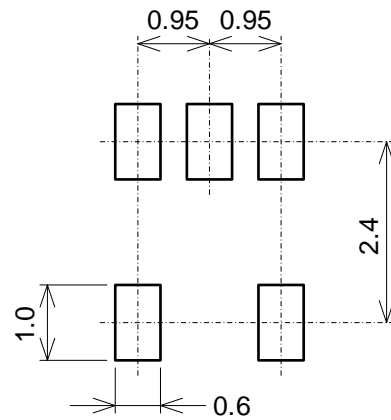
PCB specifications, 4 layers (2s2p)

Conforms to JEDEC standard JESD51-7

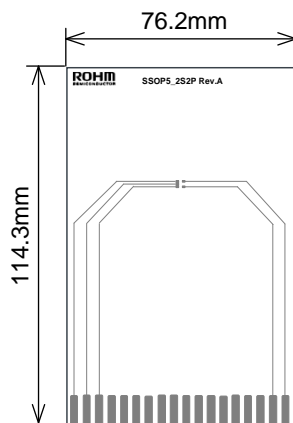
Item		Value
Board thickness		1.60 mm
Board outline dimensions		76.2 mm × 114.3 mm
Board material		FR-4
Trace thickness (Finished thickness)	Top	70 μm (2 oz)
	Middle 1	35 μm (1 oz)
	Middle 2	35 μm (1 oz)
	Bottom	70 μm (2 oz)
Lead width		0.254 mm
Copper foil area	Top	Footprint
	Middle 1	5505 mm ² (74.2 mm × 74.2 mm)
	Middle 2	5505 mm ² (74.2 mm × 74.2 mm)
	Bottom	5505 mm ² (74.2 mm × 74.2 mm)



4-layer board sectional view



Footprint dimensions



Footprint

Top layer layout



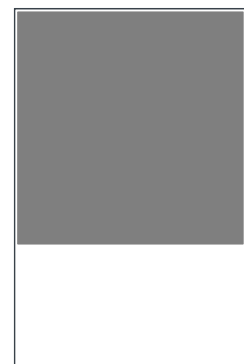
5505 mm²
(74.2 mm × 74.2 mm)

Middle 1 layer layout



5505 mm²
(74.2 mm × 74.2 mm)

Middle 2 layer layout



5505 mm²
(74.2 mm × 74.2 mm)

Bottom layer layout

Thermal resistance data, 1 layer (1s)

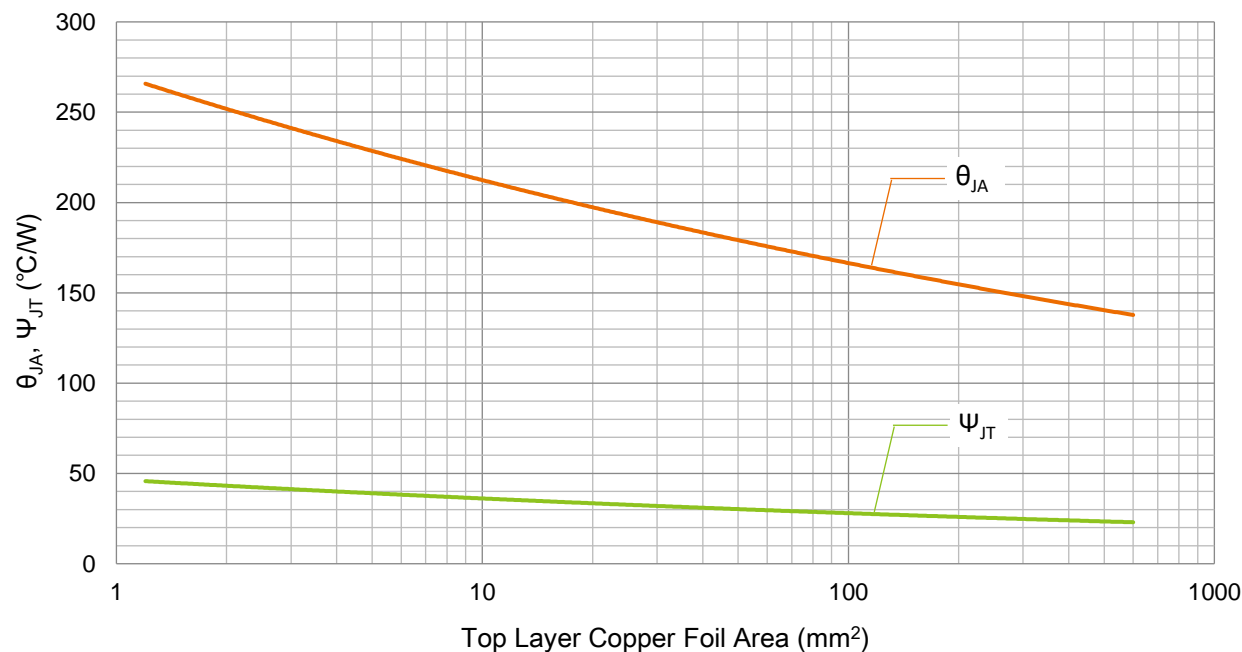


Figure 1. θ_{JA} , Ψ_{JT} vs. copper foil surface area

Thermal resistance data, 2 layers

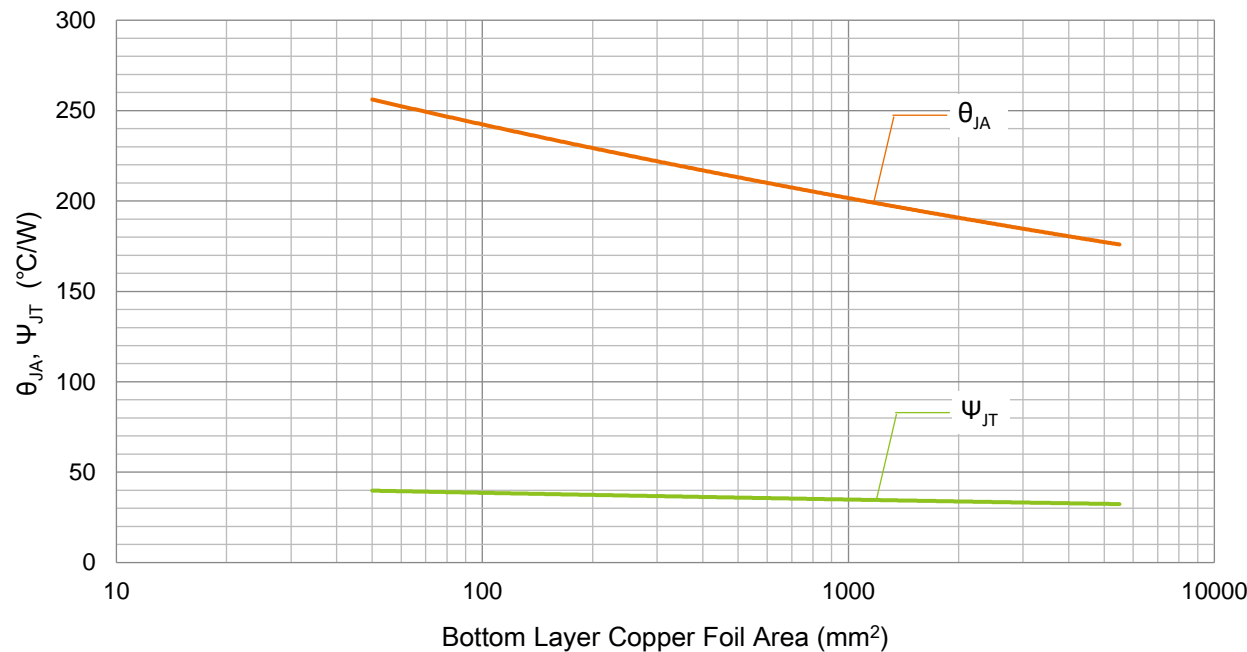
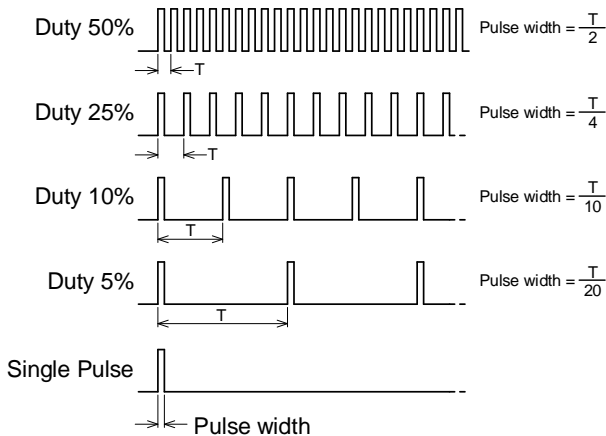


Figure 2. θ_{JA} , Ψ_{JT} vs. Bottom layer copper foil area

Transient thermal resistance

Conforms to JEDEC standard JESD51

X axis: Pulse width is the time to apply power to the device



Y axis: Transient thermal resistance

Transient thermal resistance data, 1 layer (1s)

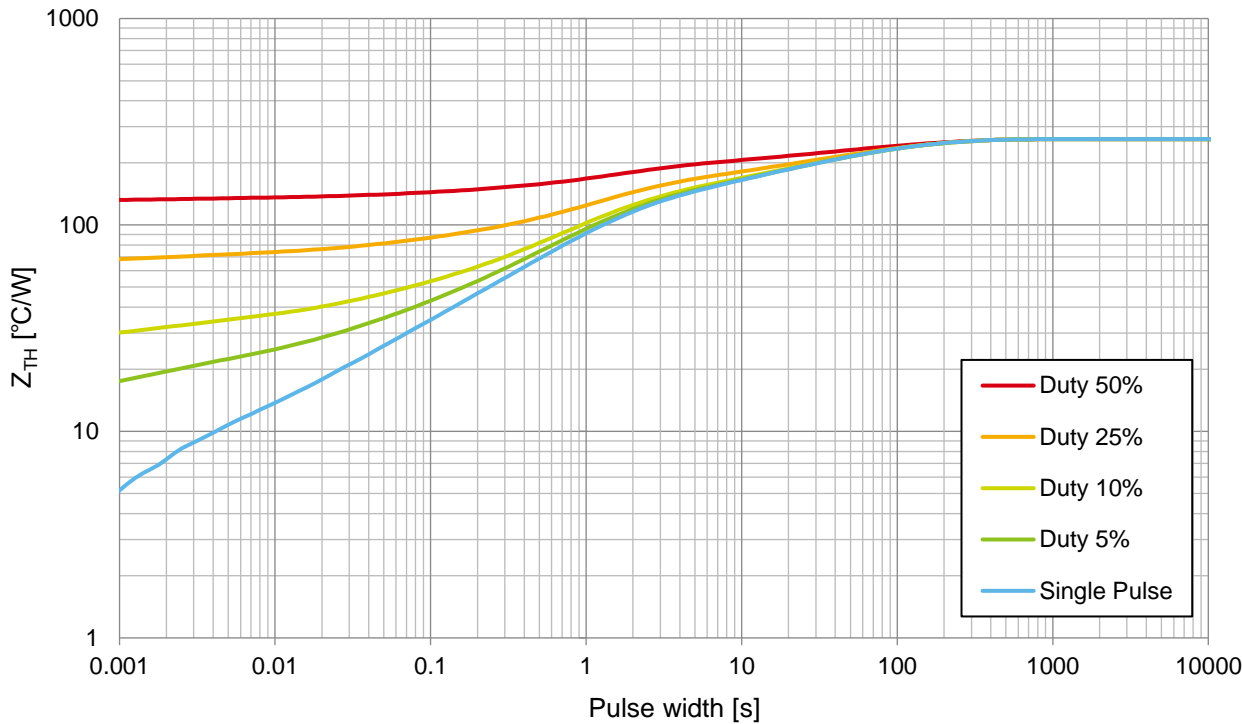


Figure 3. Transient thermal resistance, 1 layer, Copper foil surface area 1.2 mm² (Footprint)

Transient thermal resistance data, 1 layer (1s), continued

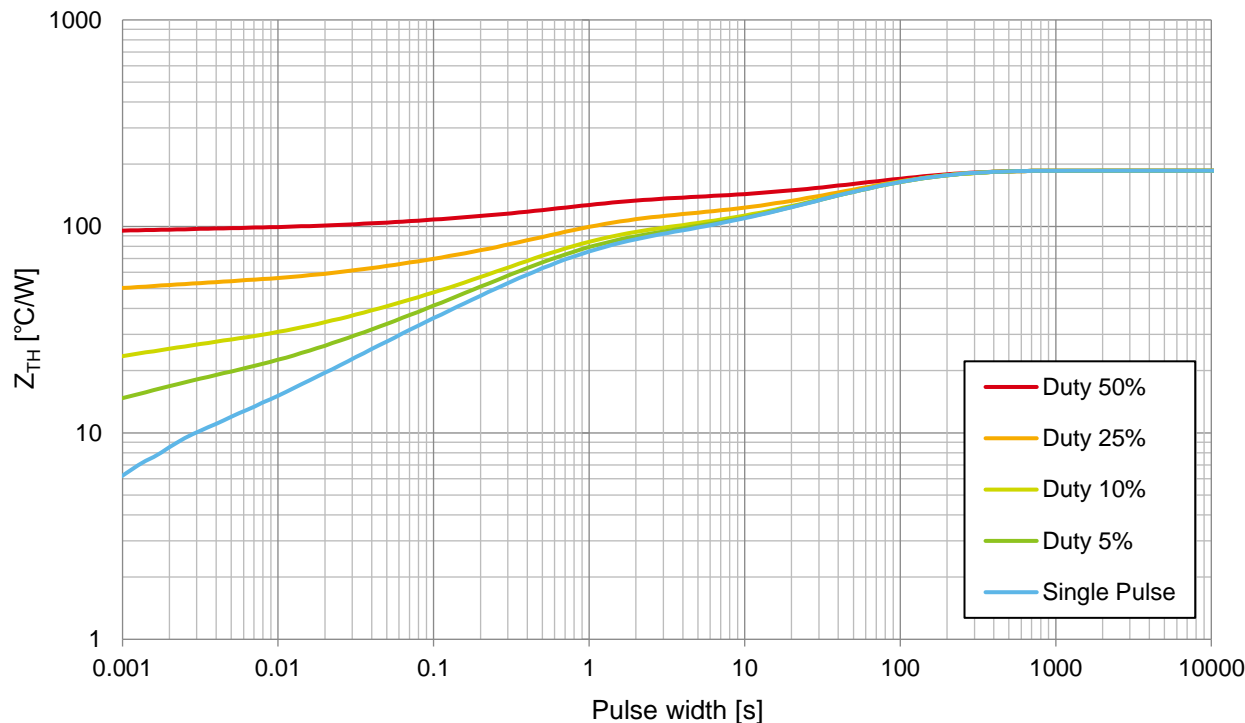


Figure 4. Transient thermal resistance, 1 layer, Copper foil surface area 50 mm²

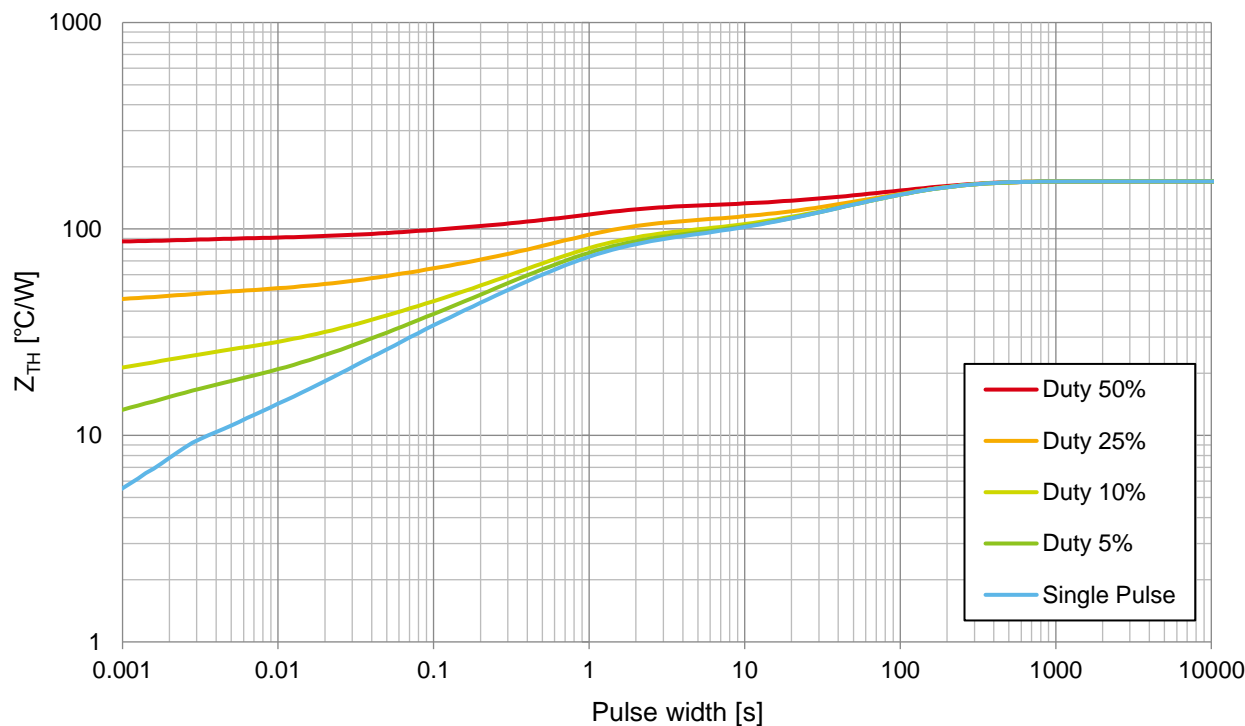


Figure 5. Transient thermal resistance, 1 layer, Copper foil surface area 100 mm²

Transient thermal resistance data, 1 layer (1s), continued

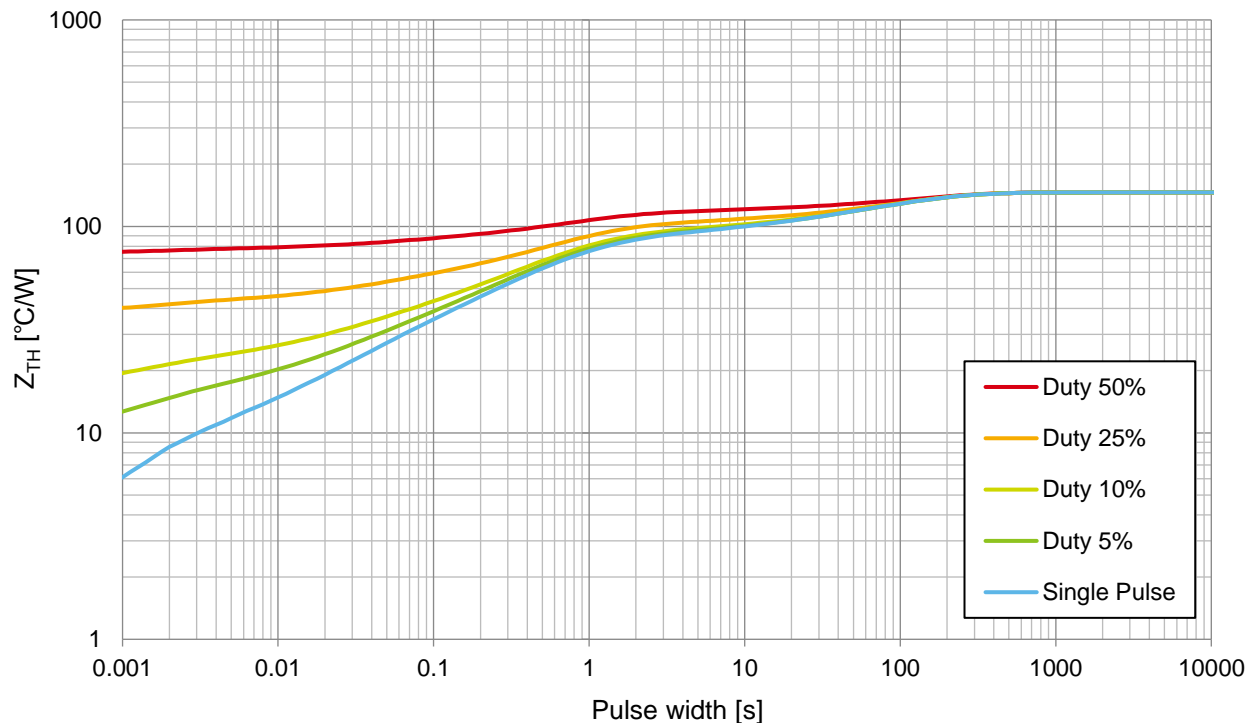


Figure 6. Transient thermal resistance, 1 layer, Copper foil surface area 300 mm²

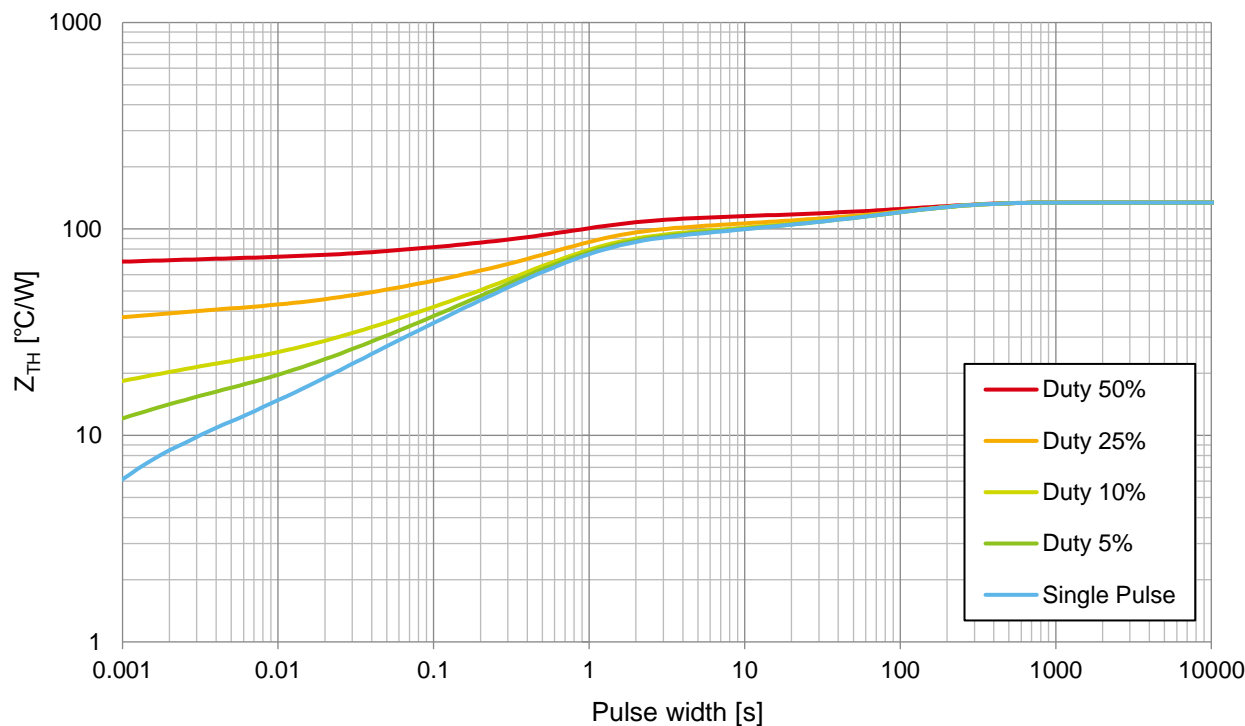


Figure 7. Transient thermal resistance, 1 layer, Copper foil surface area 600 mm²

Transient thermal resistance data, 2 layers

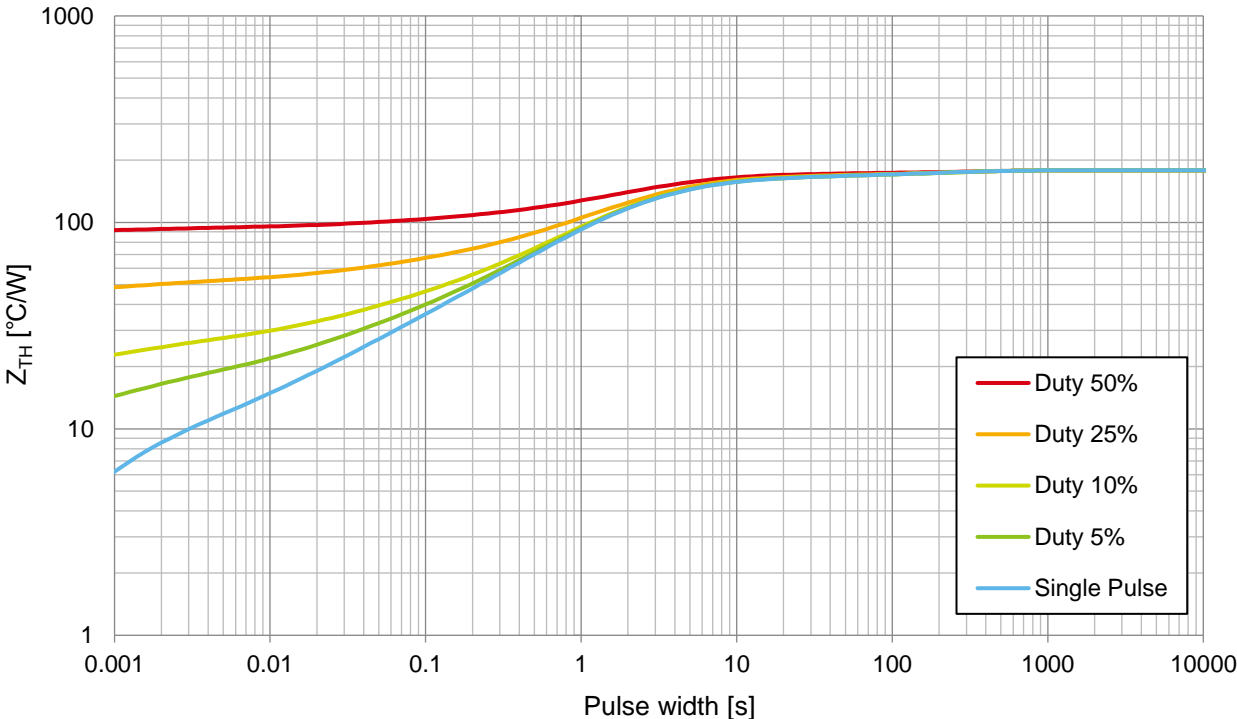


Figure 8. Transient thermal resistance, 2 layers, Copper foil bottom area 5505 mm²

Transient thermal resistance data, 4 layers (2s2p)

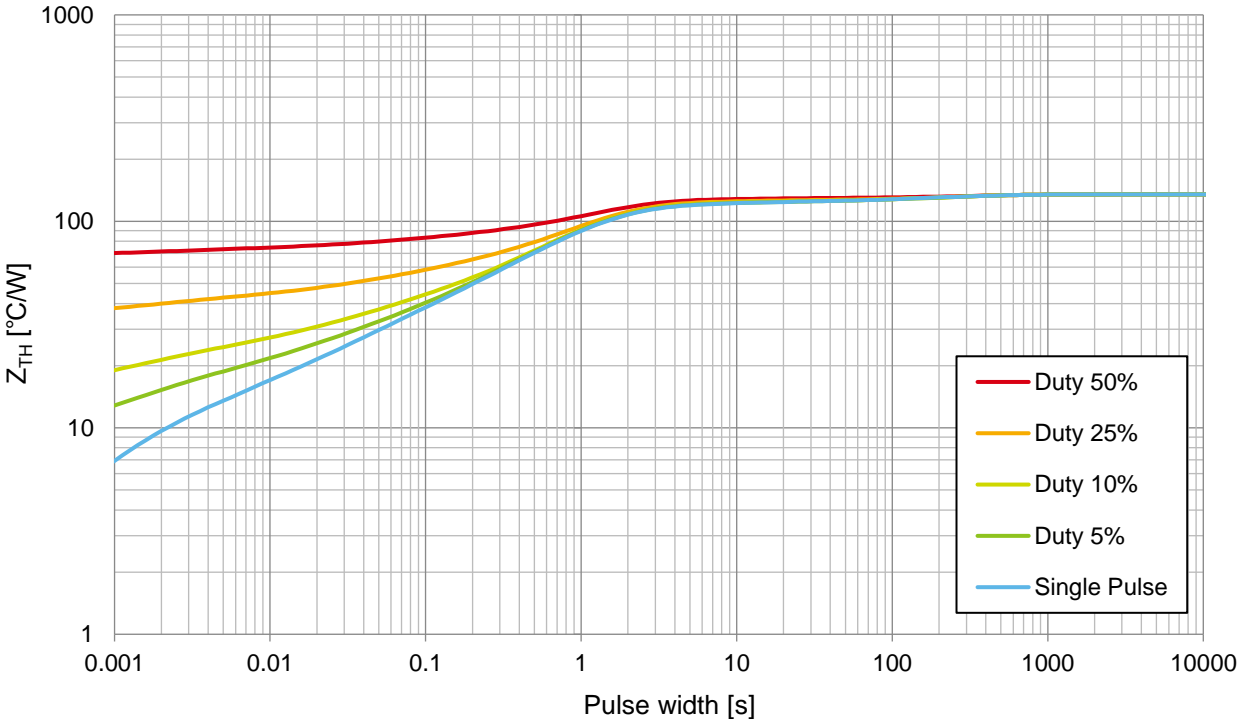


Figure 9. Transient thermal resistance, 4 layers

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