

## Linear Regulator Series

# Thermal Resistance Data: TO252-3

## BD4xxM5FP-C Series

This application note provides the thermal resistance data of the TO252-3 package used for the thermal design of the BD4xxM5FP-C series linear regulator IC.

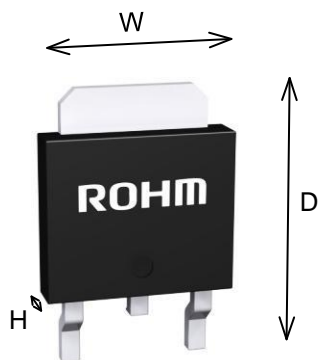
### IC summary

The BD4xxM5FP-C series includes low quiescent current regulators with a breakdown voltage of 45 V, output current of 500 mA, and current consumption of 38  $\mu$ A. These regulators are ideal for reducing the current consumption of systems directly connected to batteries. They support AEC-Q100 and allow usage in every automotive application.

- Operating temperature range:  $T_J$  -40°C to +150°C
- Operating voltage range: 3.0 V to 42 V
- Low quiescent current: 38  $\mu$ A
- Output current: 500 mA
- Output voltage: 3.3 V, 5.0 V
- Output voltage precision:  $\pm$ 2%

See Datasheet for more details.

### Package



TO252-3

W (typ) D (typ) H (max)

6.5mm  $\times$  9.5mm  $\times$  2.5mm

### Measurement environment

Content	Standard
Measurement environment	JEDEC STANDARD JESD51-2A (Still Air)
Measurement board standard	JEDEC STANDARD JESD51-3 JESD51-5 JESD51-7

### Thermal resistance

Configuration	$\theta_{JA}$ (°C/W)	$\Psi_{JT}$ (°C/W)
1 layer	132.2	13
2 layers	30.2	3
4 layers	23.3	2

$\theta_{JA}$ : Thermal resistance between  
junction  $T_J$  - ambient temperature  $T_A$

$\Psi_{JT}$ : Thermal characteristics parameter between  
junction  $T_J$  - package surface center temperature  $T_T$

Note: The thermal resistances and thermal characteristics parameters in this application note are based on measurement under a JEDEC environment and may not always be consistent with the values for actual equipment. It is necessary to consider variations in the values due to the PCB characteristics, PCB layout, parts layout, chassis shape, surrounding environment, and so on.

PCB specifications, 1 layer (1s)

Conforms to JEDEC standard JESD51-3

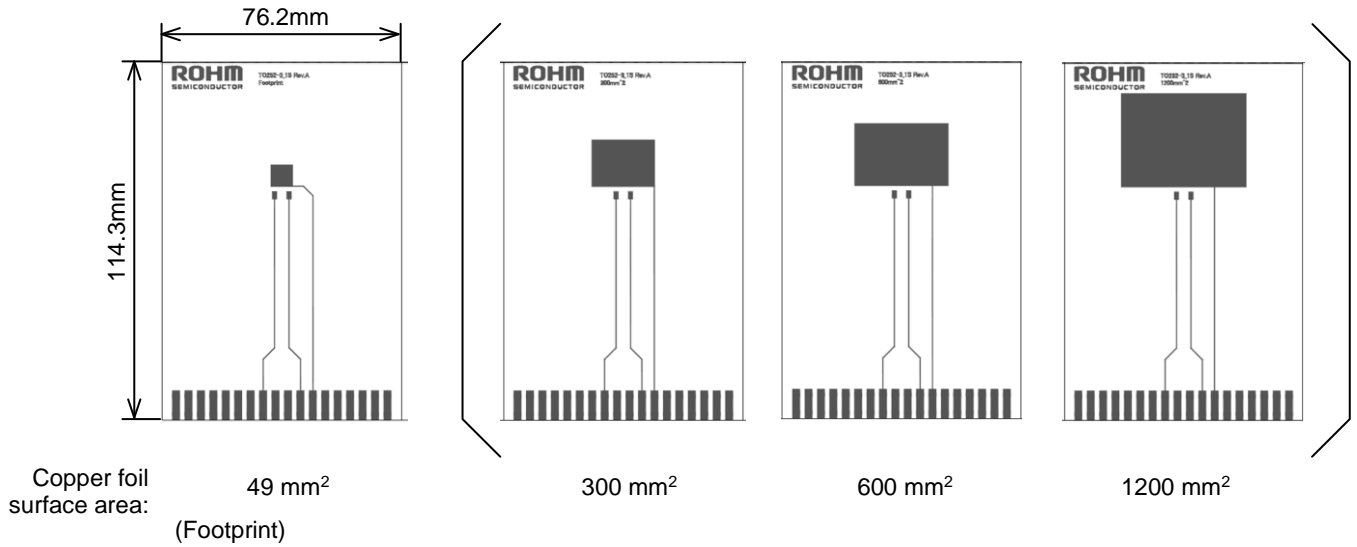


Figure 1. Top Layer Trace

Item	Value
Board thickness	1.57 mm
Board outline dimensions	76.2 mm × 114.3 mm
Board material	FR-4
Copper foil thickness	70 μm (2 oz copper foil)
Lead width	0.254 mm
Copper foil area	49 mm <sup>2</sup> (Footprint), [300 mm <sup>2</sup> , 600 mm <sup>2</sup> , 1200 mm <sup>2</sup> ]

Table 1. 1 layer PCB specifications

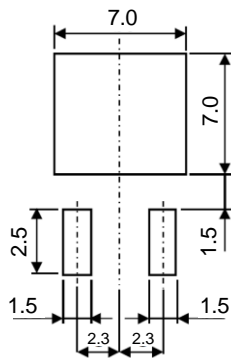


Figure 2. Footprint dimensions



Figure 3. 1 layer board sectional view

PCB specifications, 2 layers (2s)

Conforms to JEDEC standard JESD51-5, JESD51-7

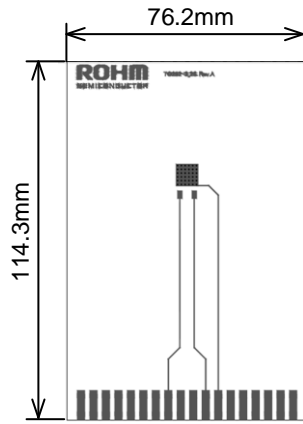


Figure 4. Top Layer Trace

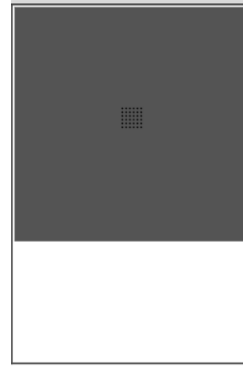


Figure 5. Bottom Layer Trace

Item		Value
Board thickness		1.60 mm
Board outline dimensions		76.2 mm x 114.3 mm
Board material		FR-4
Copper foil thickness	Top	70 μm (1 oz copper foil + plating)
	Bottom	70 μm (1 oz copper foil + plating)
Lead width		0.254 mm
Copper foil area	Top	49 mm <sup>2</sup> (Footprint)
	Bottom	5,505 mm <sup>2</sup> (74.2 mm x 74.2 mm)

Table 2. 2 layer PCB specifications

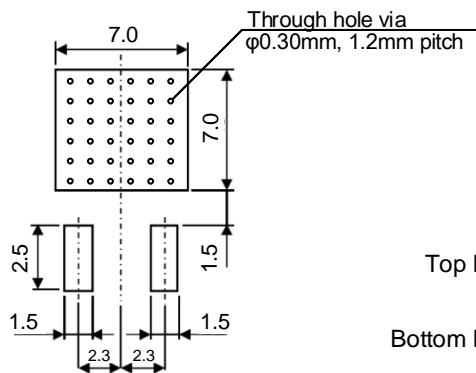


Figure 6. Footprint dimensions

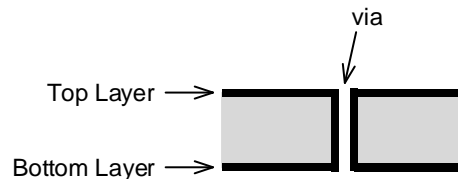


Figure 7. 2 layer board sectional view

PCB specifications, 4 layers (2s2p)

Conforms to JEDEC standard JESD51-5, JESD51-7

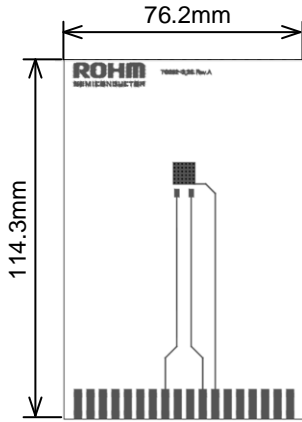


Figure 8.  
Top Layer Trace

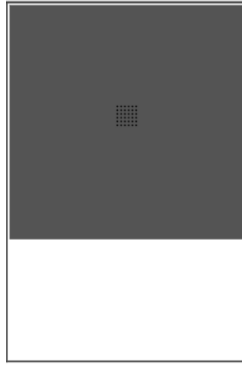


Figure 9.  
Middle 1 Layer Trace

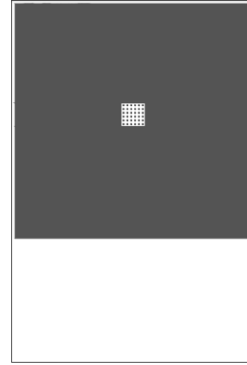


Figure 10.  
Middle 2 Layer Trace

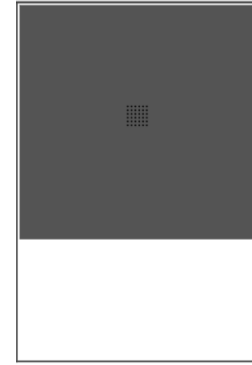


Figure 11.  
Bottom Layer Trace

Item	Value
Board thickness	1.60 mm
Board outline dimensions	76.2 mm × 114.3 mm
Board material	FR-4
Copper foil thickness	Top 70 μm (1 oz copper foil + plating) Middle 1 35 μm (1 oz copper foil) Middle 2 35 μm (1 oz copper foil) Bottom 70 μm (1 oz copper foil + plating)
Lead width	0.254 mm
Copper foil area	Top 49 mm <sup>2</sup> (Footprint) Middle 1 5505 mm <sup>2</sup> (74.2 mm×74.2 mm) Middle 2 5505 mm <sup>2</sup> (74.2 mm×74.2 mm) Bottom 5505 mm <sup>2</sup> (74.2 mm×74.2 mm)

Table 3. 4 layer PCB specifications

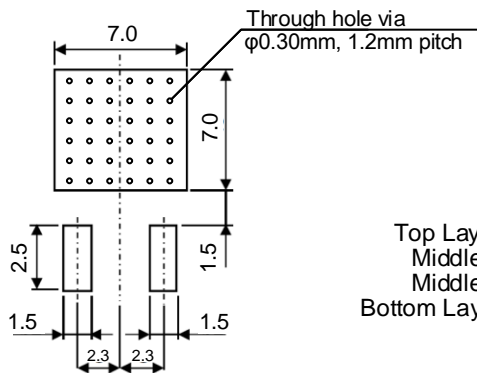


Figure 12. Footprint dimensions

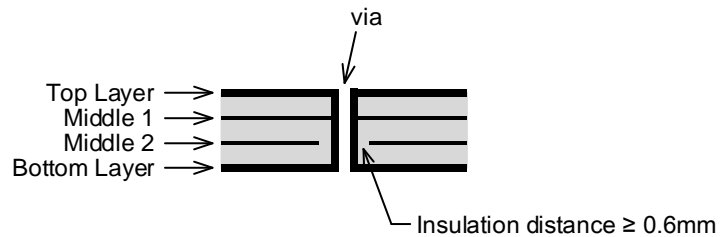


Figure 13. 4 layer board sectional view

Thermal resistance data, 1 layer (1s)

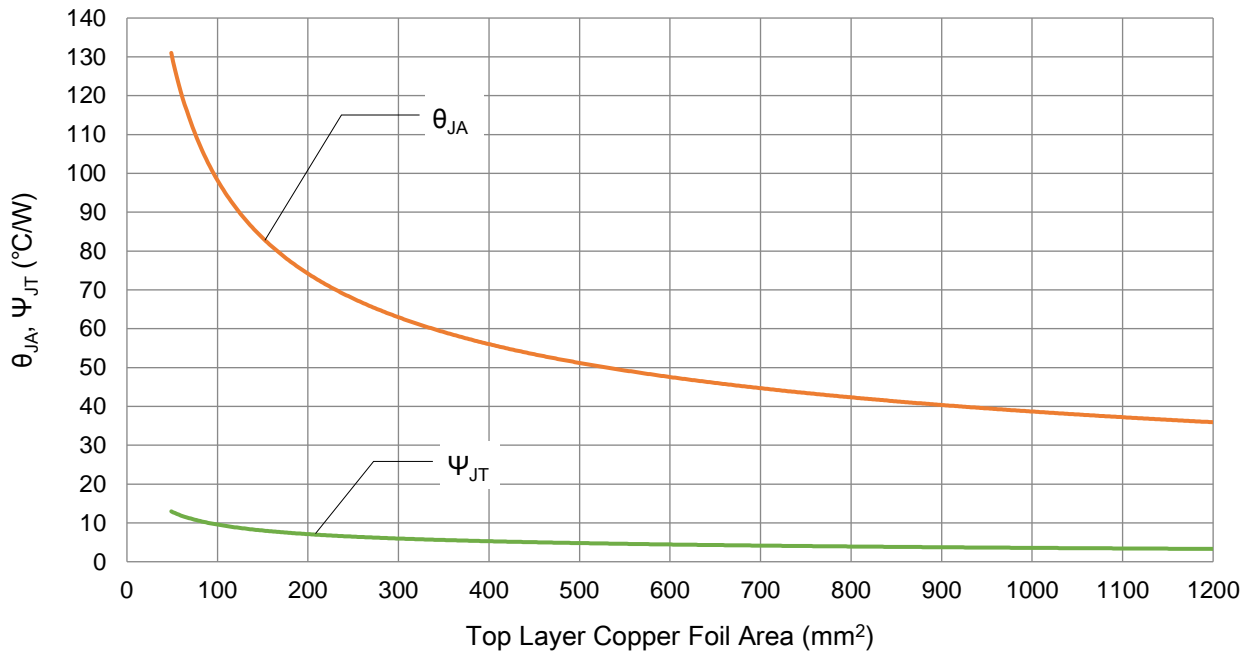


Figure 14.  $\theta_{JA}$ ,  $\psi_{JT}$  vs. copper foil surface area

Thermal resistance data, 2 layers (2s)

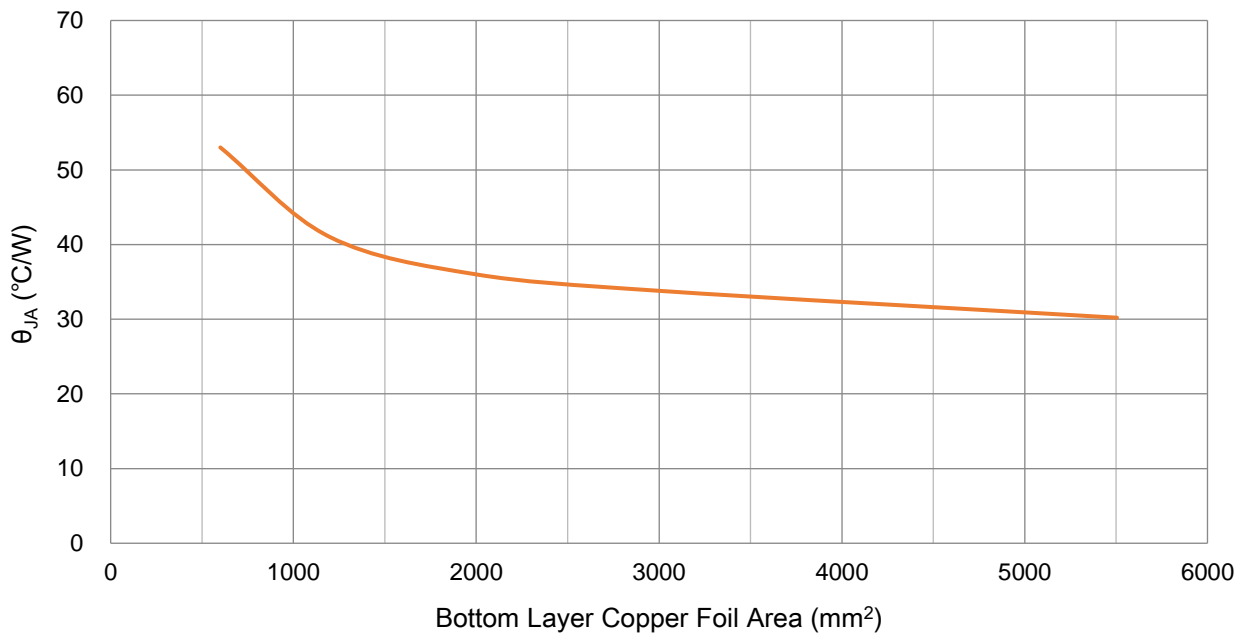


Figure 15.  $\theta_{JA}$  vs. copper foil back surface area

Transient thermal resistance data, 1 layer (1s)

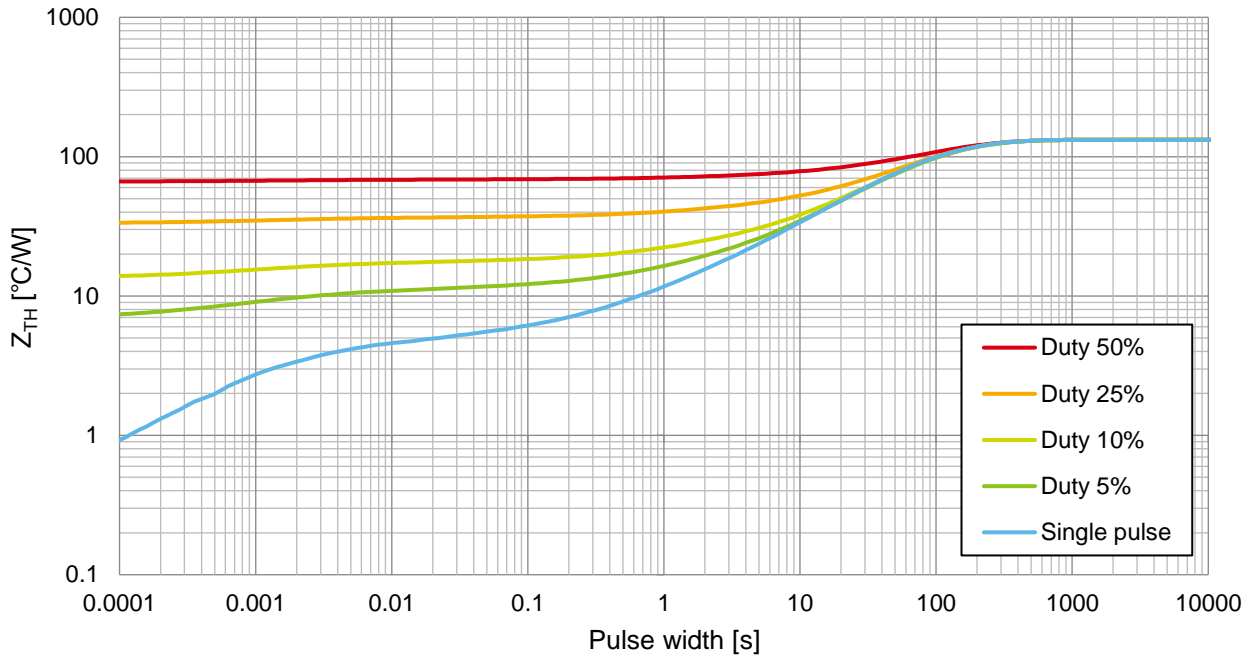


Figure 16. Transient thermal resistance, 1 layer  
Copper foil surface area 49 mm<sup>2</sup> (Footprint)

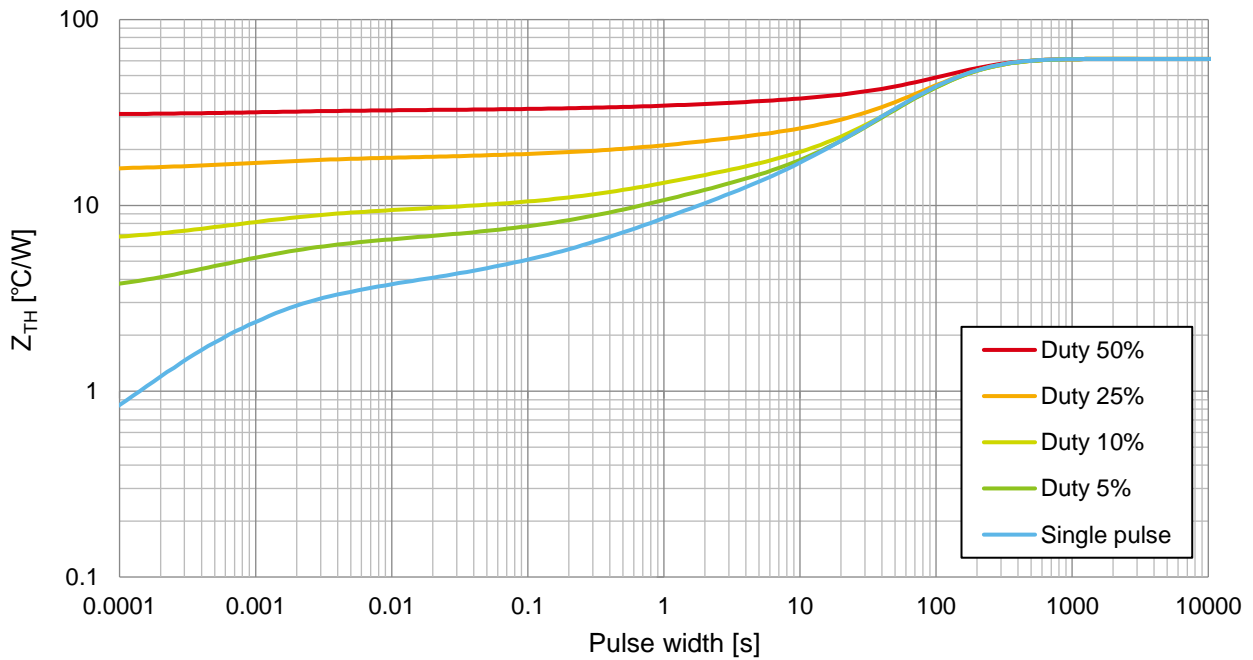


Figure 17. Transient thermal resistance, 1 layer  
Copper foil surface area 300 mm<sup>2</sup>

Transient thermal resistance data, 1 layer (1s), continued

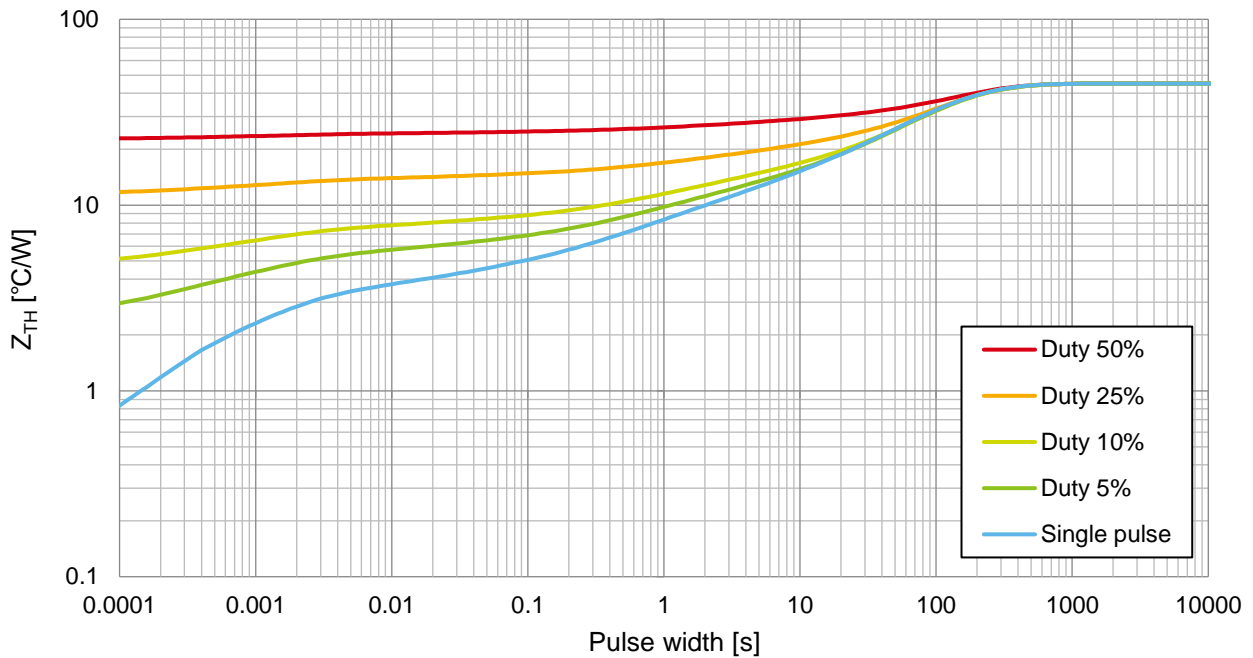


Figure 18. Transient thermal resistance, 1 layer  
Copper foil surface area 600 mm<sup>2</sup>

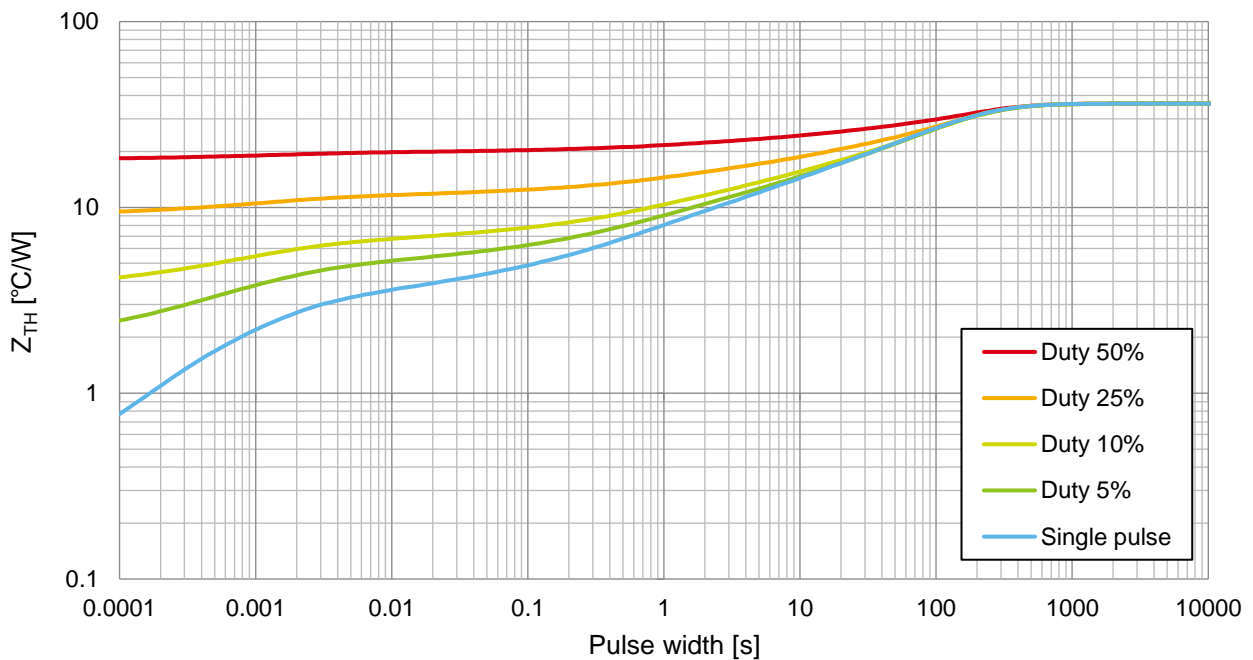


Figure 19. Transient thermal resistance, 1 layer  
Copper foil surface area 1,200 mm<sup>2</sup>

Transient thermal resistance data, 2 layers (2s)

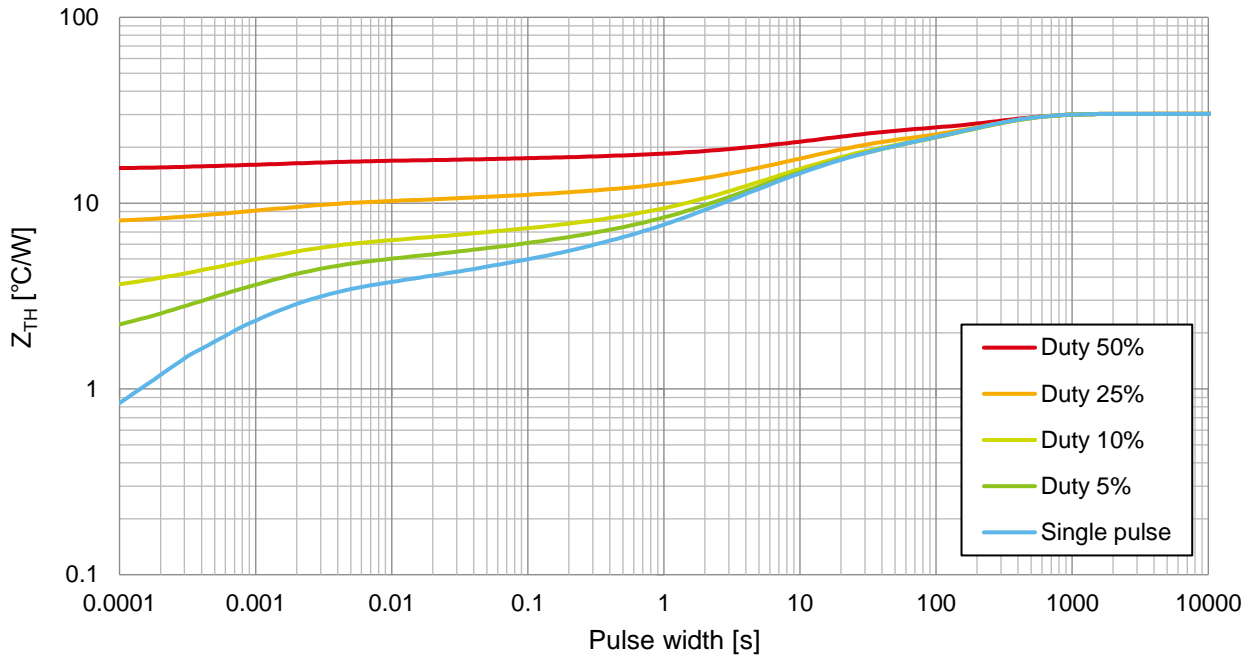


Figure 20. Transient thermal resistance, 2 layers

Transient thermal resistance data, 4 layers (2s2p)

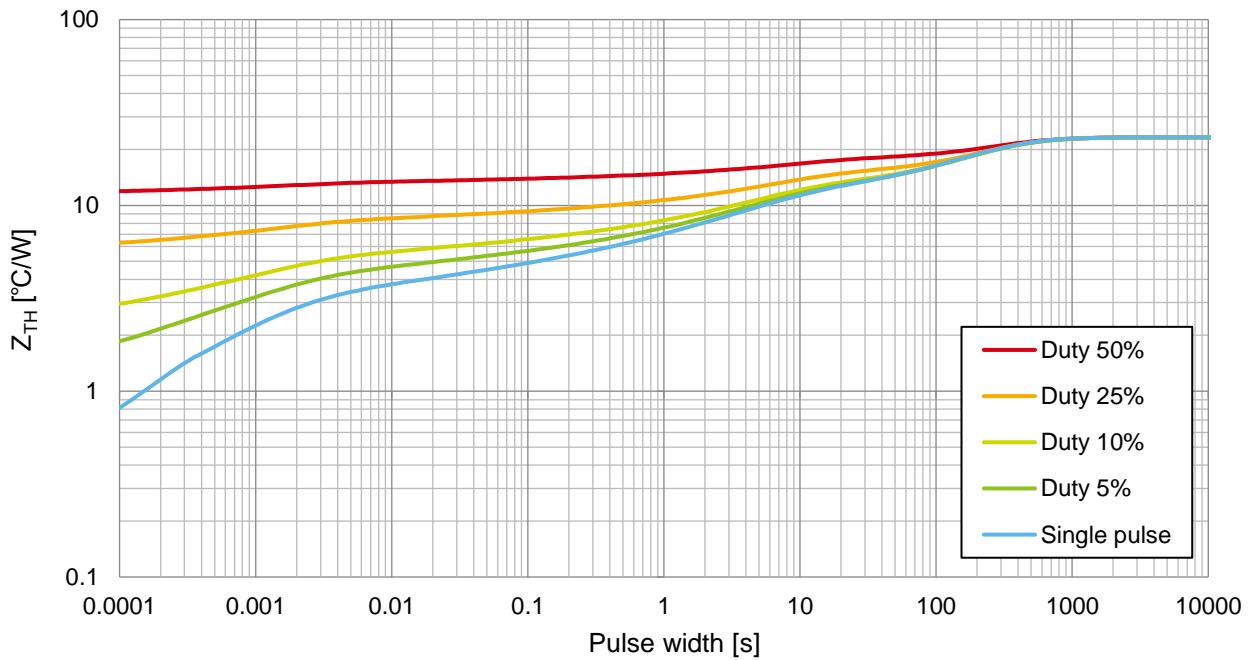


Figure 21. Transient thermal resistance, 4 layers



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