

Thermal Design

TO252 Package Thermal Resistance Information

This application note provides information on the thermal resistances required for performing thermal design using the TO252 package. Use this information for the reference values in the temperature estimation during the initial designing.

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1. Package overview

Package name: TO252

TO252-J3

TO252-5

TO252-J5

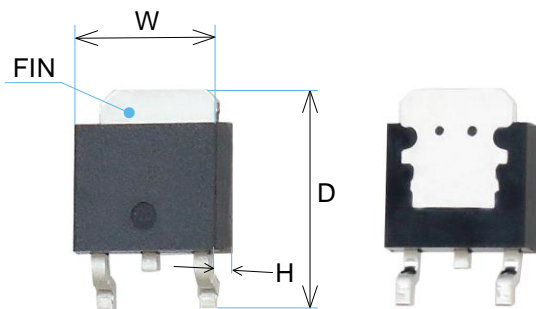
Package group: TO

In this application note, values for TO252-3 are given as a typical package. For packages other than those listed above, the thermal resistance values are strictly different, but the same values can be applied since these values are within the acceptable range for temperature estimation applications in the early design stage.

TO252-3 Outline dimensions

W (typ) D (typ) H (max)

6.5 mm × 9.5 mm × 2.5 mm



2. Thermal resistances and thermal characteristics parameters under environment in accordance with JEDEC standard

2-1. Measurement environment

Content	Standard
Measurement environment	JEDEC STANDARD JESD51-2A (Still Air)
Measurement board standard	JEDEC STANDARD JESD51-3 JESD51-5 JESD51-7

2-2. Numerical values

Configuration	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)
1 layer (1s)	132.2	13
4 layers (2s2p)	23.2	2

θ_{JA} : Thermal resistance between junction temperature T_J and ambient temperature T_A

Ψ_{JT} : Thermal characteristics parameter between junction temperature T_J and package surface center temperature T_T

Note: The thermal resistances and thermal characteristics parameters in this application note are values under a measurement environment in accordance with the JEDEC standard and may not always be consistent with the values for actual equipment. It is necessary to consider variations in the values due to the PCB characteristics, PCB layout, parts layout, chassis shape, surrounding environment, and so on.

2-3. PCB specifications, 1 layer (1s)

Conforms to JEDEC standard JESD51

Item		Value
Board thickness		1.57mm
Board outline dimensions		76.2 mm × 114.3 mm
Board material		FR-4
Trace thickness (Finished thickness)	Top	70 μm (2 oz)
Lead width		0.254mm
Copper foil area	Top	49mm ² (Footprint)

Table 2-3-1. 1-layer PCB specifications



Figure 2-3-1. 1-layer board sectional view

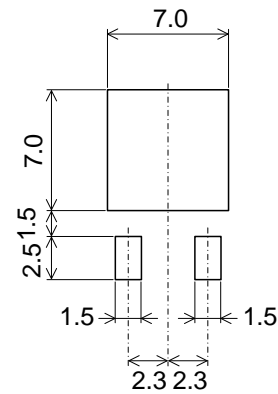


Figure 2-3-2. Footprint dimensions

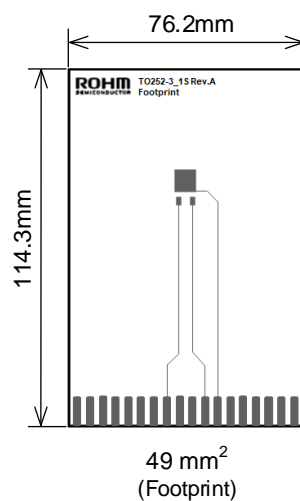


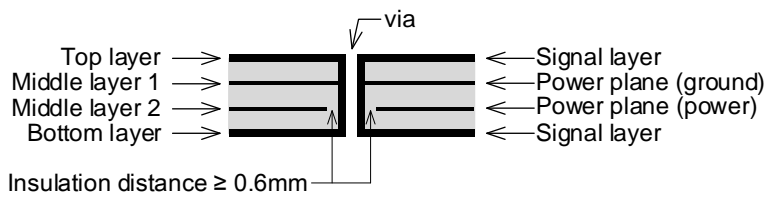
Figure 2-3-3. Top layer

2-4. PCB specifications, 4 layers (2s2p)

Conforms to JEDEC standard JESD51

Item		Value
Board thickness		1.60mm
Board outline dimensions		76.2 mm × 114.3 mm
Board material		FR-4
Trace thickness (Finished thickness)	Top	70 μm (2 oz)
	Middle 1	35 μm (1 oz)
	Middle 2	35 μm (1 oz)
	Bottom	70 μm (2 oz)
Lead width		0.254mm
Copper foil area	Top	49mm ² (Footprint)
	Middle 1	5,505 mm ² (74.2 mm × 74.2 mm)
	Middle 2	5,505 mm ² (74.2 mm × 74.2 mm)
	Bottom	5,505 mm ² (74.2 mm × 74.2 mm)

Table 2-4-1. 4-layer PCB specifications



The middle layers are spaced equally in the thickness direction

Figure 2-4-2. 4-layer board sectional view

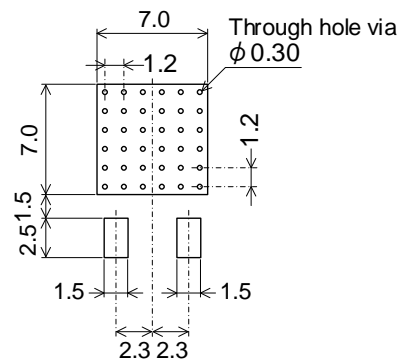


Figure 2-4-3. Footprint dimensions

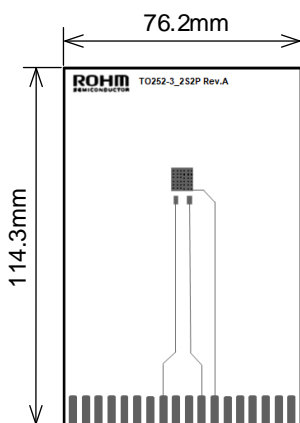


Figure 2-4-4.
Top layer

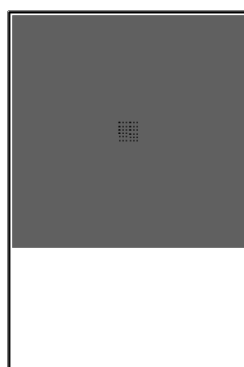


Figure 2-4-5.
Middle 1 layer

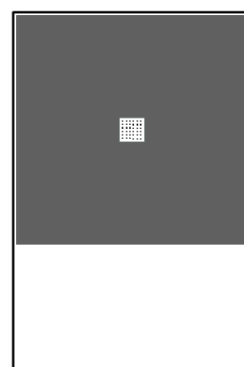


Figure 2-4-6.
Middle 2 layer

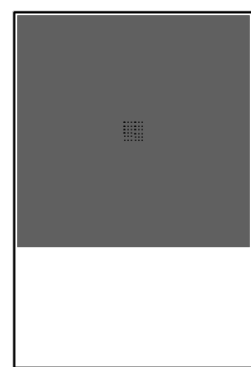


Figure 2-4-7.
Bottom layer

3. Thermal resistances and thermal characteristics parameters with changes in various parameters

3-1. Change in copper foil area

3-1-1. 1 layer

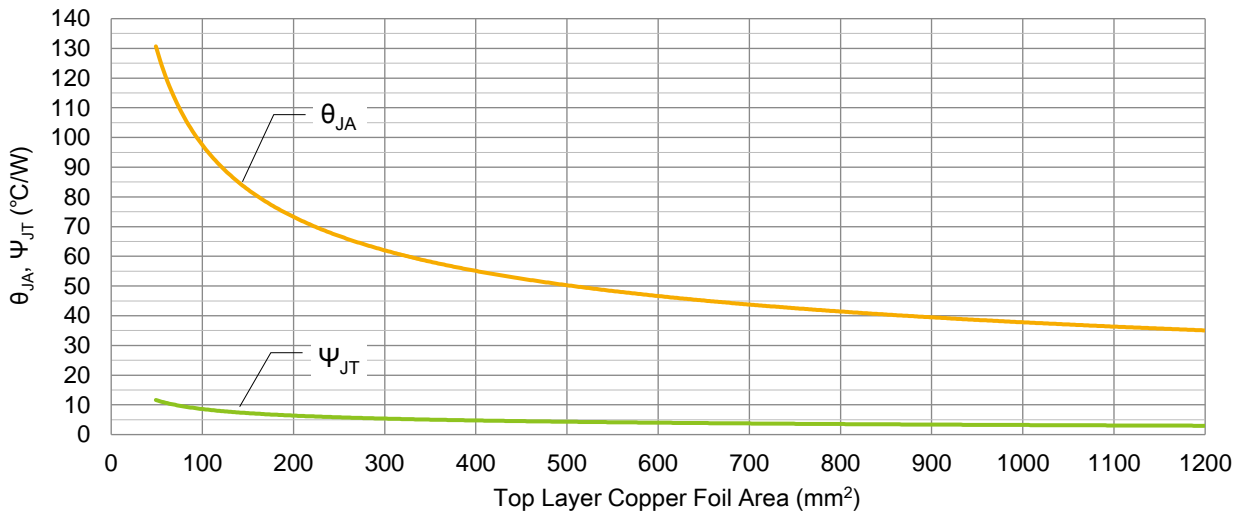


Figure 3-1-1-1. θ_{JA} , ψ_{JT} vs. copper foil area



Figure 3-1-1-2. 1-layer board sectional view

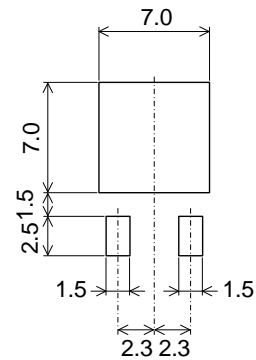


Figure 3-1-1-3. Footprint dimensions

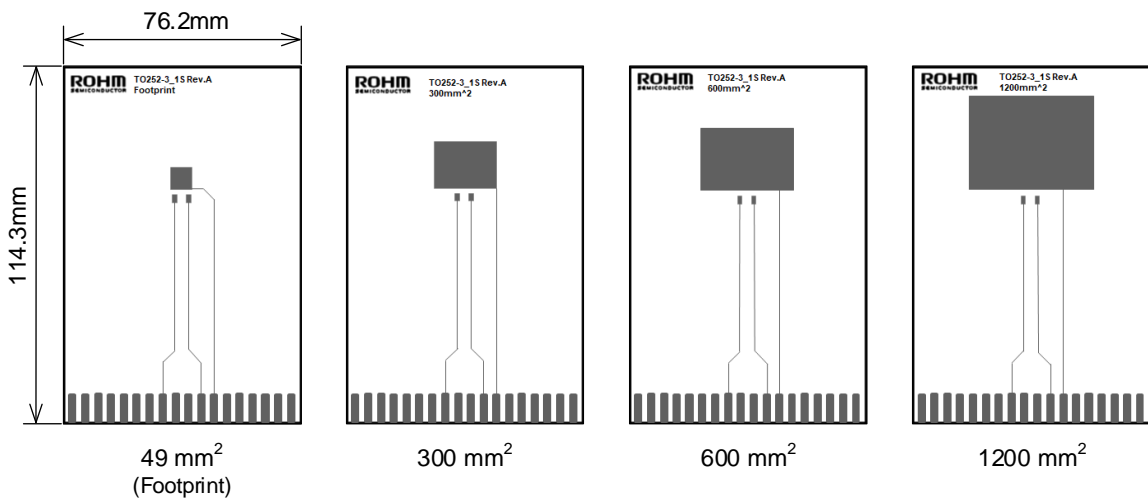


Figure 3-1-1-4. Top layer

3-1. Change in copper foil area (continued)

3-1-2. 2 layers, change in copper foil area of bottom layer only

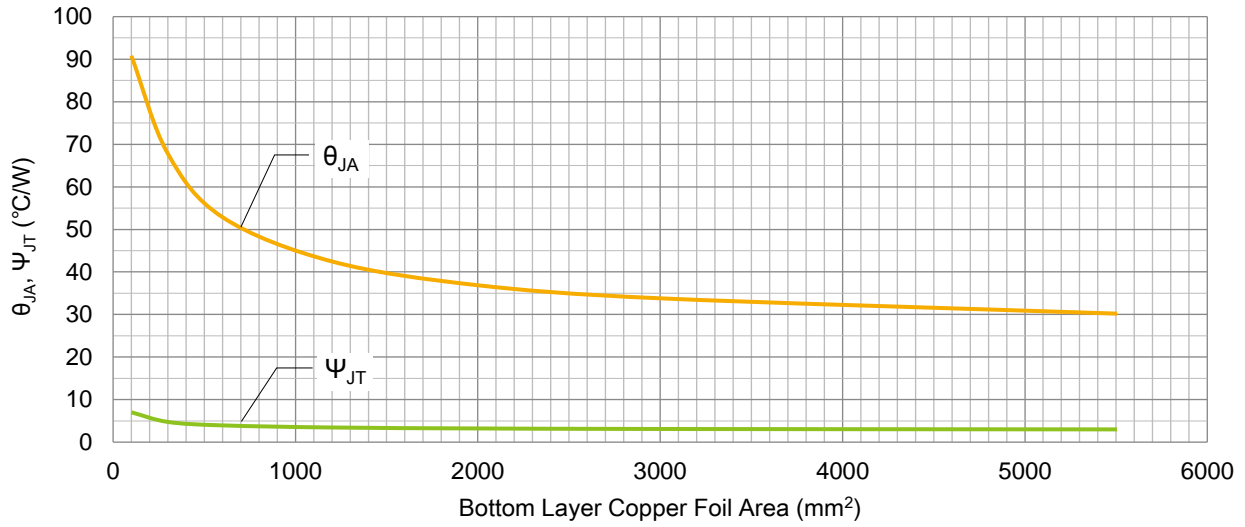


Figure 3-1-2-1. θ_{JA} , ψ_{JT} vs. copper foil area

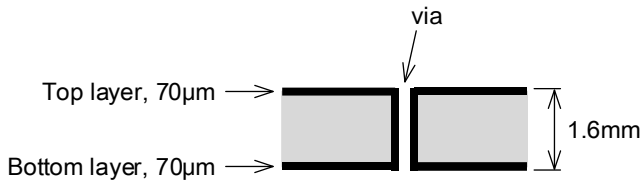


Figure 3-1-2-2. 2-layer board sectional view

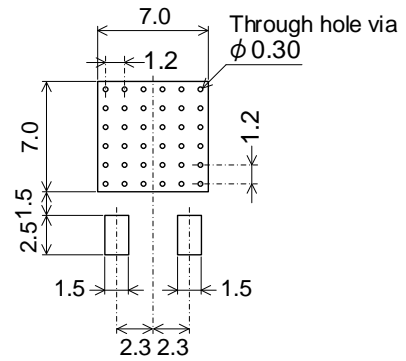


Figure 3-1-2-3. Footprint dimensions

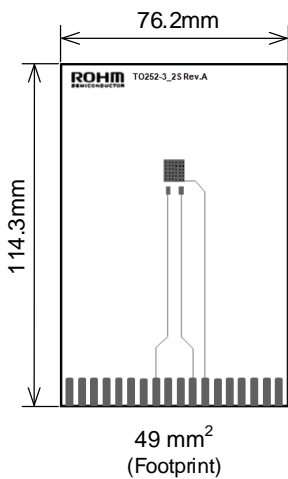


Figure 3-1-2-4. Top layer

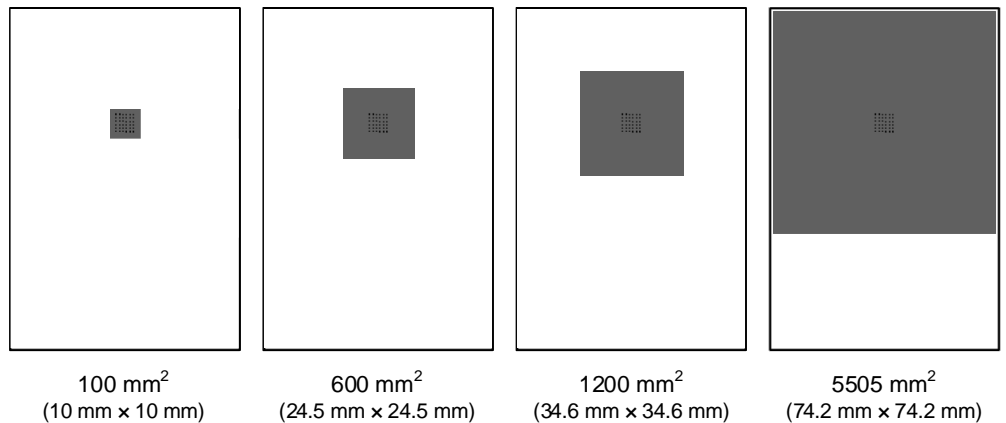


Figure 3-1-2-5. Bottom layer

3-1. Change in copper foil area (continued)

3-1-3. 2 layers, change in copper foil area of multiple layers

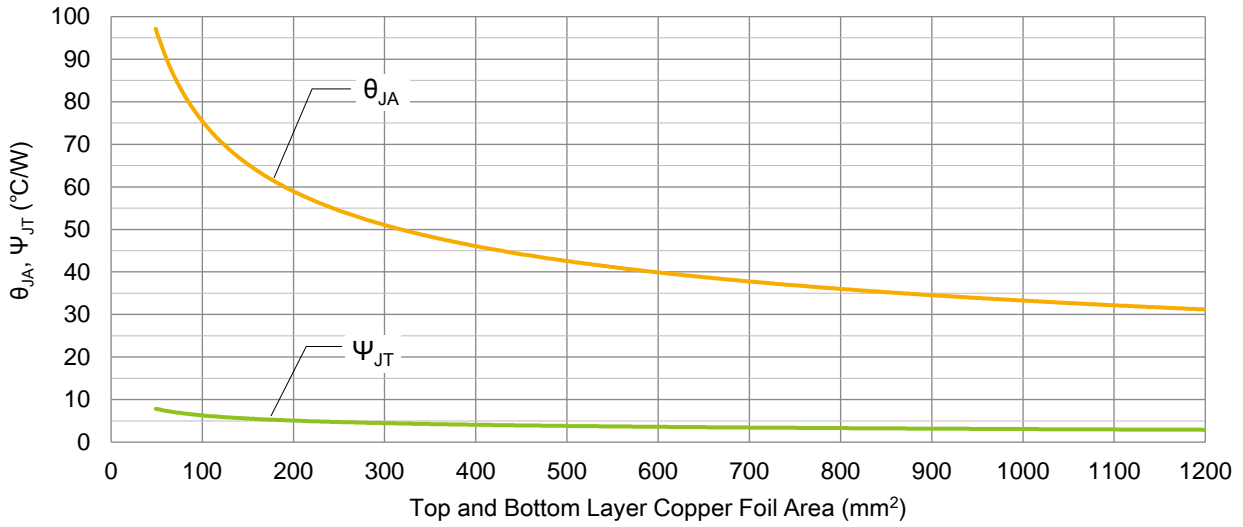


Figure 3-1-3-1. θ_{JA} , Ψ_{JT} vs. copper foil area

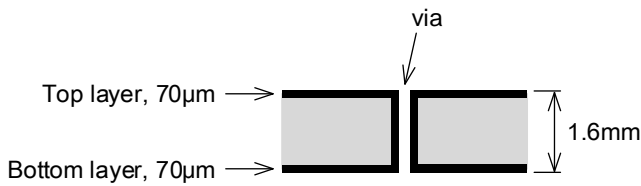


Figure 3-1-3-2. 2-layer board sectional view

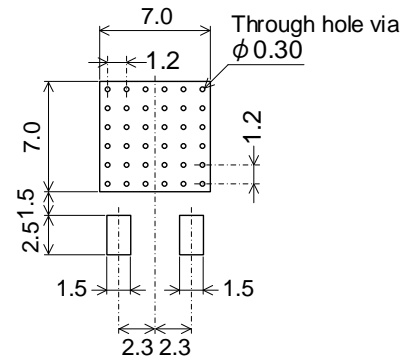


Figure 3-1-3-3. Footprint dimensions

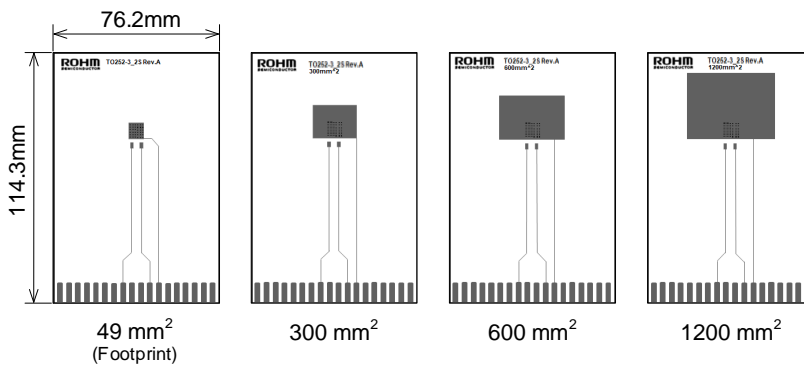


Figure 3-1-3-4. Top layer

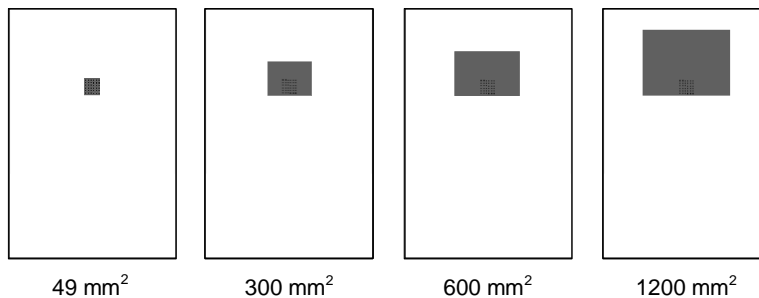


Figure 3-1-3-5. Bottom layer

3-1. Change in copper foil area (continued)

3-1-4. 4 layers, change in copper foil area of multiple layers

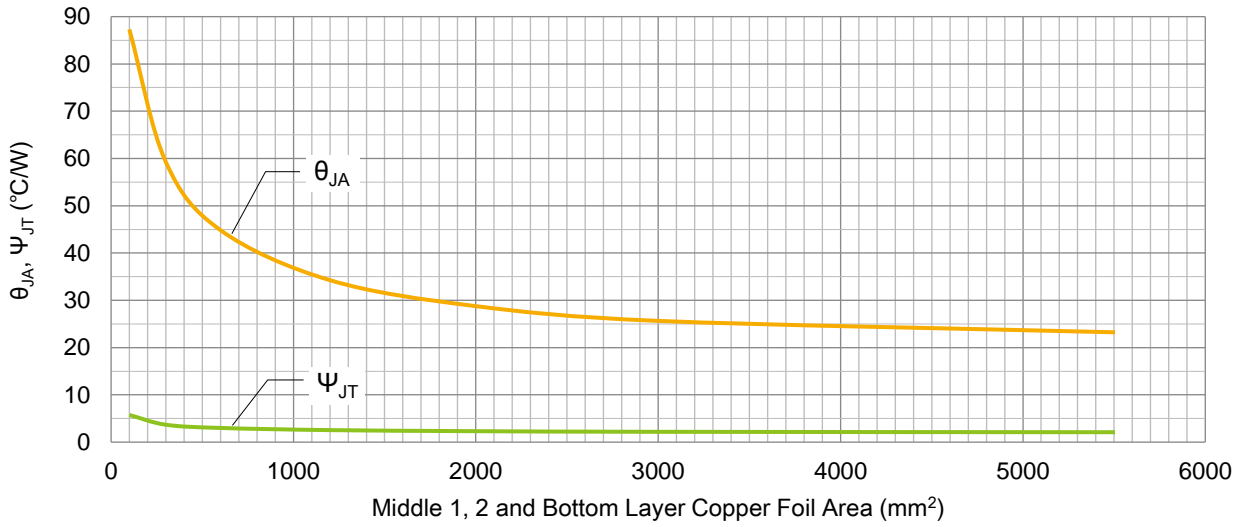
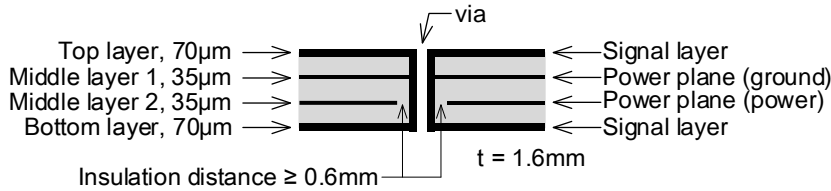


Figure 3-1-4-1. θ_{JA} , ψ_{JT} vs. copper foil area



The middle layers are spaced equally in the thickness direction

Figure 3-1-4-2. 4-layer board sectional view

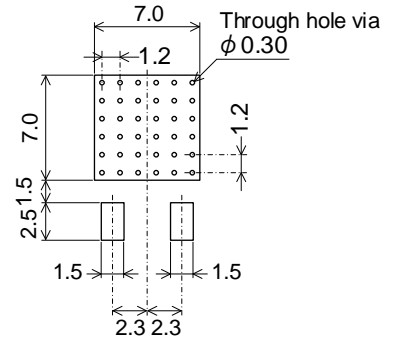


Figure 3-1-4-3. Footprint dimensions

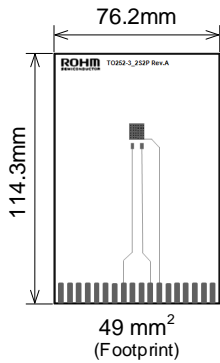


Figure 3-1-4-4. Top layer

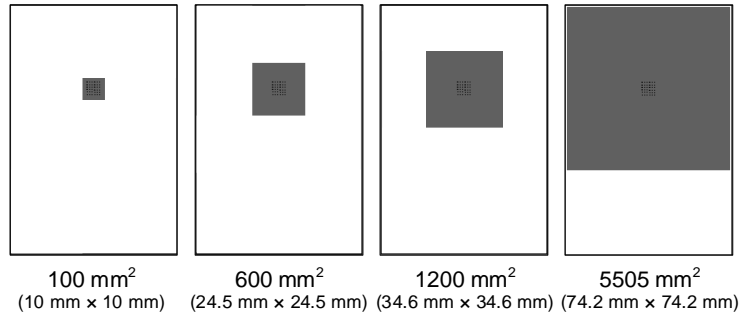


Figure 3-1-4-5. Middle layer 1, Bottom layer

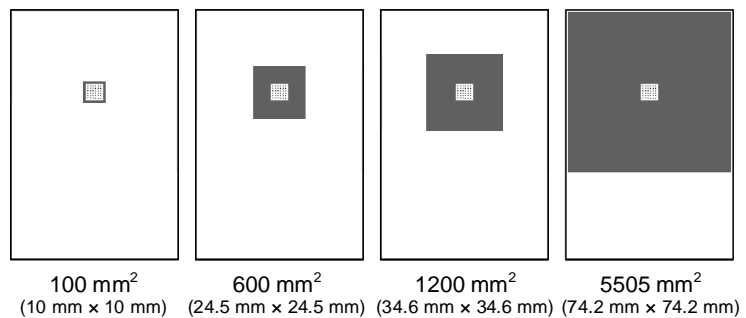


Figure 3-1-4-6. Middle layer 2

3-1. Change in copper foil area (continued)

3-1-5. 4 layers, change in copper foil area of bottom layer only

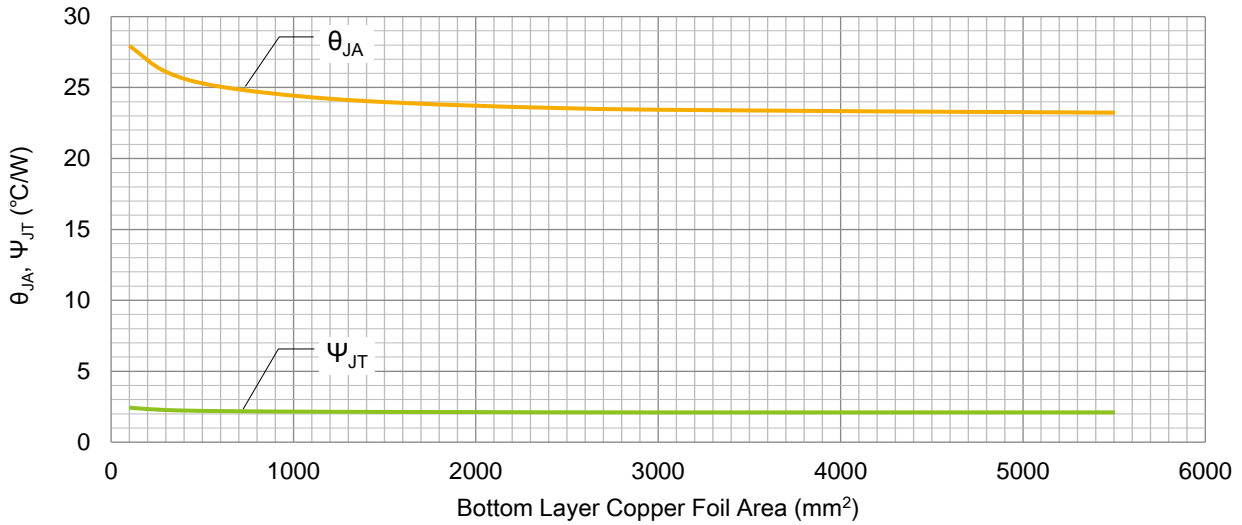


Figure 3-1-5-1. θ_{JA} , ψ_{JT} vs. copper foil area

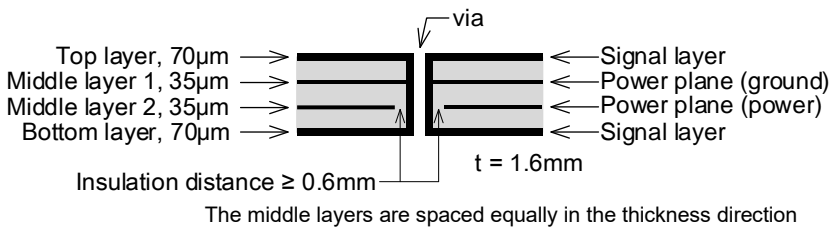


Figure 3-1-5-2. 4-layer board sectional view

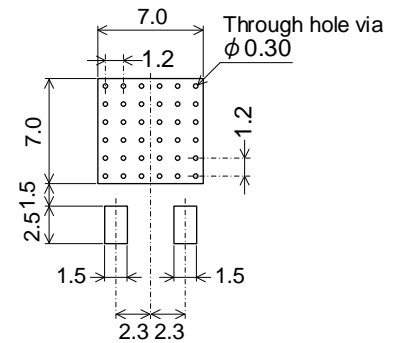


Figure 3-1-5-3. Footprint dimensions

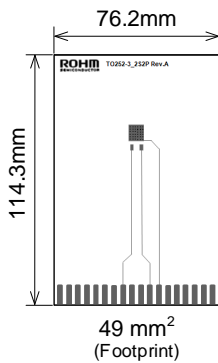


Figure 3-1-5-4. Top layer



Figure 3-1-5-5. Middle layer 1

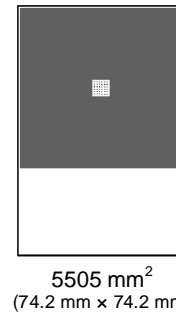


Figure 3-1-5-6. Middle layer 2

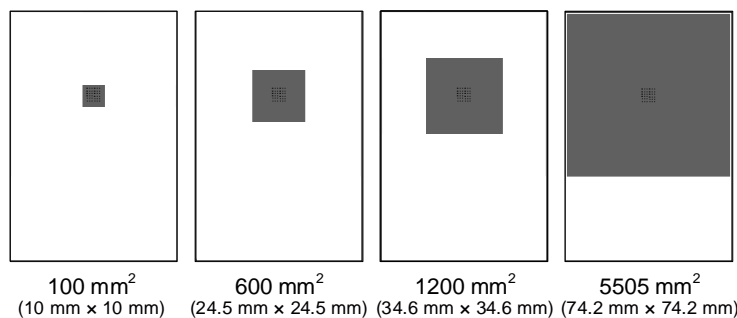


Figure 3-1-5-7. Bottom layer

3-1. Change in copper foil area (continued)

3-1-6. 6 layers, change in copper foil area of multiple layers

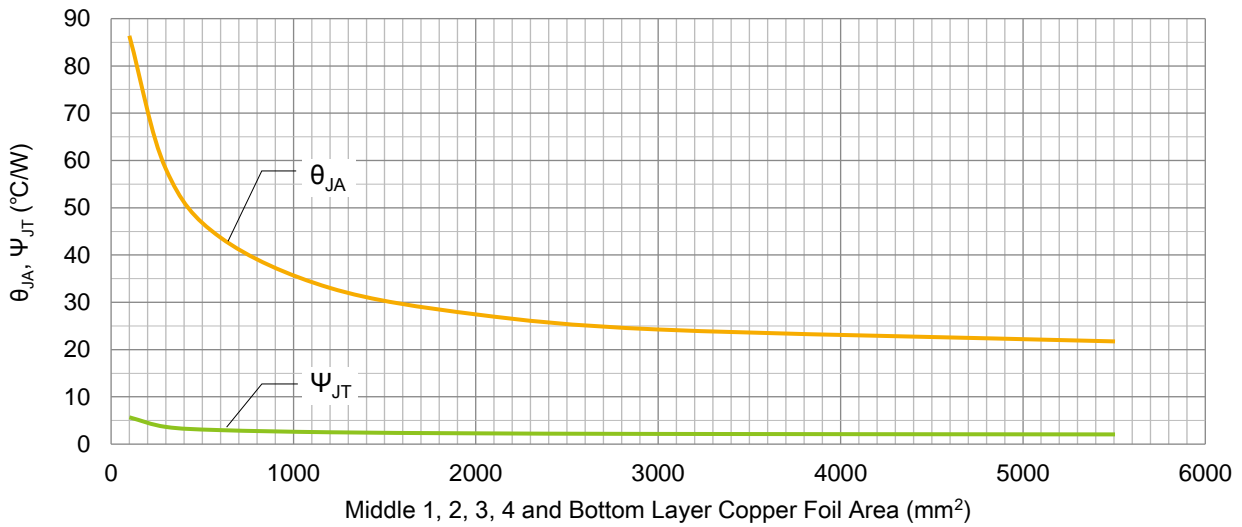
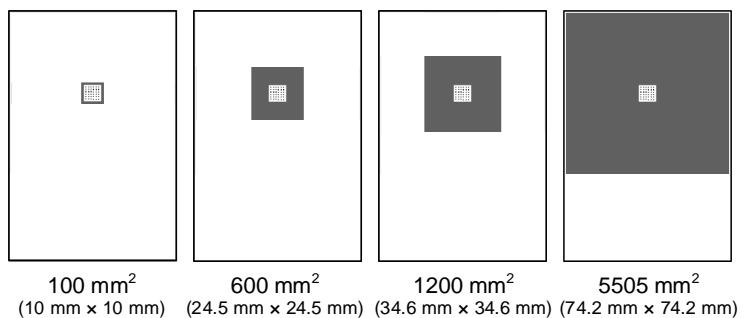
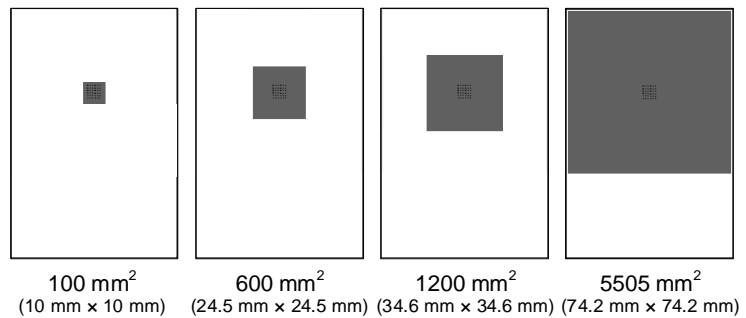
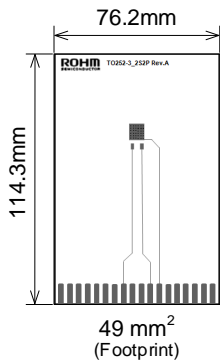
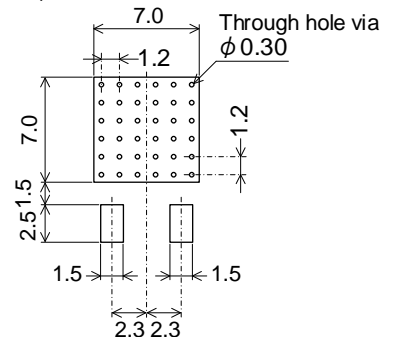
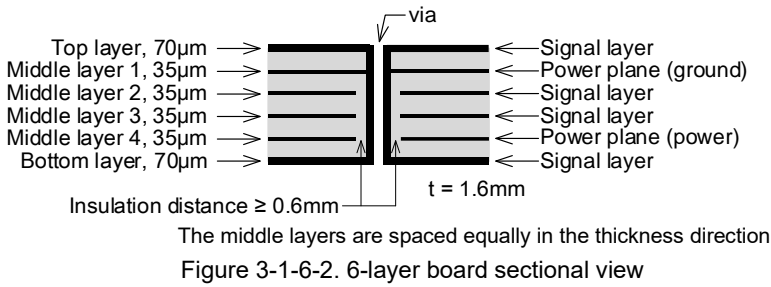


Figure 3-1-6-1. θ_{JA} , ψ_{JT} vs. copper foil area



3-1. Change in copper foil area (continued)

3-1-7. 6 layers, change in copper foil area of bottom layer only

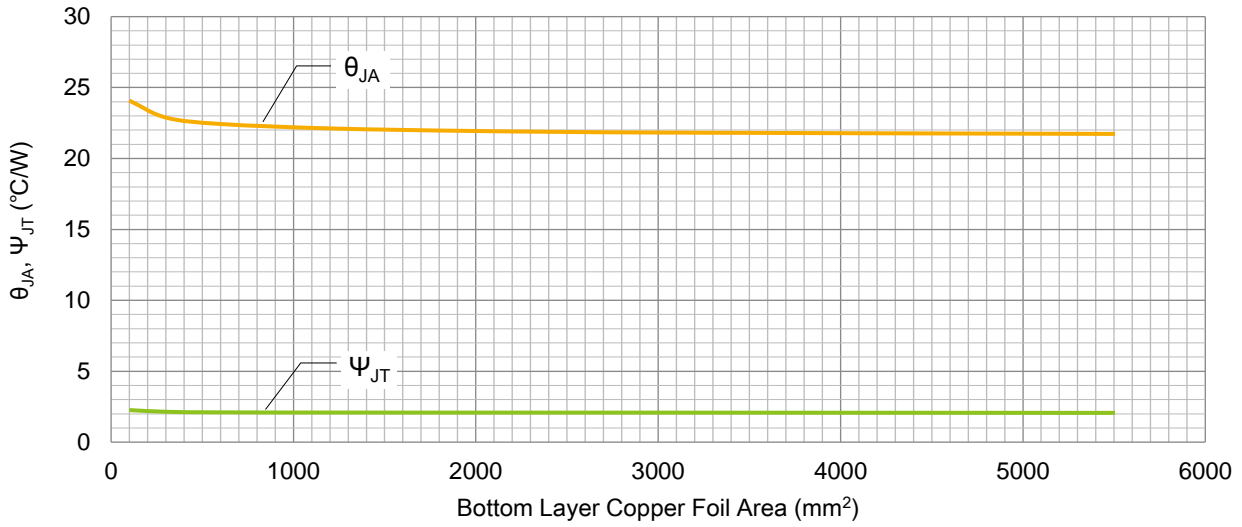
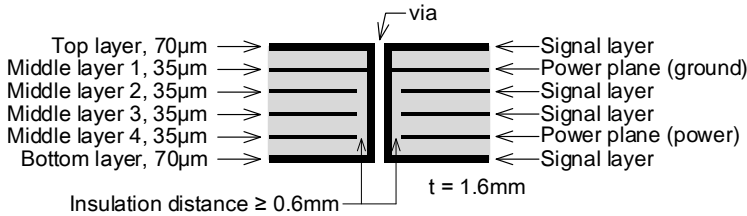


Figure 3-1-7-1. θ_{JA} , ψ_{JT} vs. copper foil area



The middle layers are spaced equally in the thickness direction

Figure 3-1-7-2. 6-layer board sectional view

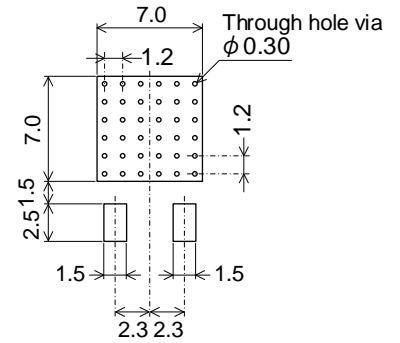


Figure 3-1-7-3. Footprint dimensions

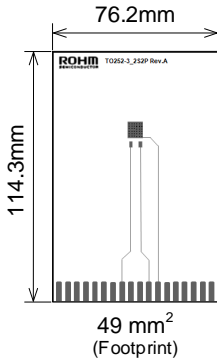


Figure 3-1-7-4. Top layer

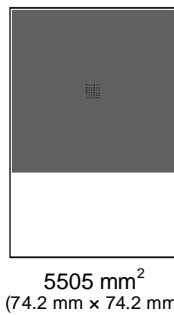


Figure 3-1-7-5. Middle layer 1

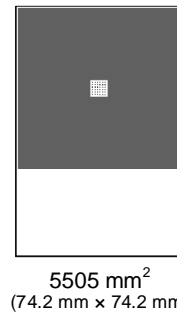


Figure 3-1-7-6. Middle layer 2, 3, 4

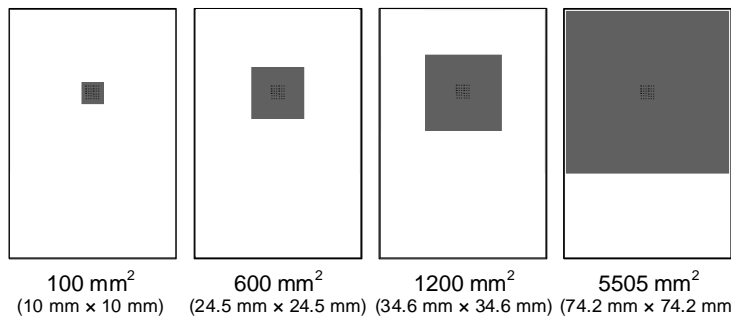


Figure 3-1-7-7. Bottom layer

3-1. Change in copper foil area (continued)

3-1-8. 8 layers, change in copper foil area of multiple layers

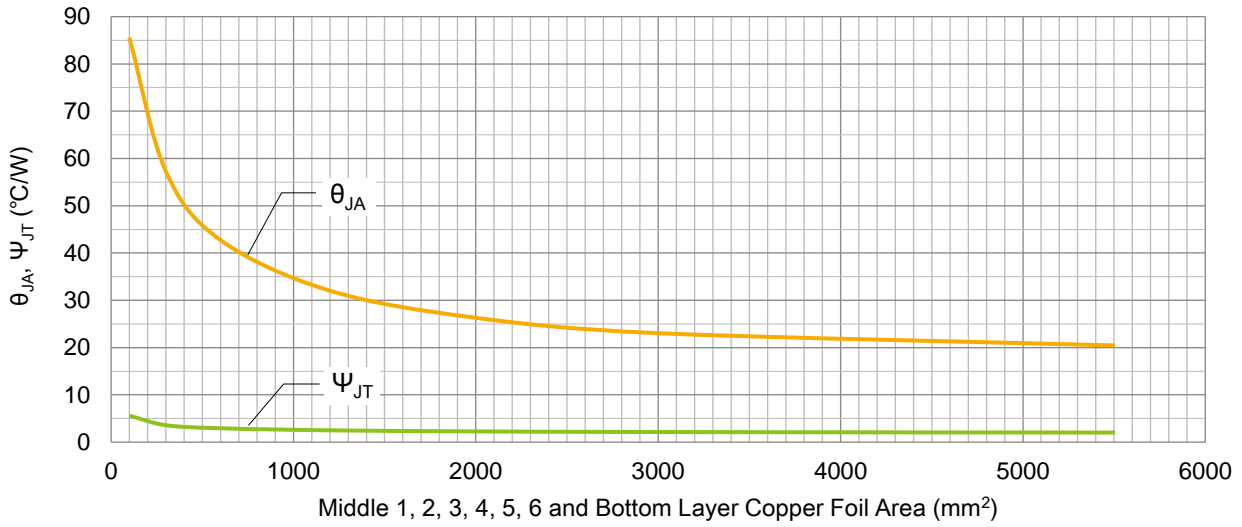
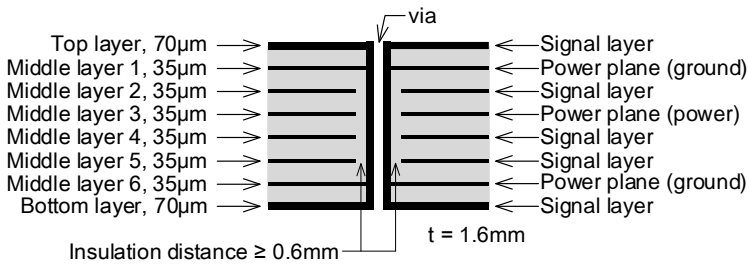


Figure 3-1-8-1. θ_{JA} , Ψ_{JT} vs. copper foil area



The middle layers are spaced equally in the thickness direction
Figure 3-1-8-2. 8-layer board sectional view

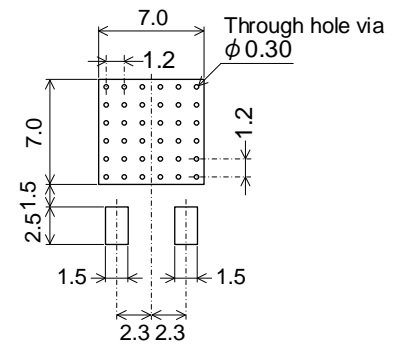


Figure 3-1-8-3. Footprint dimensions

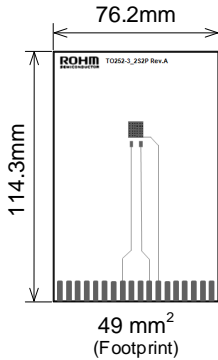


Figure 3-1-8-4. Top layer

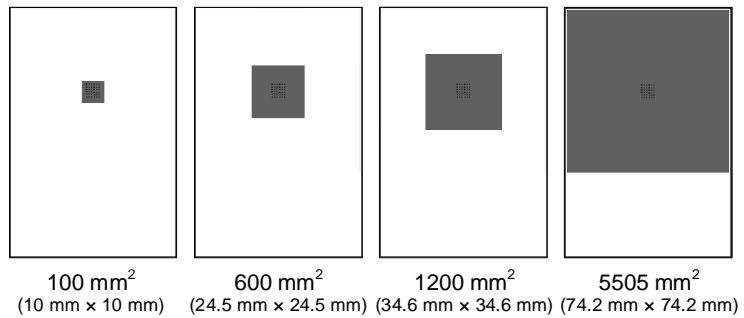


Figure 3-1-8-5. Middle layer 1, 6, Bottom layer

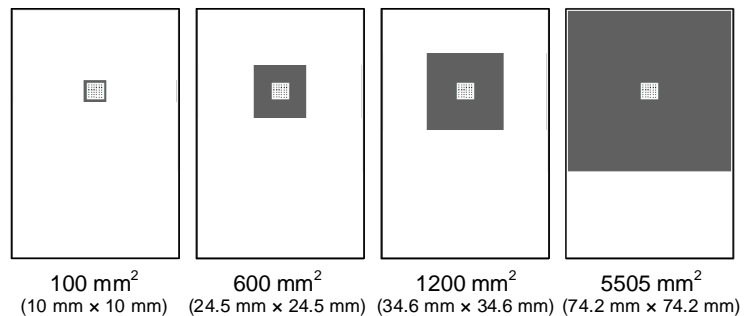


Figure 3-1-8-6. Middle layer 2, 3, 4, 5

3-1. Change in copper foil area (continued)

3-1-9. 8 layers, change in copper foil area of bottom layer only

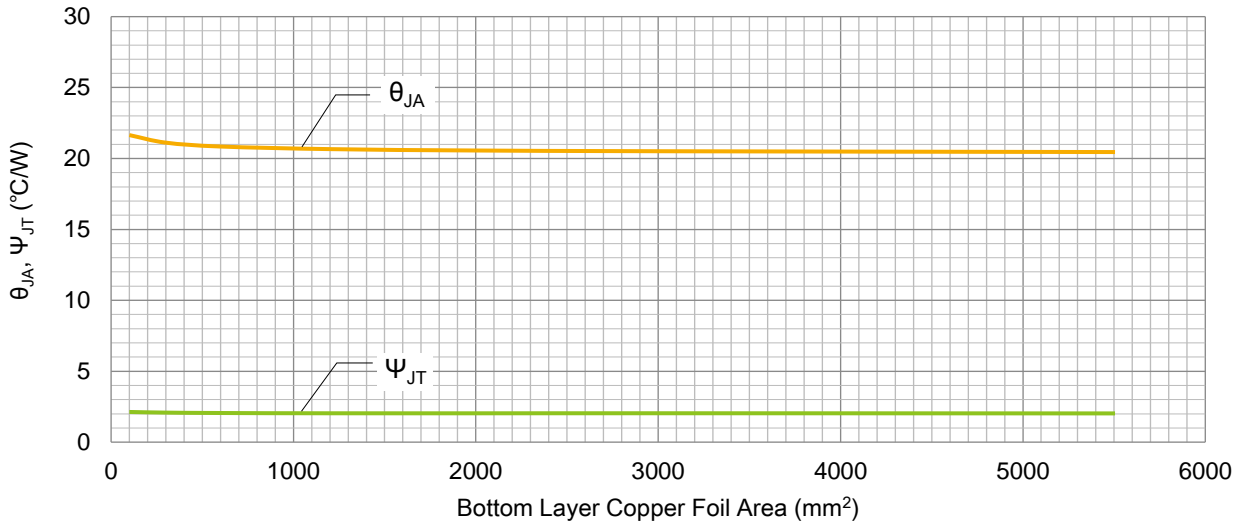


Figure 3-1-9-1. θ_{JA}, Ψ_{JT} vs. copper foil area

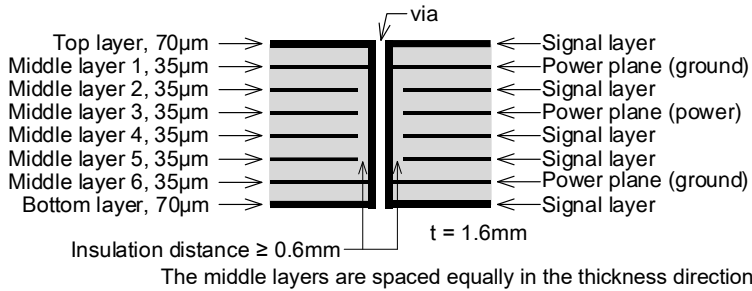


Figure 3-1-9-2. 8-layer board sectional view

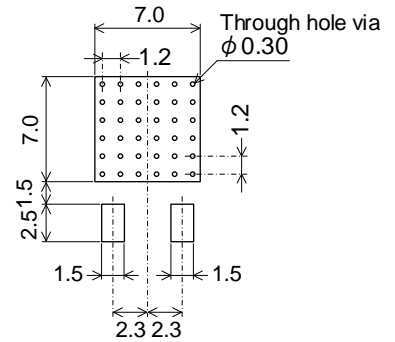


Figure 3-1-9-3. Footprint dimensions

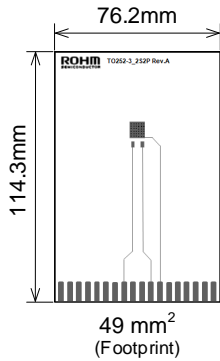


Figure 3-1-9-4. Top layer

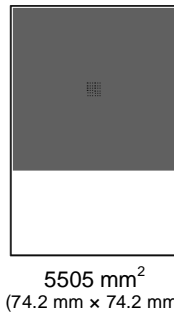


Figure 3-1-9-5. Middle layer 1, 6

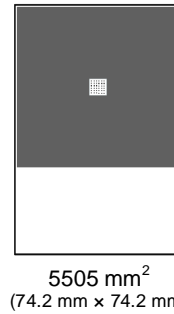


Figure 3-1-9-6. Middle layer 2, 3, 4, 5

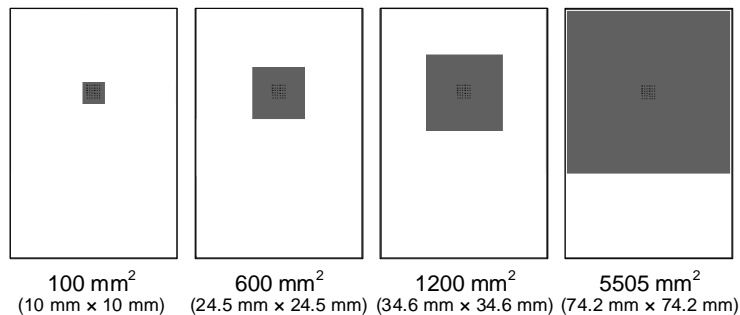


Figure 3-1-9-6. Bottom layer

3-2. Change in copper foil thickness

3-2-1. 1 layer

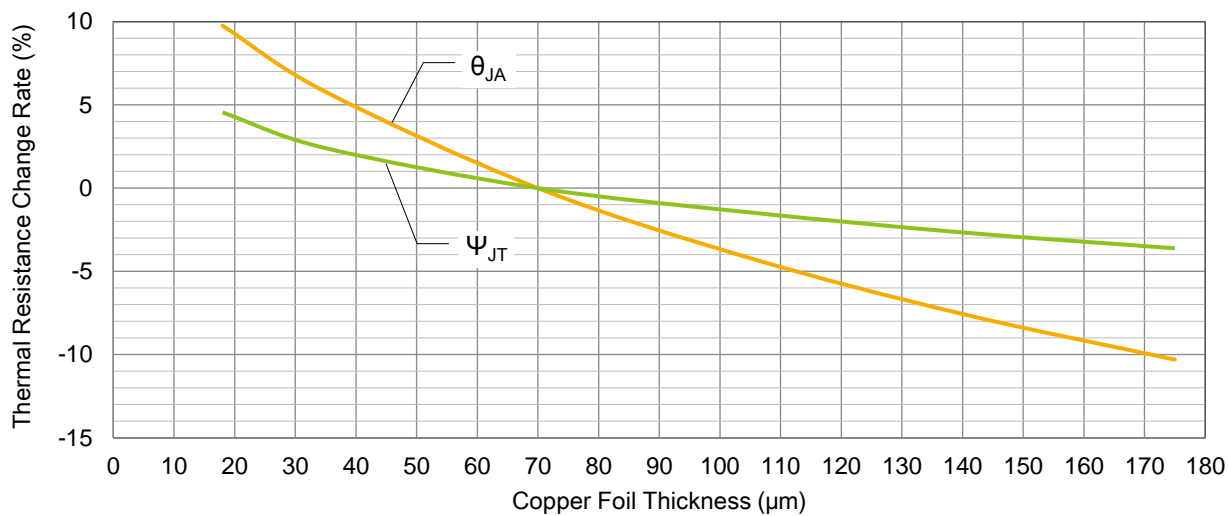


Figure 3-2-1-1. Variation rates of θ_{JA} and Ψ_{JT} vs. copper foil thickness

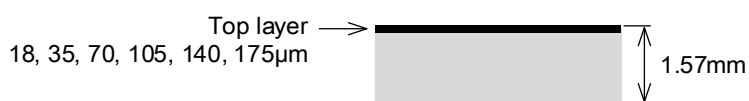


Figure 3-2-1-2. 1-layer board sectional view

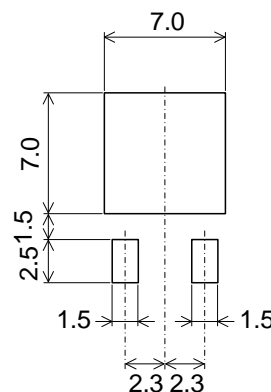


Figure 3-2-1-3. Footprint dimensions

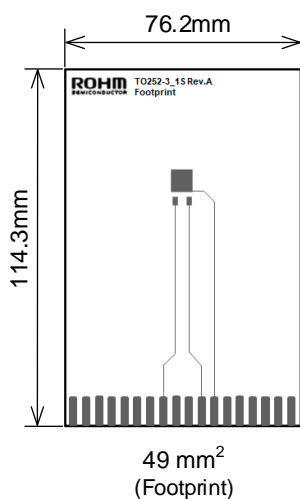


Figure 3-2-1-4. Top layer

3-2. Change in copper foil thickness (continued)

3-2-2. 2 layers

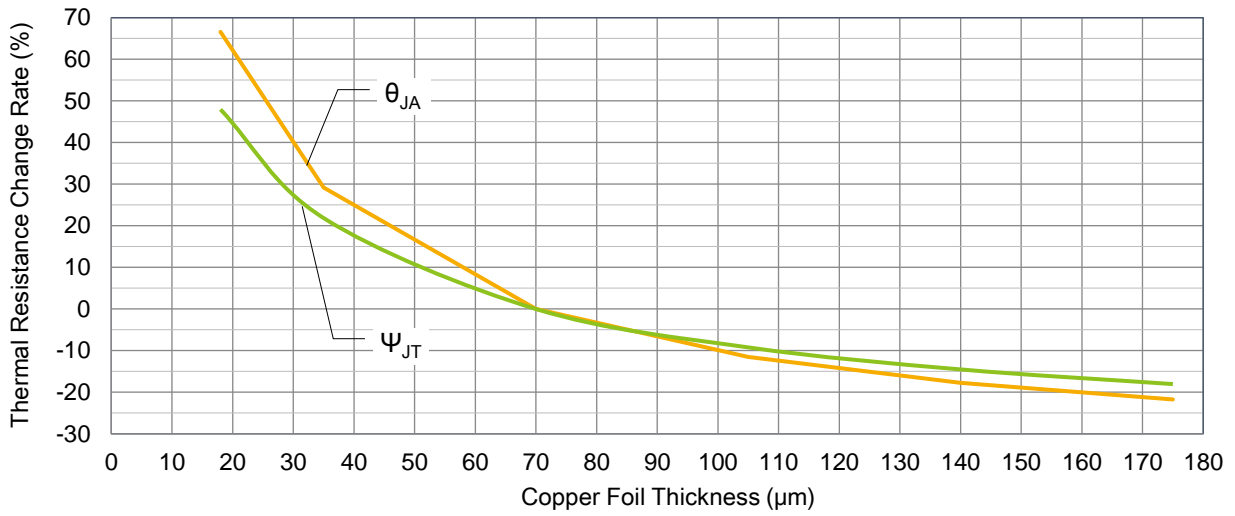


Figure 3-2-2-1. Variation rates of θ_{JA} and ψ_{JT} vs. copper foil thickness

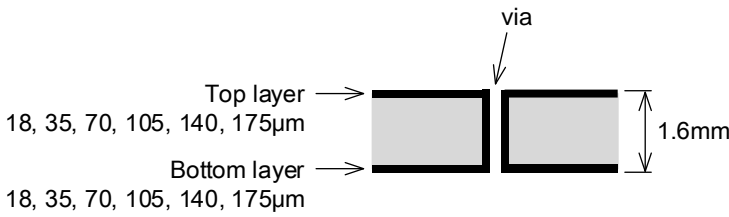


Figure 3-2-2-2. 2-layer board sectional view

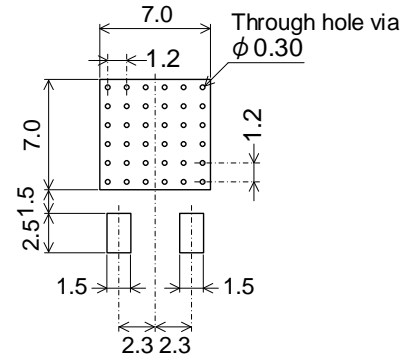


Figure 3-2-2-3. Footprint dimensions

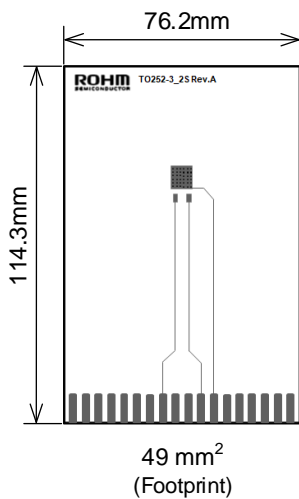


Figure 3-2-2-4. Top layer

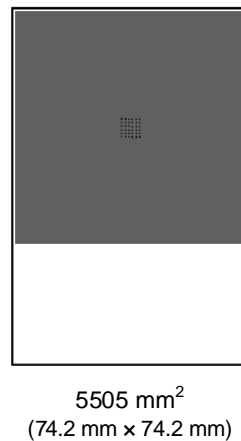


Figure 3-2-2-5. Bottom layer

3-2. Change in copper foil thickness (continued)

3-2-3. 4 layers

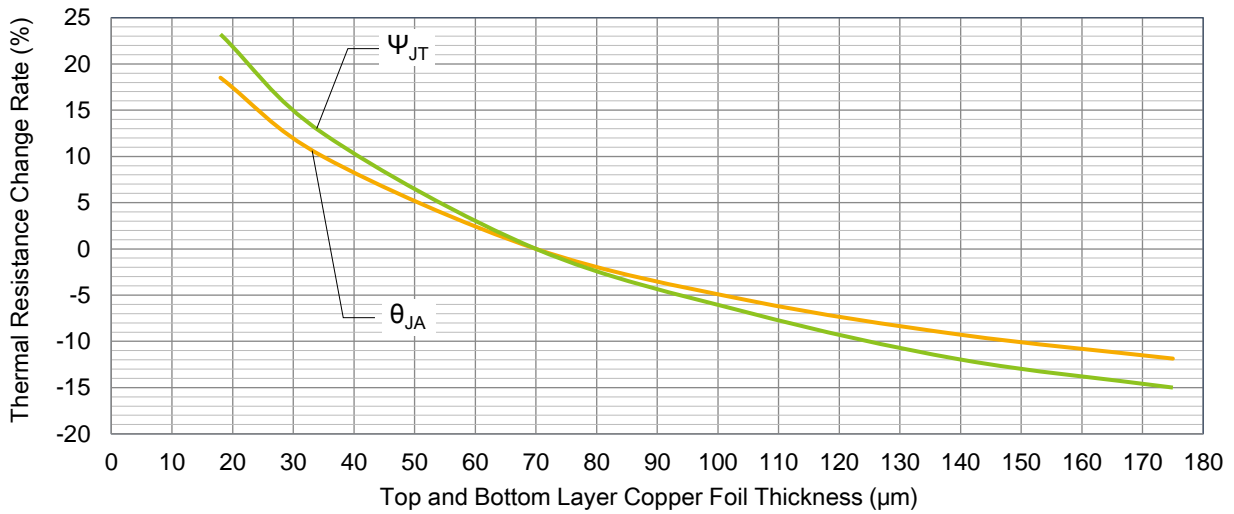


Figure 3-2-3-1. Variation rates of θ_{JA} and Ψ_{JT} vs. copper foil thickness

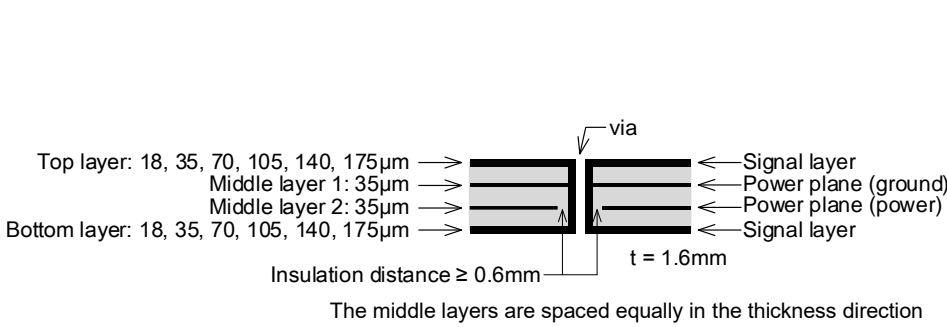


Figure 3-2-3-2. 4-layer board sectional view

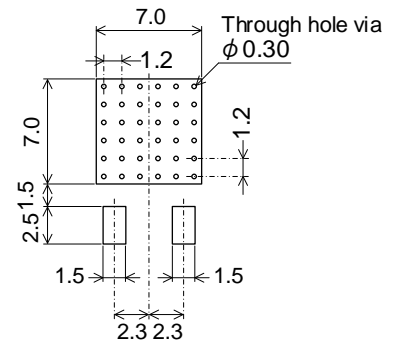


Figure 3-2-3-3. Footprint dimensions

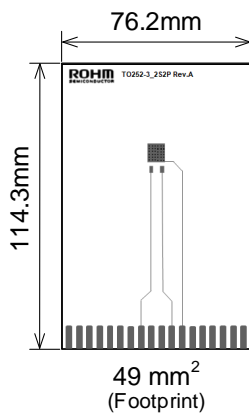


Figure 3-2-3-4. Top layer

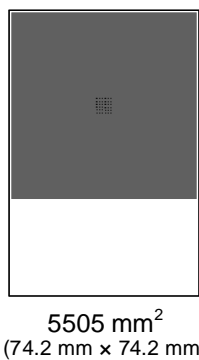


Figure 3-2-3-5. Middle layer 1

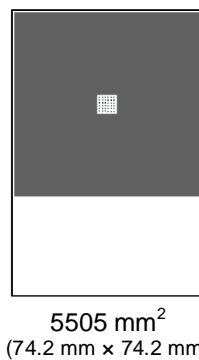


Figure 3-2-3-6. Middle layer 2

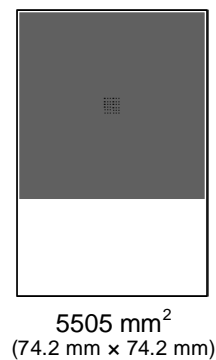


Figure 3-2-3-7. Bottom layer

3-3. Thermal via configuration

3-3-1. 2 layers

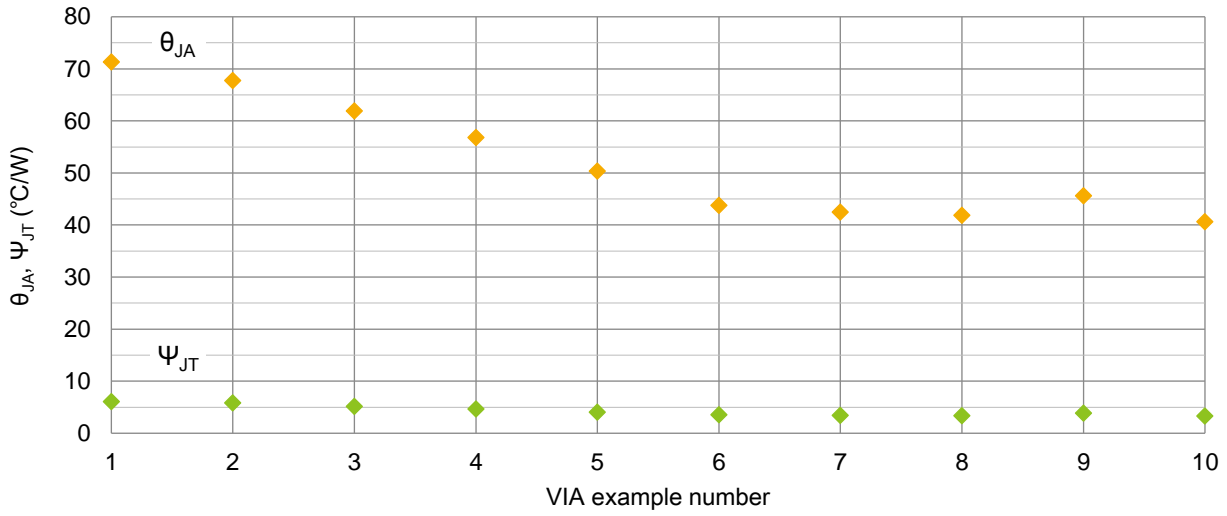


Figure 3-3-1-1. θ_{JA} , ψ_{JT} vs. thermal via configuration

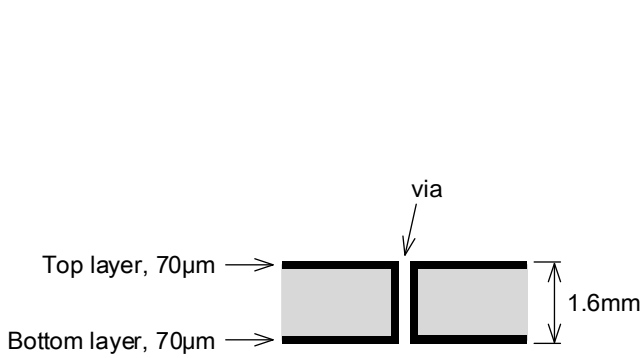


Figure 3-3-1-2. 2-layer board sectional view

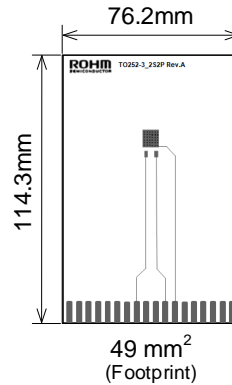


Figure 3-3-1-3. Top layer

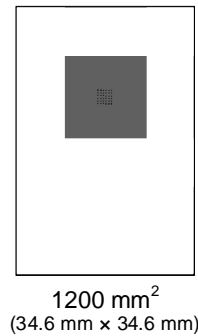
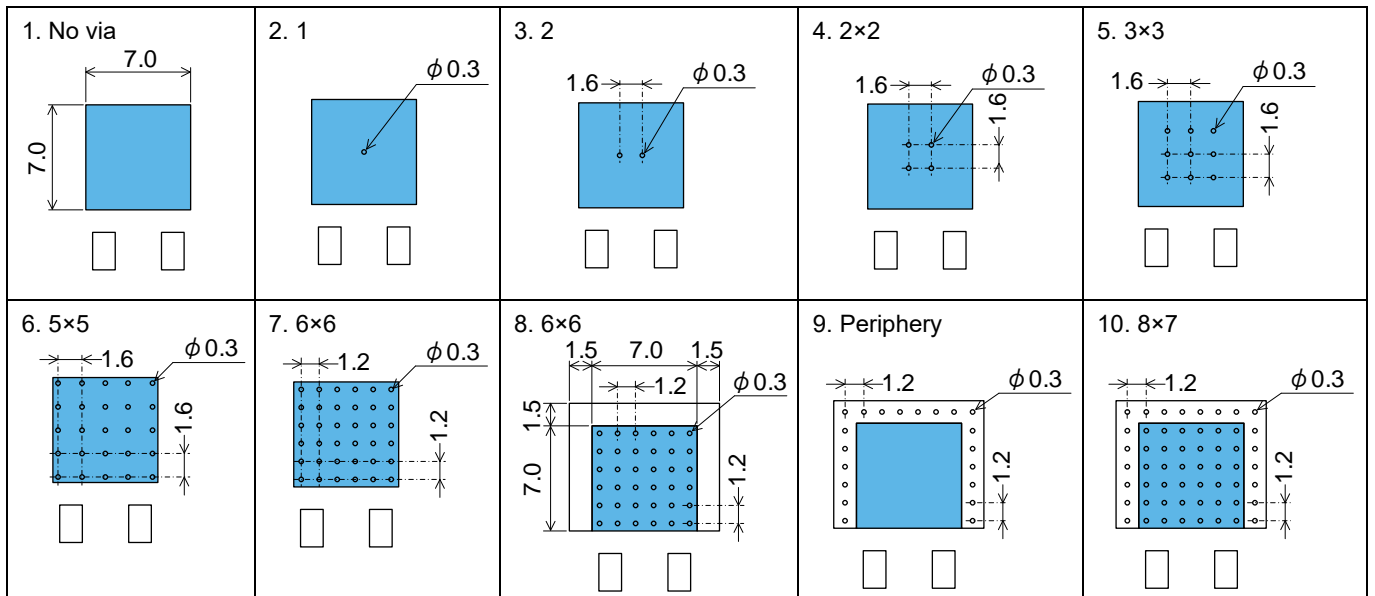


Figure 3-3-1-4. Bottom layer

Numbers for via examples

■ represents solder on the FIN area



3-3. Thermal via configuration (continued)

3-3-2. 4 layers

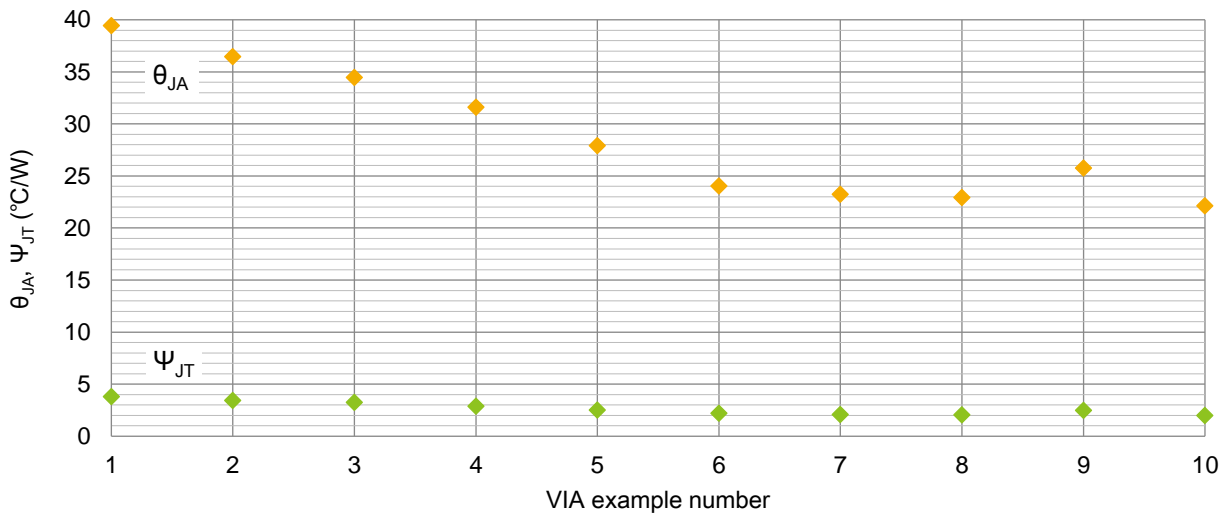


Figure 3-3-2-1. θ_{JA} , ψ_{JT} vs. thermal via configuration

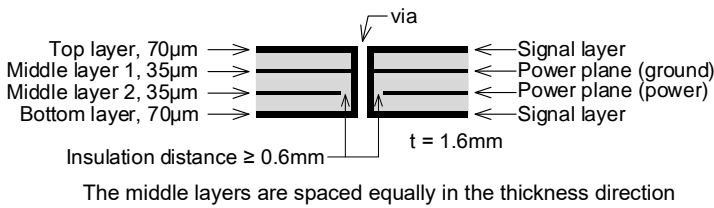


Figure 3-3-2-2. 4-layer board sectional view

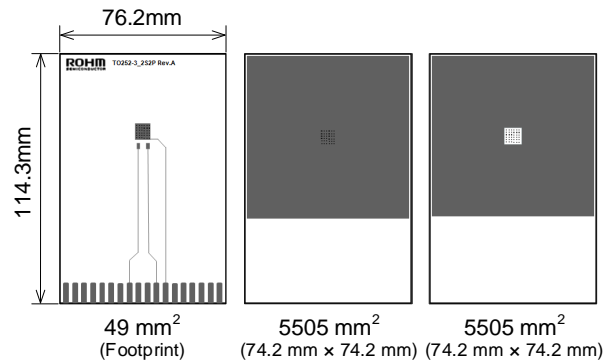
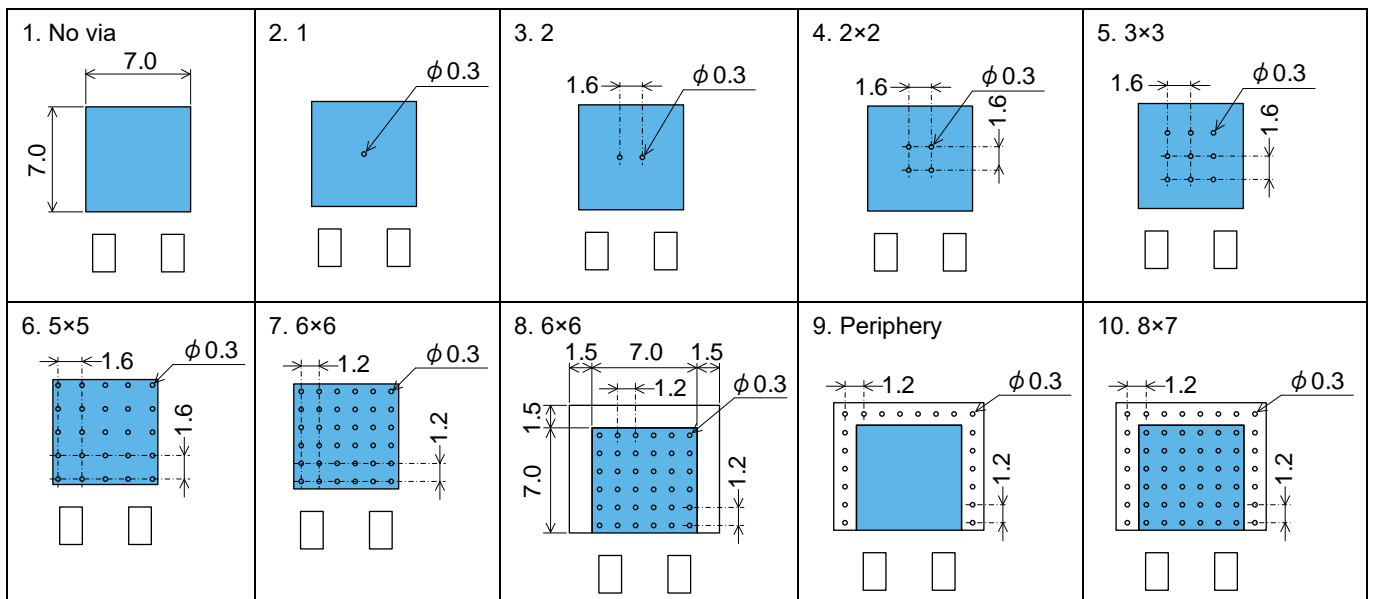


Figure 3-3-2-3. Top layer
 Figure 3-3-2-4. Middle layer 1, Bottom layer
 Figure 3-3-2-5. Middle layer 2

Numbers for via examples

■ represents solder on the FIN area



3-4. Change in board thickness

3-4-1. 1 layer

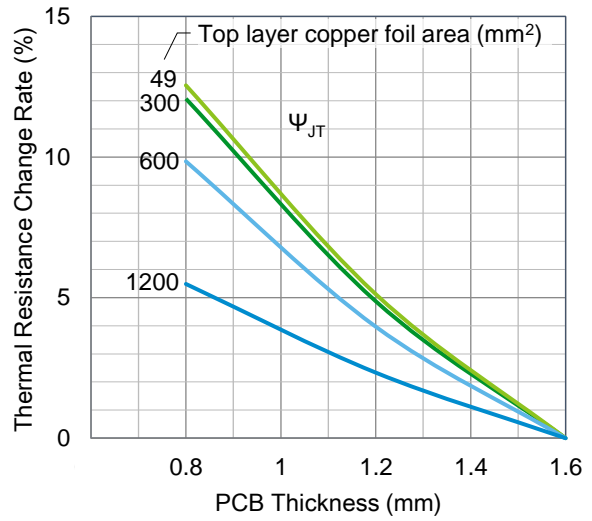
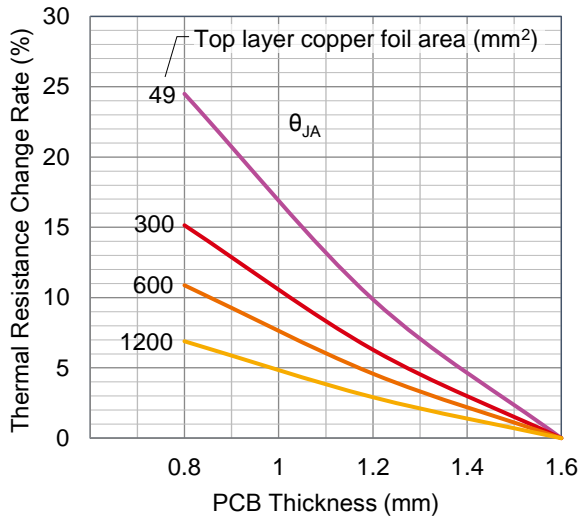


Figure 3-4-1-1. Variation rates of θ_{JA} and Ψ_{JT} vs. board thickness



Figure 3-4-1-2. 1-layer board sectional view

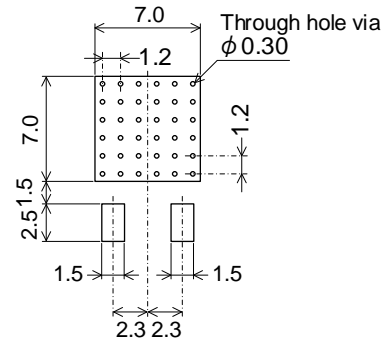


Figure 3-4-1-3. Footprint dimensions

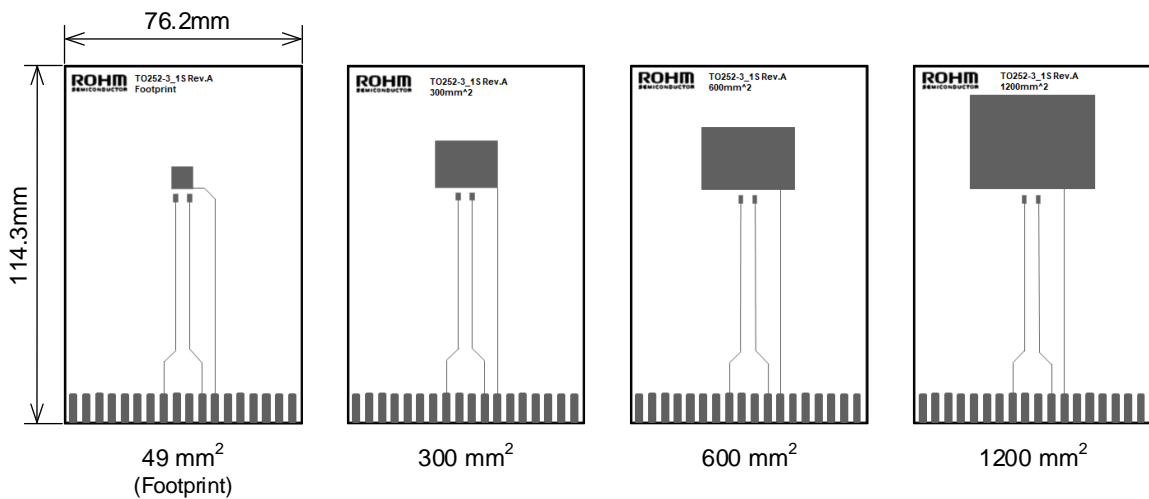


Figure 3-4-1-4. Top layer

3-4. Change in board thickness (continued)

3-4-2. 2 layers

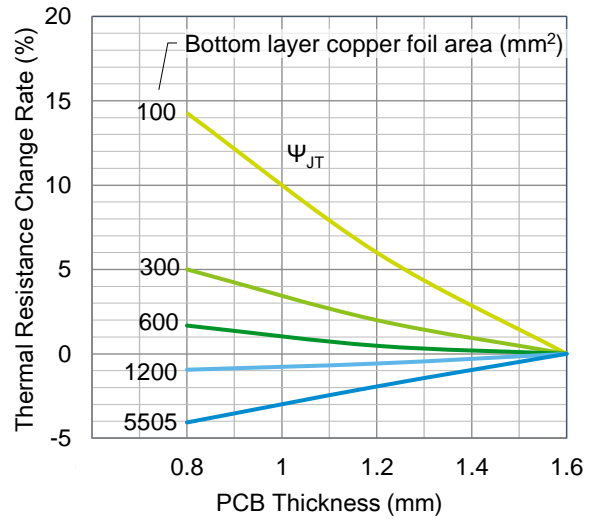
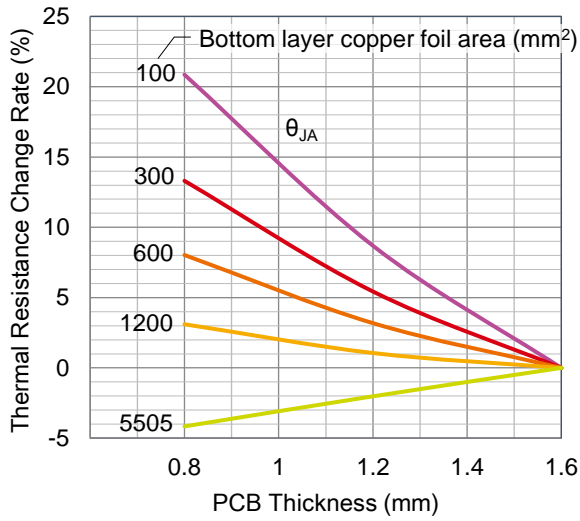


Figure 3-4-2-1. Variation rates of θ_{JA} and Ψ_{JT} vs. board thickness

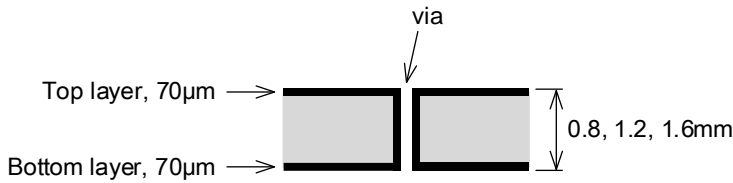


Figure 3-4-2-2. 2-layer board sectional view

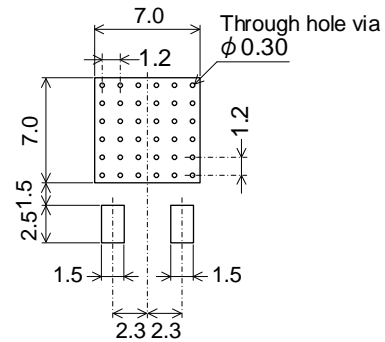


Figure 3-4-2-3. Footprint dimensions

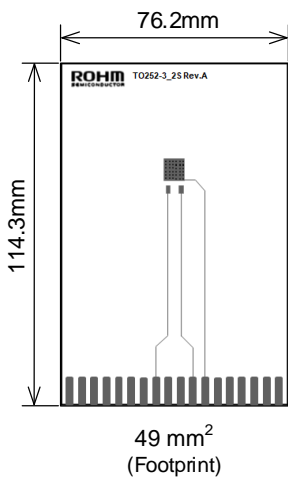


Figure 3-4-2-4. Top layer

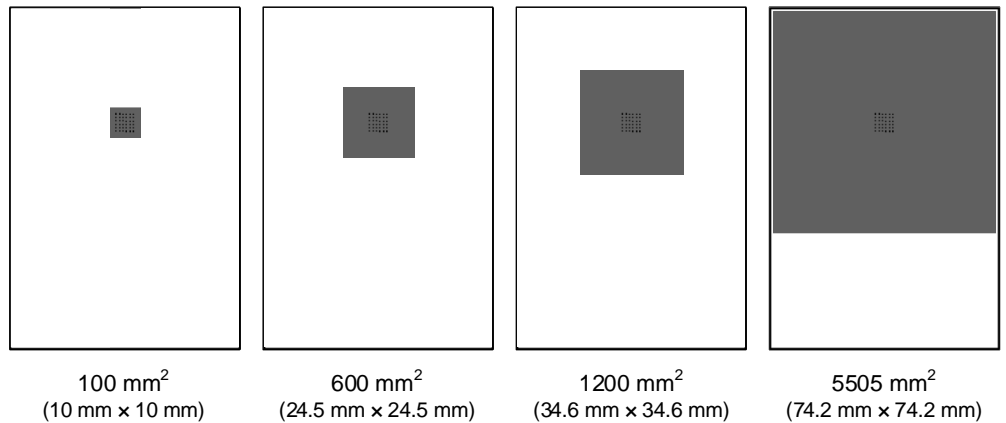


Figure 3-4-2-5. Bottom layer

3-4. Change in board thickness (continued)

3-4-3. 4 layers

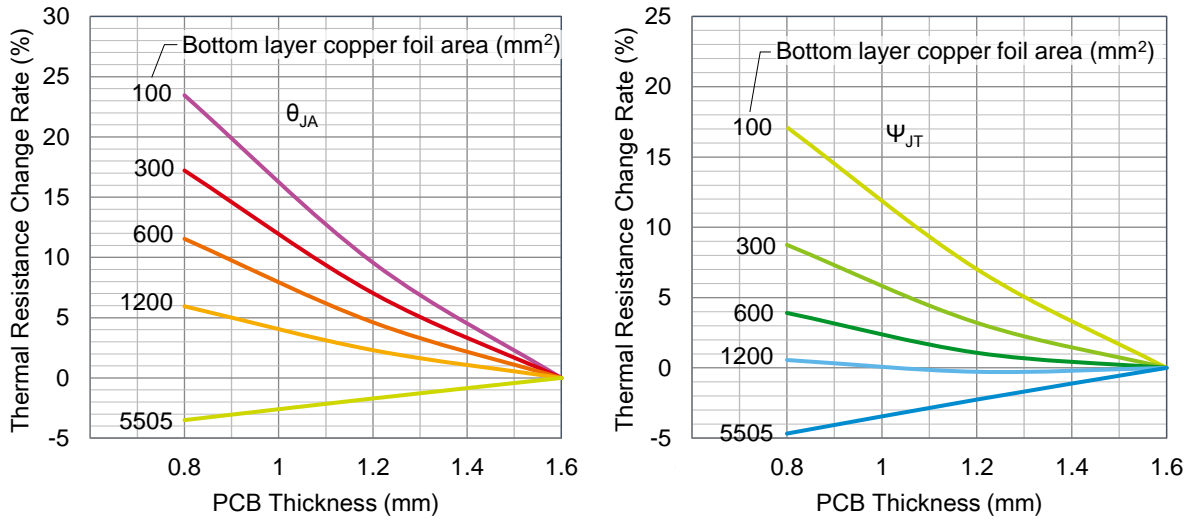


Figure 3-4-3-1. Variation rates of θ_{JA} and Ψ_{JT} vs. board thickness

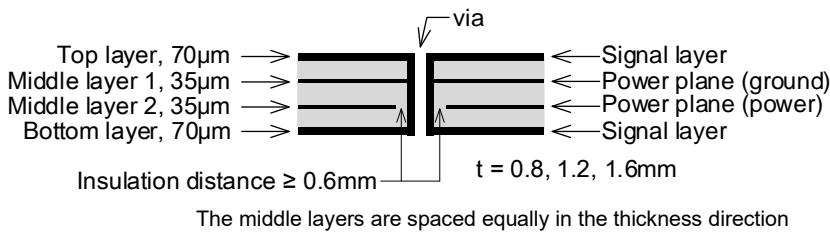


Figure 3-4-3-2. 4-layer board sectional view

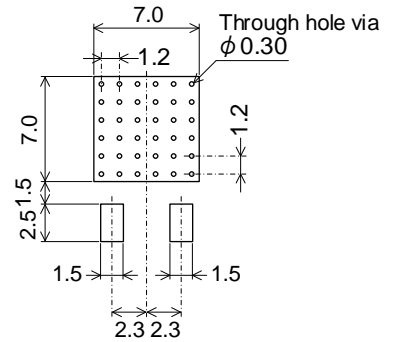


Figure 3-4-3-3. Footprint dimensions

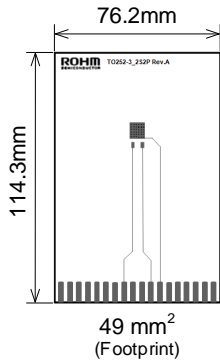


Figure 3-4-3-4. Top layer

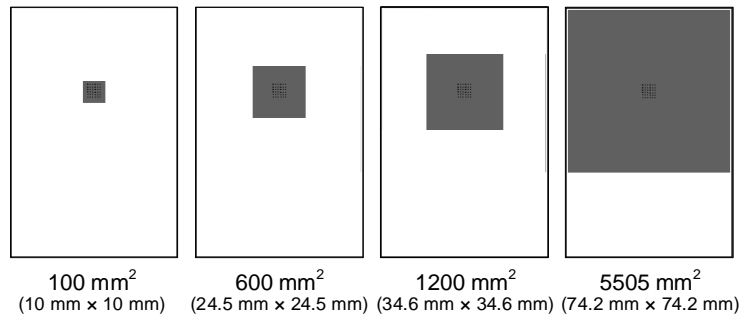


Figure 3-4-3-5. Middle layer 1, Bottom layer

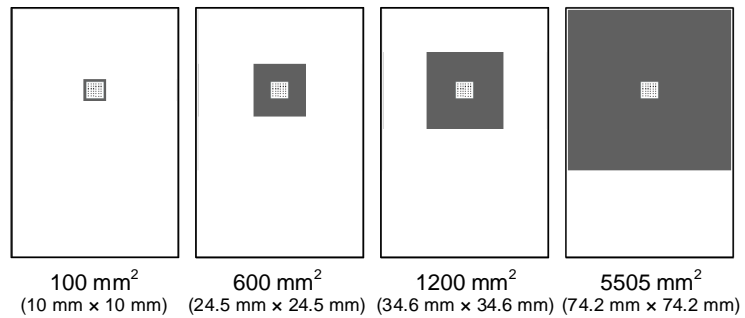
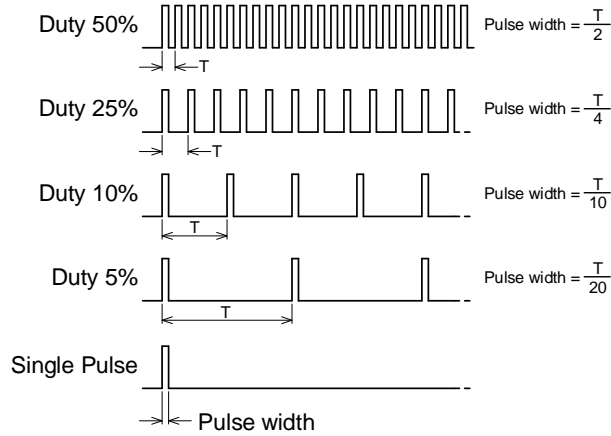


Figure 3-4-3-6. Middle layer 2

4. Transient thermal resistance

Graph axes descriptions

X-axis: The pulse width refers to the time during which the power is applied to a device



Y-axis: Transient thermal resistance

4-1. Transient thermal resistance, 1 layer



Figure 4-1-1. 1-layer board sectional view

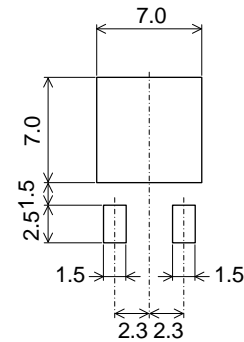


Figure 4-1-2. Footprint dimensions

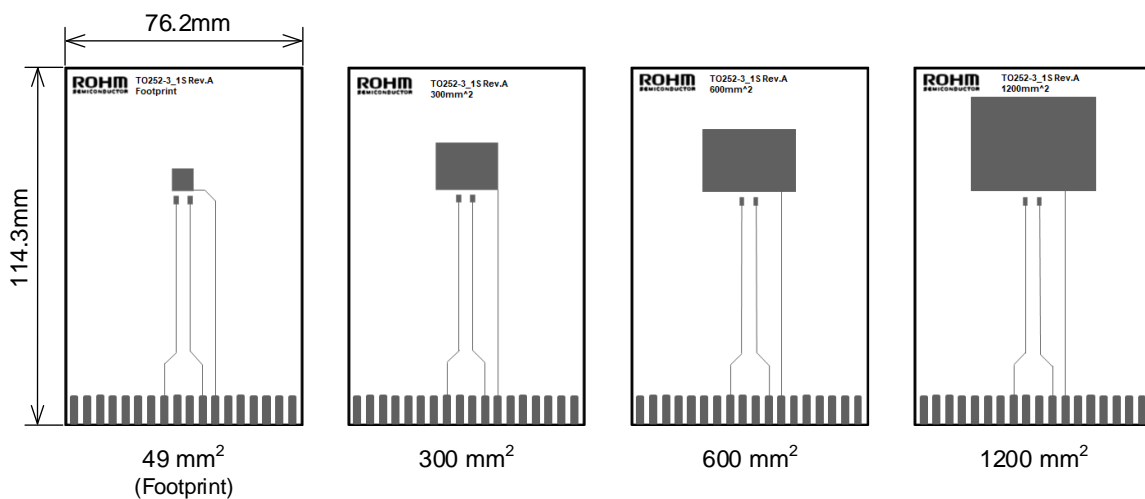


Figure 4-1-3. Top layer

4-1. Transient thermal resistance, 1 layer (continued)

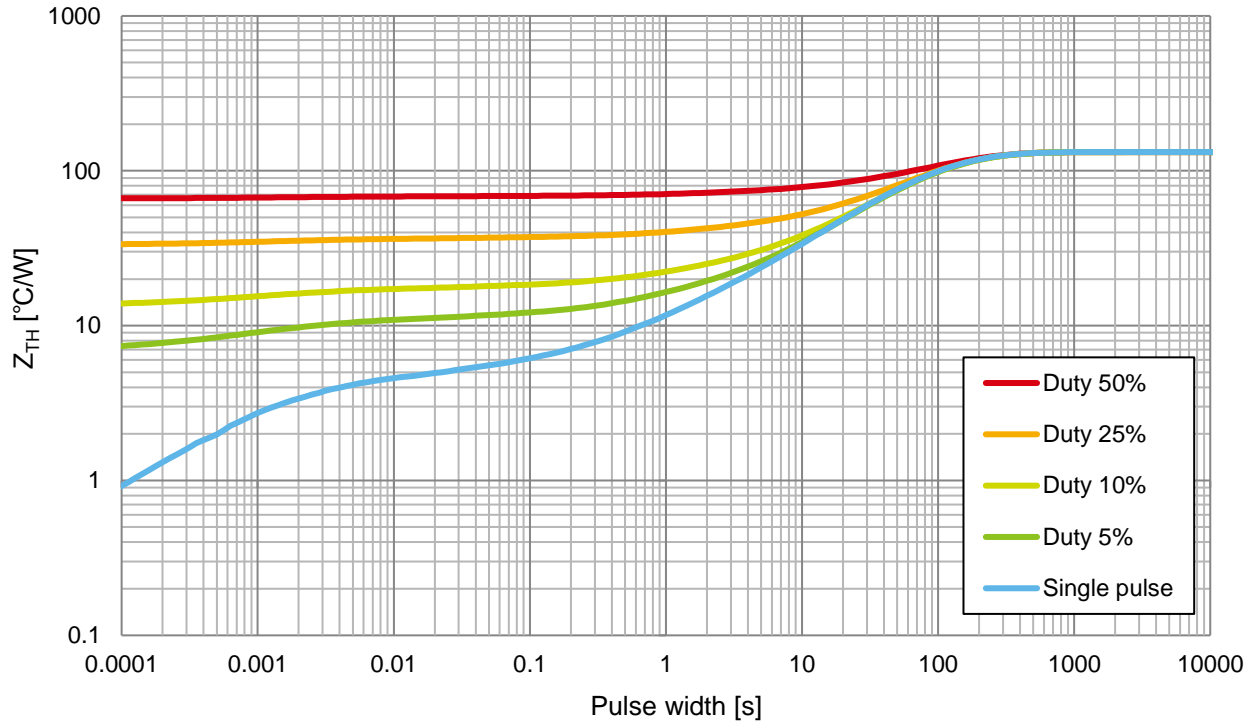


Figure 4-1-4. Transient thermal resistance, 1 layer
Copper foil area 49 mm² (Footprint)

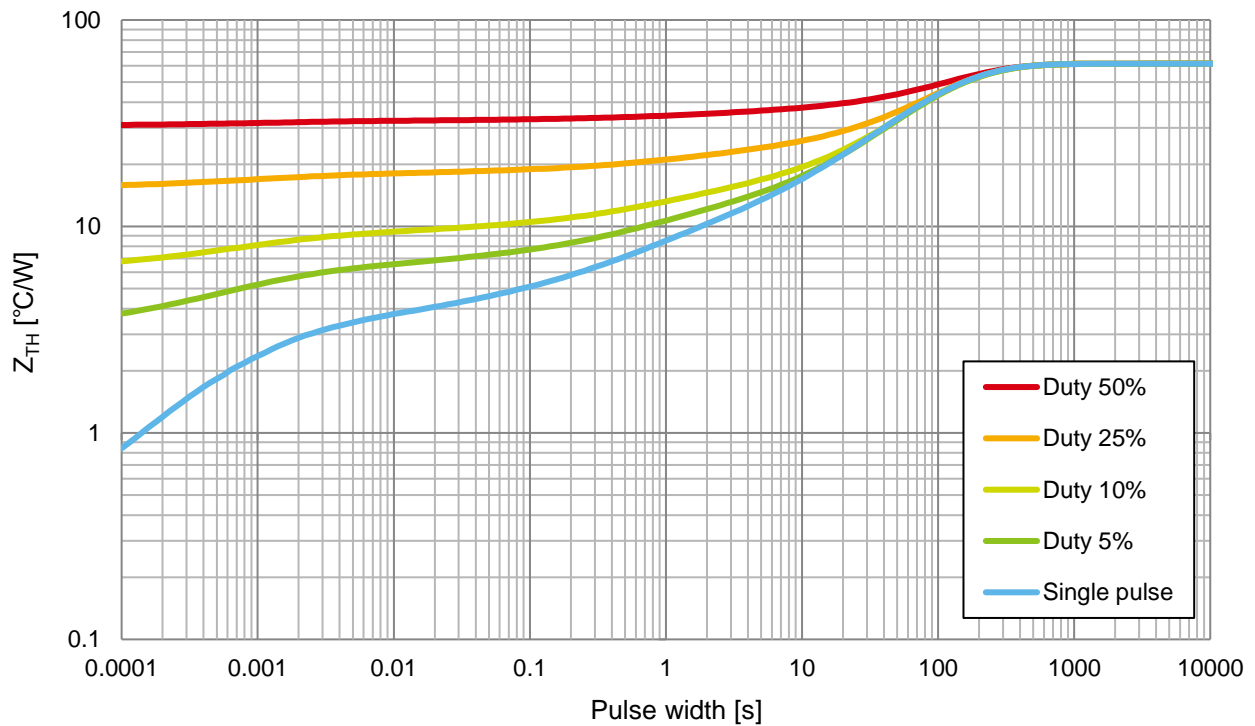


Figure 4-1-5. Transient thermal resistance, 1 layer
Copper foil area 300 mm²

4-1. Transient thermal resistance, 1 layer (continued)

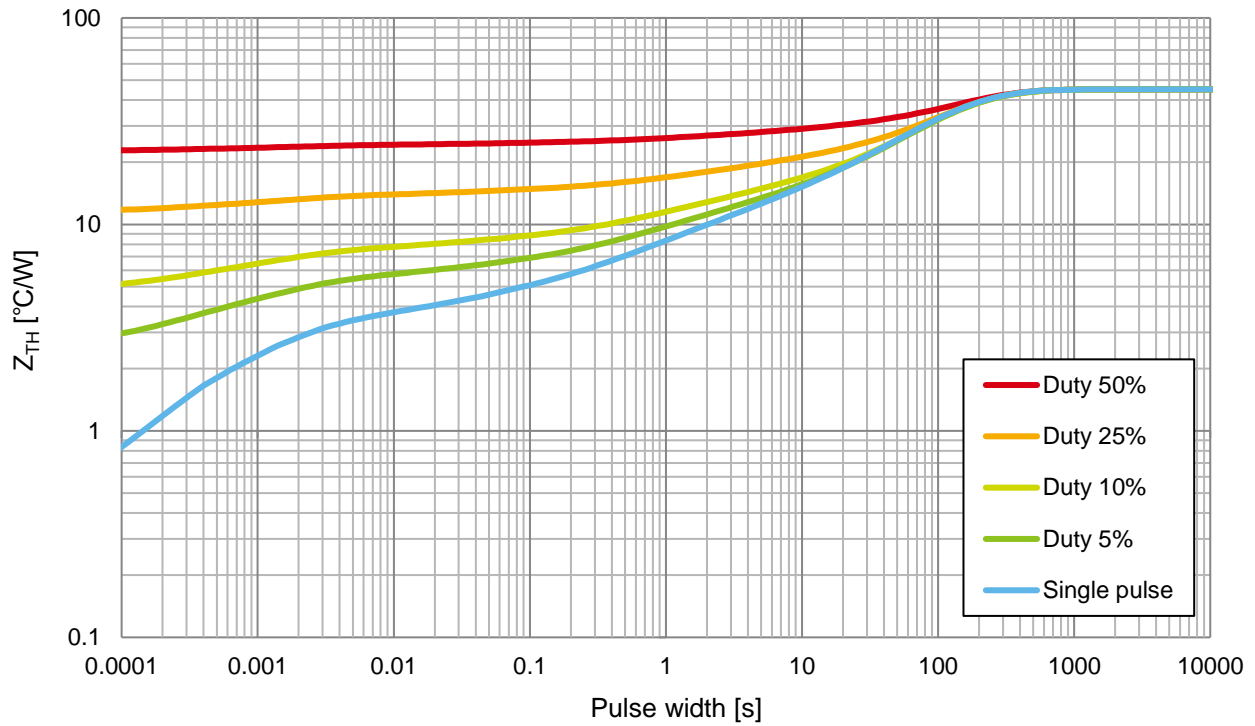


Figure 18. Transient thermal resistance, 1 layer
Copper foil area 600 mm²

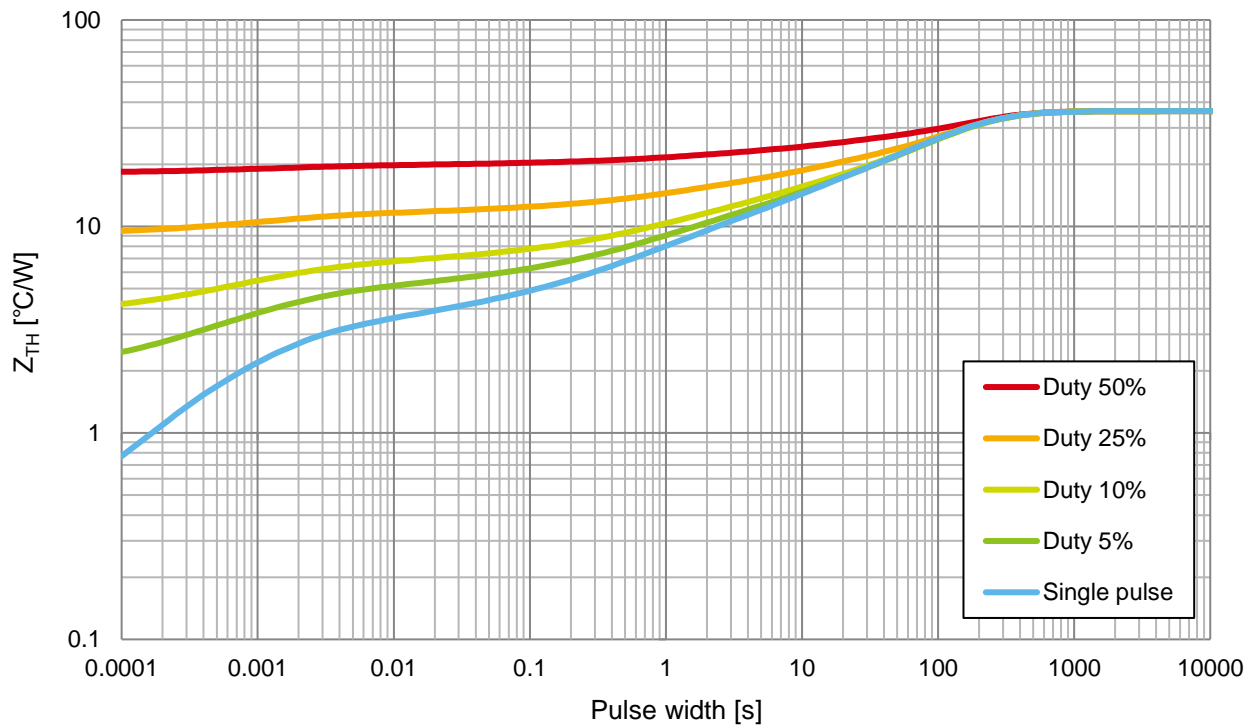


Figure 19. Transient thermal resistance, 1 layer
Copper foil area 1,200 mm²

4-2. Transient thermal resistance, 2 layers

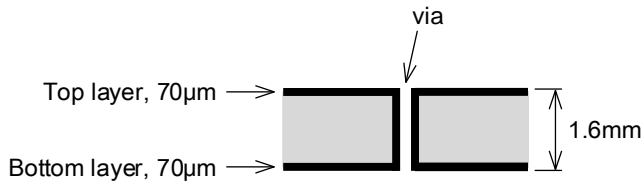


Figure 4-2-1. 2-layer board sectional view

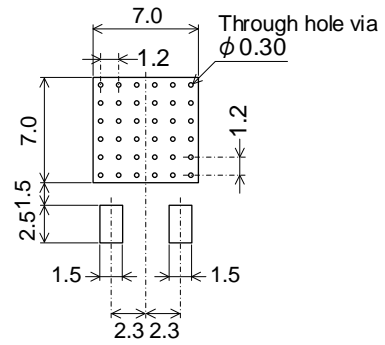
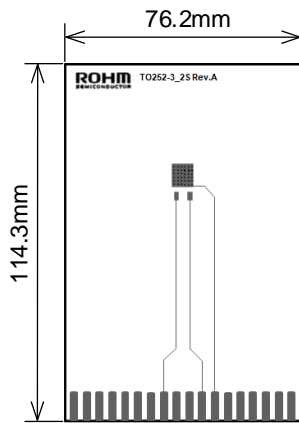
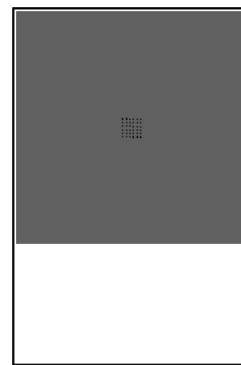


Figure 4-2-2. Footprint dimensions



49 mm²
(Footprint)

Figure 4-2-3. Top layer



5505 mm²
(74.2 mm x 74.2 mm)

Figure 4-2-4. Bottom layer

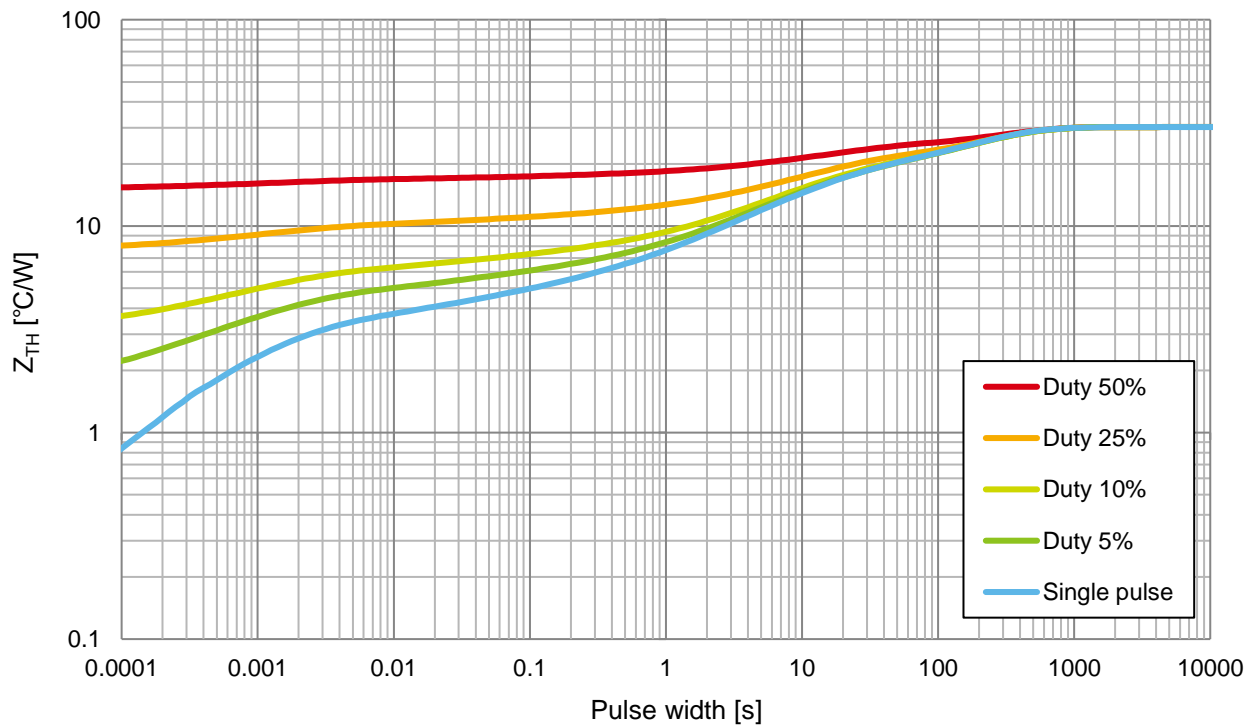


Figure 4-2-5. Transient thermal resistance, 2 layers

4-3. Transient thermal resistance, 4 layers

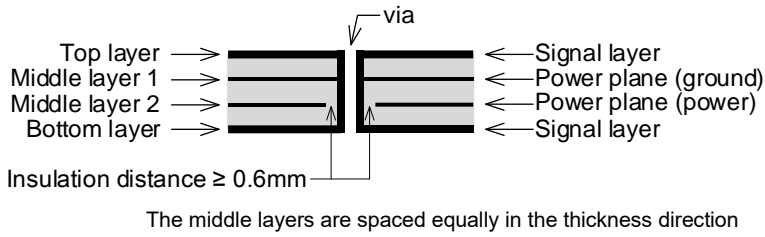


Figure 4-3-1. 4-layer board sectional view

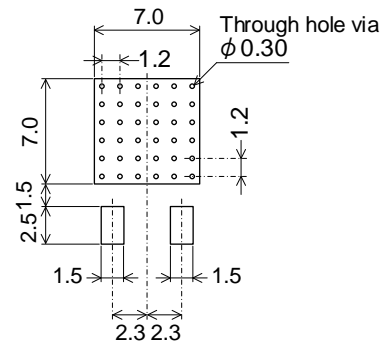
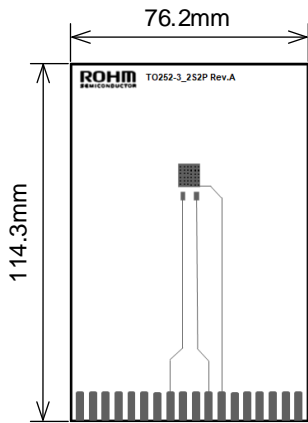


Figure 4-3-2. Footprint dimensions



49 mm²
(Footprint)
Figure 4-3-3.
Top layer

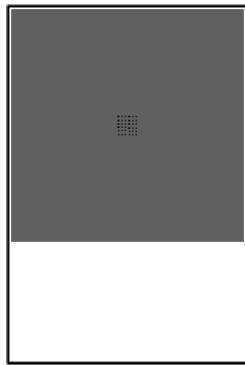


Figure 4-3-4.
Middle 1 layer

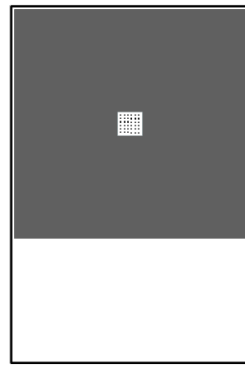


Figure 4-3-5.
Middle 2 layer

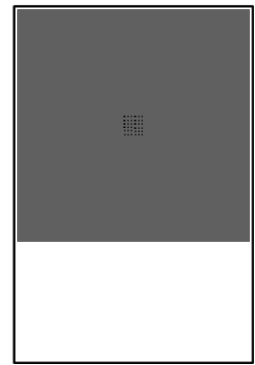


Figure 4-3-6.
Bottom layer

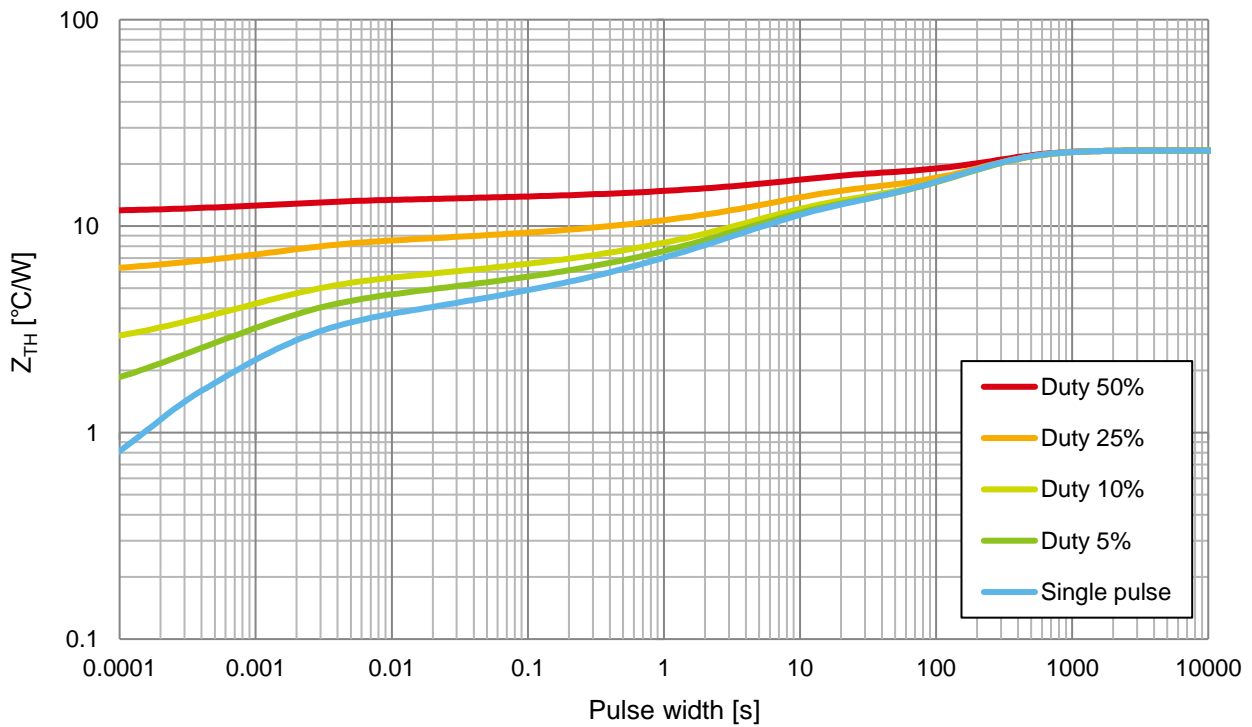


Figure 4-3-7. Transient thermal resistance, 4 layers

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