Linear Regulator Series

Thermal Resistance Data: VSON008X2030

BDxxGA3WNUX Series

This application note provides the thermal resistance data of the VSON008X2030 package used for the thermal design of the BDxxGA3WNUX series linear regulator IC.

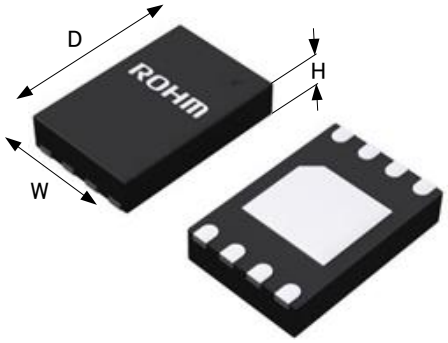
IC summary

The BDxxGA3WNUX series are LDO regulators with an output current of 0.3A. The output accuracy is ±1% of the output voltage. The VSON008X2030 package can contribute to downsizing of the set.

- Operating temperature range: -25°C to +85°C
- Input voltage range: 4.5 V to 14.0 V
- Quiescent current: 0 μA (Typ.)
- Output current: 0.3 A (Max.)
- Output voltage: 1.5 V to 13.0 V
- Output voltage precision: ±1%

See Datasheet for more details.

Package



VSON008X2030

W (typ) D (typ) H (max)

2.0 mm × 3.0 mm × 0.6 mm

Measurement environment

Content	Standard
Measurement environment	JEDEC STANDARD JESD51-2A (Still Air)
Measurement board standard	JEDEC STANDARD JESD51-3 JESD51-5 JESD51-7

Thermal resistance

Configuration	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)
1 layer	182	27
2 layers	78	12
4 layers	41	7

θ_{JA}: Thermal resistance between
junction temperature T_J -
ambient temperature T_A

Ψ_{JT}: Thermal characterization parameter between
Junction temperature T_J -
package surface center temperature T_T

Note: The thermal resistances and thermal characterization parameters in this application note are based on measurement under a JEDEC environment and may not always be consistent with the values for actual equipment. It is necessary to consider variations in the values due to the PCB characteristics, PCB layout, parts layout, chassis shape, surrounding environment, and so on.

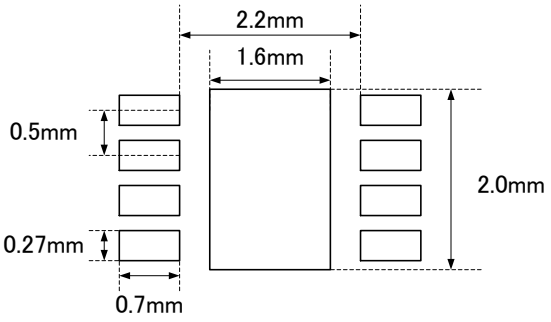
No. 62AN012E Rev.001
Aug. 2019

PCB specification, 1 layer (1s)

Conforms to JEDEC standard JESD51-3

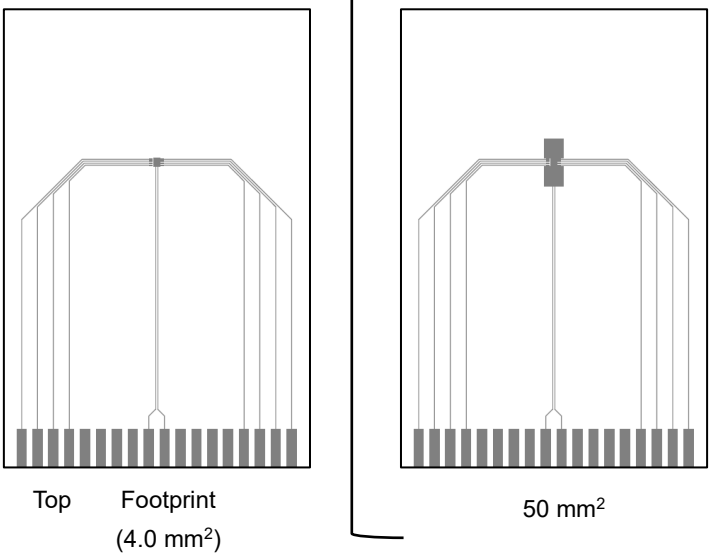
Item	Value
Board thickness	1.57 mm
Board outline dimensions	76.2 mm × 114.3 mm
Board material	FR-4
Trace thickness (finish thickness)	70 μm (2 oz)
Lead width	0.254 mm
Copper foil area	Footprint (4.0 mm^2) [50 mm^2, 100 mm^2, 300 mm^2, 600 mm^2]

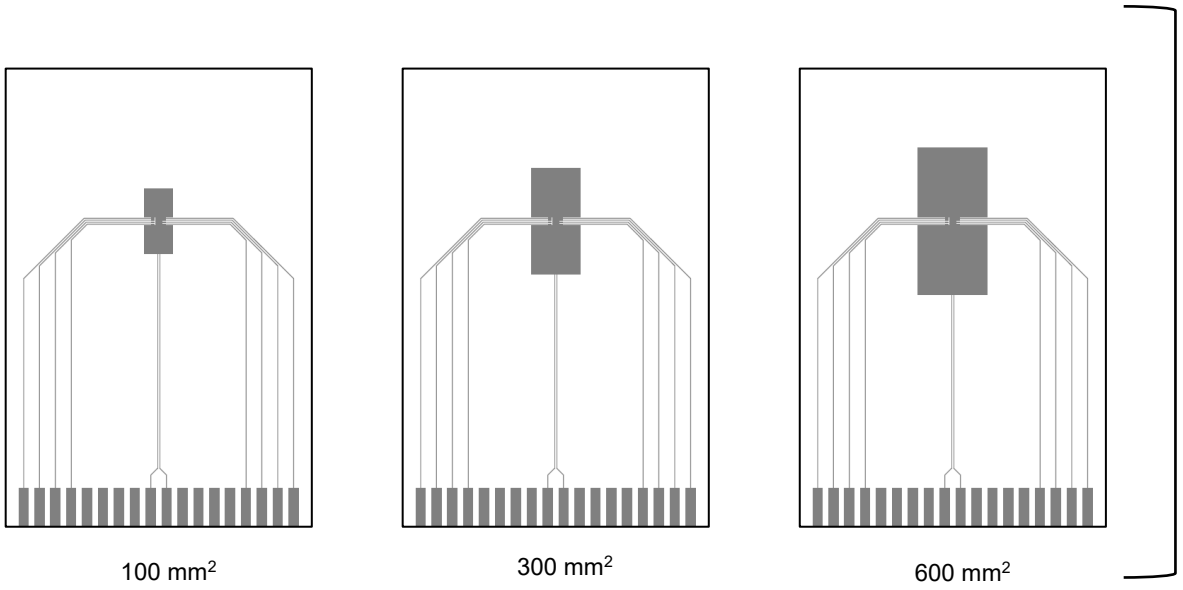
1 layer board cross sectional view



Footprint dimensions

- Trace layouts

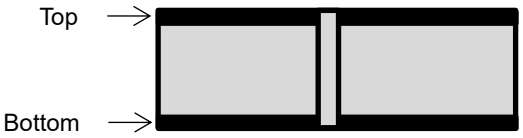




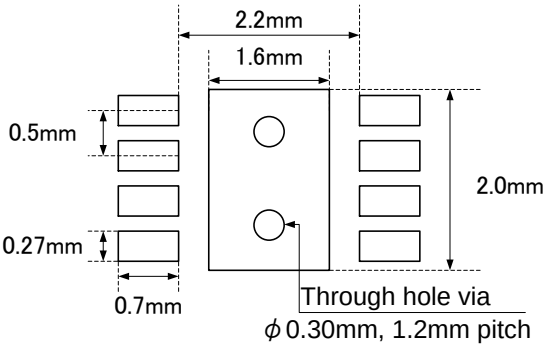
PCB specification, 2 layers (2s)

Conforms to JEDEC standard JESD51-5, JESD51-7

Item		Value
Board thickness		1.60 mm
Board outline dimensions		76.2 mm × 114.3 mm
Board material		FR-4
Trace thickness (finish thickness)	Top Bottom	70 µm (2 oz) 70 µm (2 oz)
Lead width		0.254 mm
Copper foil area	Top Bottom	Footprint (4.0 mm^2) 5505 mm^2 [50 mm^2, 100 mm^2, 300 mm^2, 600 mm^2, 1200 mm^2, 3000 mm^2]

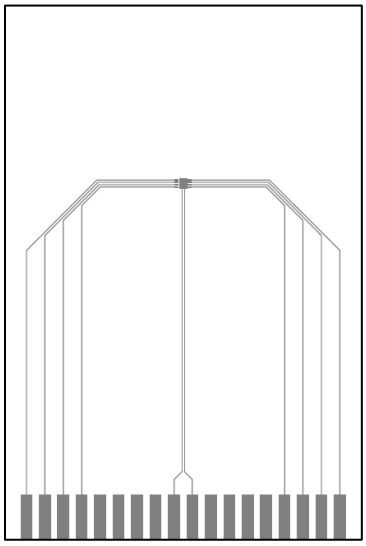


2 layer board cross sectional view

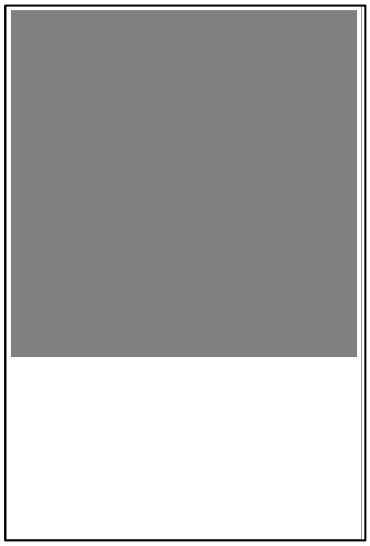


Footprint dimensions

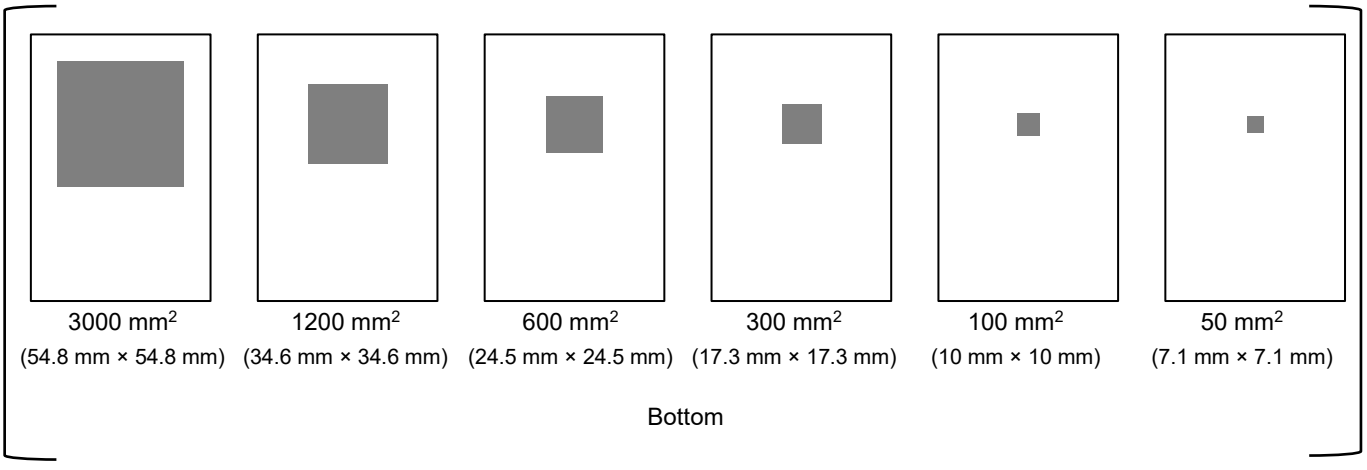
- Trace layouts



Top Footprint
(4.0 mm^2)



Bottom
5505 mm^2
(74.2 mm × 74.2 mm)



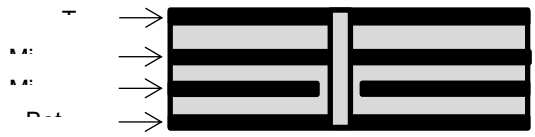
3000 mm^2 (54.8 mm × 54.8 mm) | 1200 mm^2 (34.6 mm × 34.6 mm) | 600 mm^2 (24.5 mm × 24.5 mm) | 300 mm^2 (17.3 mm × 17.3 mm) | 100 mm^2 (10 mm × 10 mm) | 50 mm^2 (7.1 mm × 7.1 mm)

Bottom

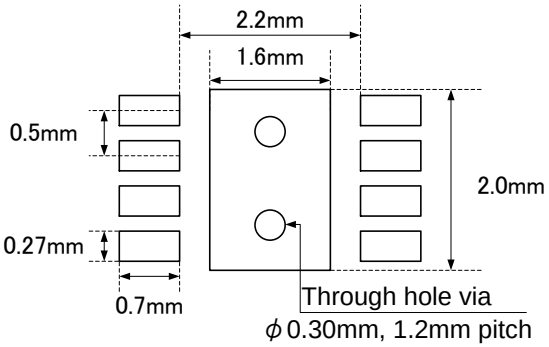
PCB specification, 4 layers (2s2p)

Conforms to JEDEC standard JESD51-5, JESD51-7

Item		Value
Board thickness		1.60 mm
Board outline dimensions		76.2 mm × 114.3 mm
Board material		FR-4
Trace thickness (finish thickness)	Top Middle 1 Middle 2 Bottom	70 µm (2 oz) 35 µm (1 oz) 35 µm (1 oz) 70 µm (2 oz)
Lead width		0.254 mm
Copper foil area	Top Middle 1 Middle 2 Bottom	Footprint (4.0 mm^2) 5505 mm^2 (74.2 mm × 74.2 mm) 5498 mm^2 (74.2 mm × 74.2 mm) 5505 mm^2 (74.2 mm × 74.2 mm)

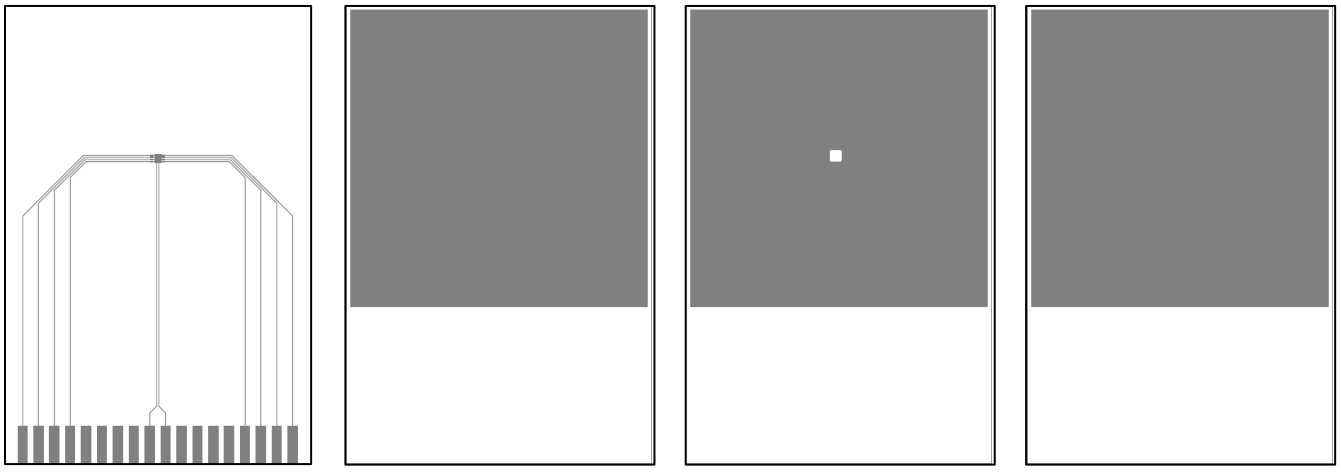


4 layer board cross sectional view



Footprint dimensions

- Trace Layouts



Top Middle 1 Middle 2 Bottom

Thermal resistance data, 1 layer (1s)

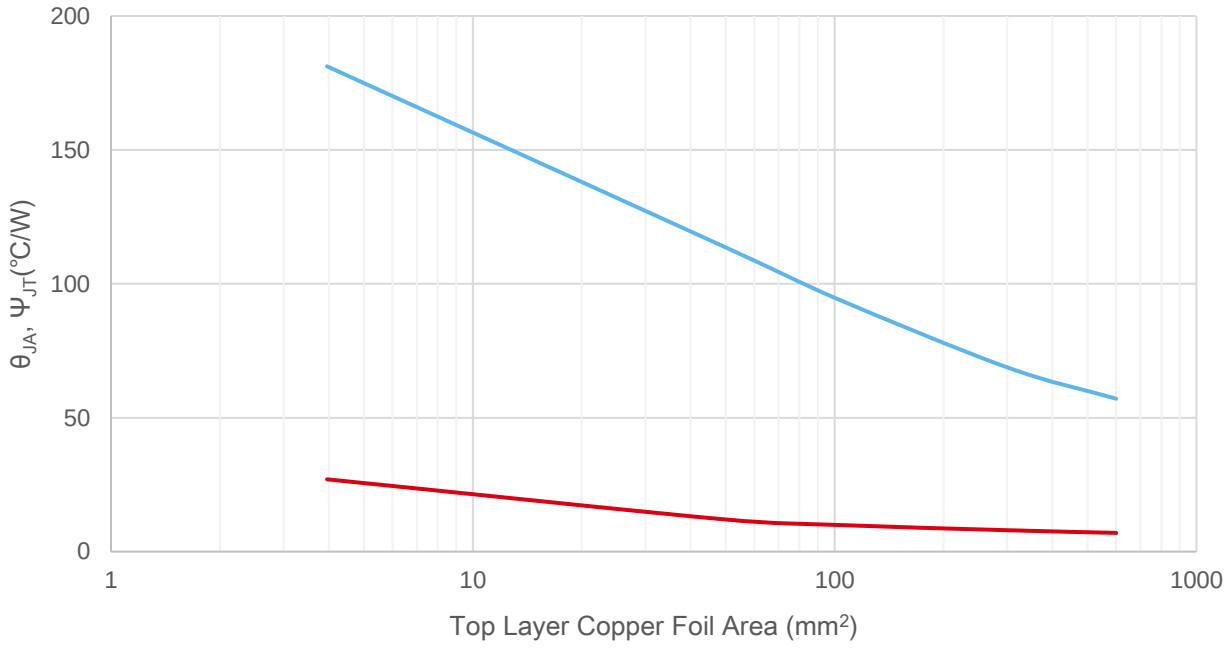


Figure 1. θ_{JA}, Ψ_{JT} vs. Top Layer Copper Foil Area

Thermal resistance data, 2 layers (2s)

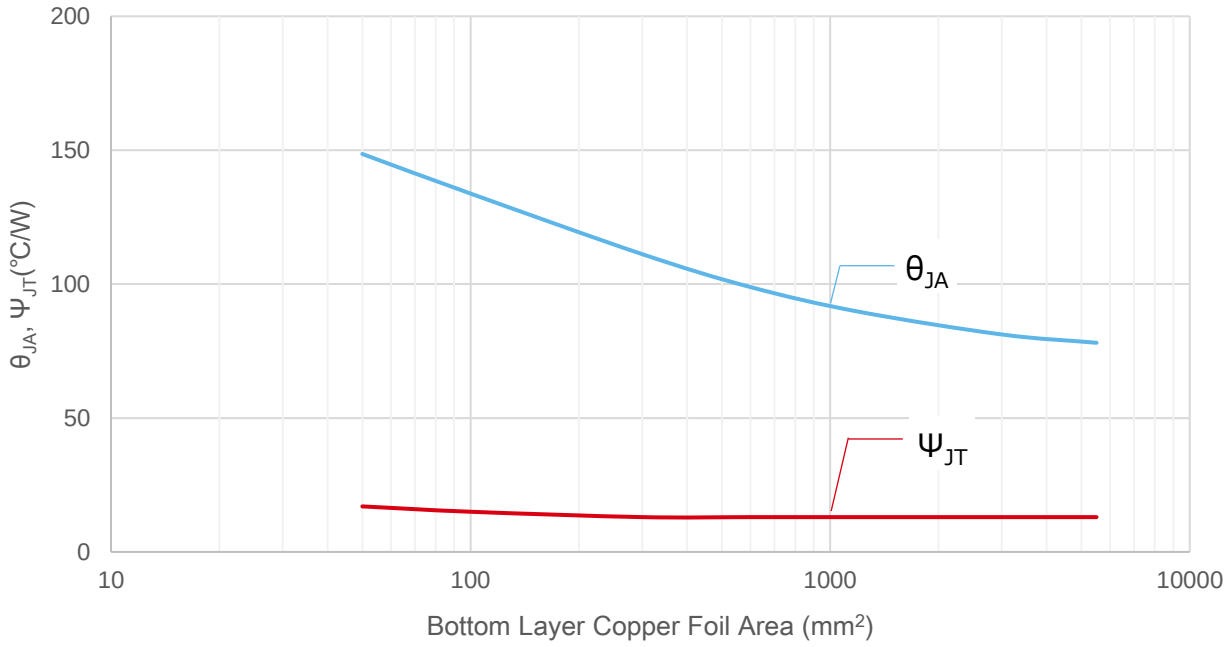
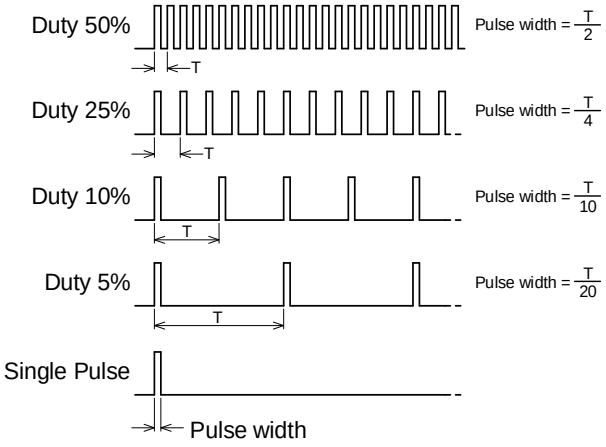


Figure 2. θ_{JA}, Ψ_{JT} vs. Bottom Layer Copper Foil Area

Transient thermal resistance

Conforms to JEDEC standard JESD51

X axis: The length of time electrical power is applied to the device-under-test



Y axis: Transient thermal resistance

Transient thermal resistance data, 1 layer (1s)

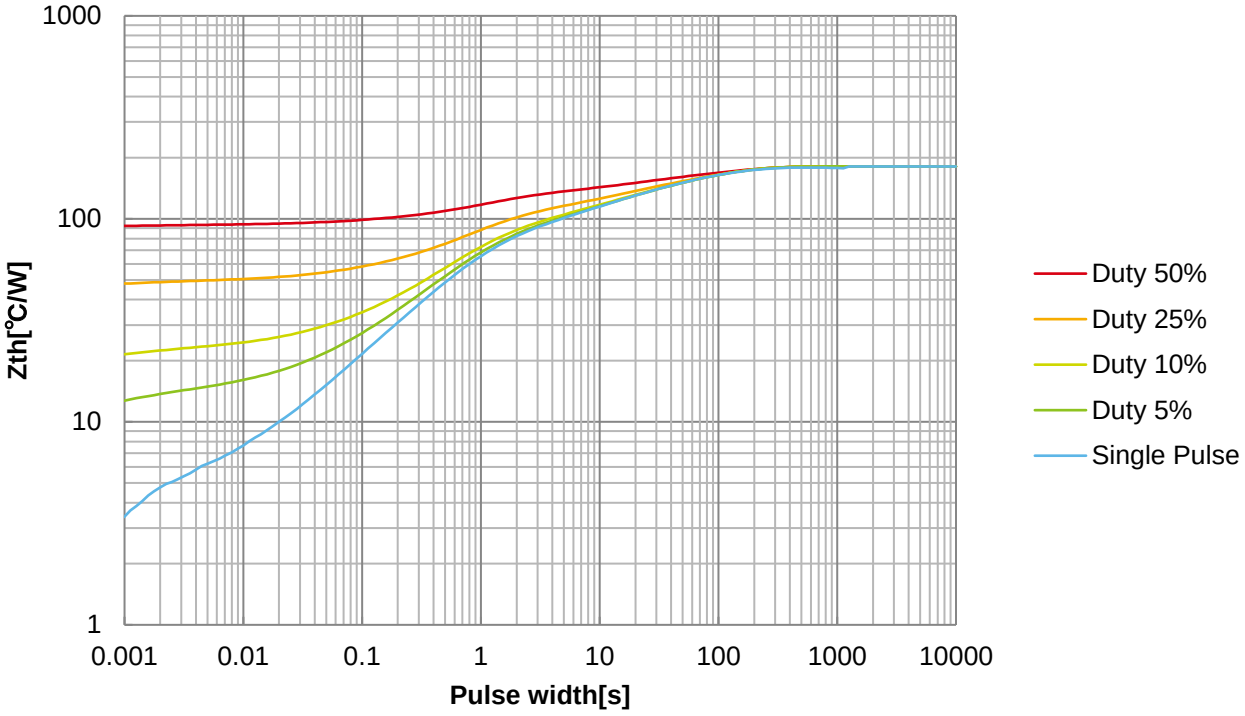


Figure 3. Transient thermal resistance, 1 layer, Copper foil surface area 4.0 mm^2 (Footprint)

Transient thermal resistance data, 1 layer (1s), continued

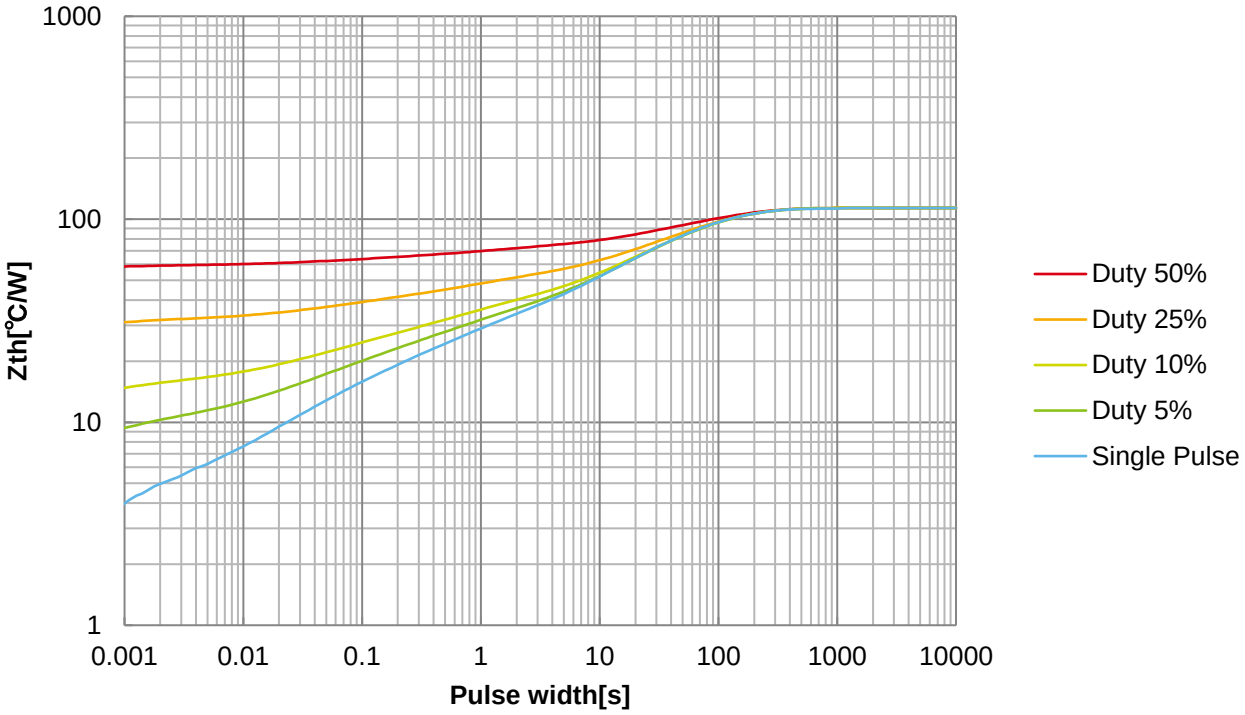


Figure 4. Transient thermal resistance, 1 layer, Copper foil surface area 50 mm^2

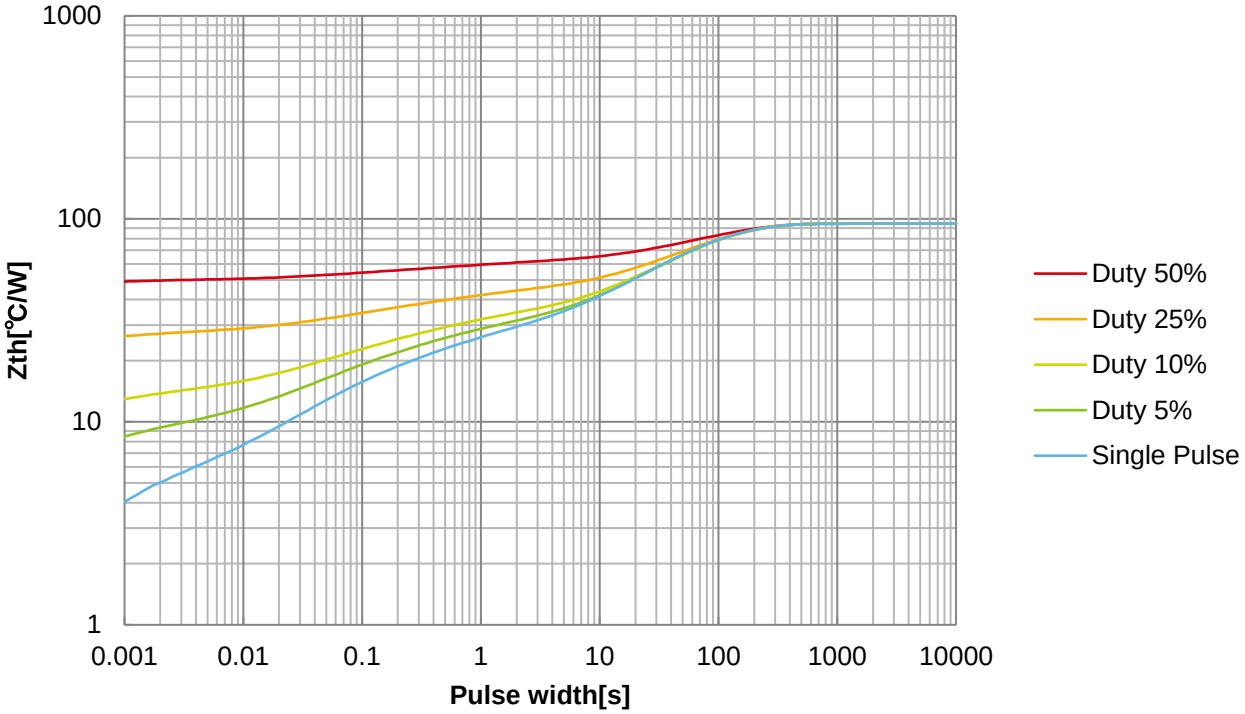


Figure 5. Transient thermal resistance, 1 layer, Copper foil surface area 100 mm^2

Transient thermal resistance data, 1 layer (1s), continued

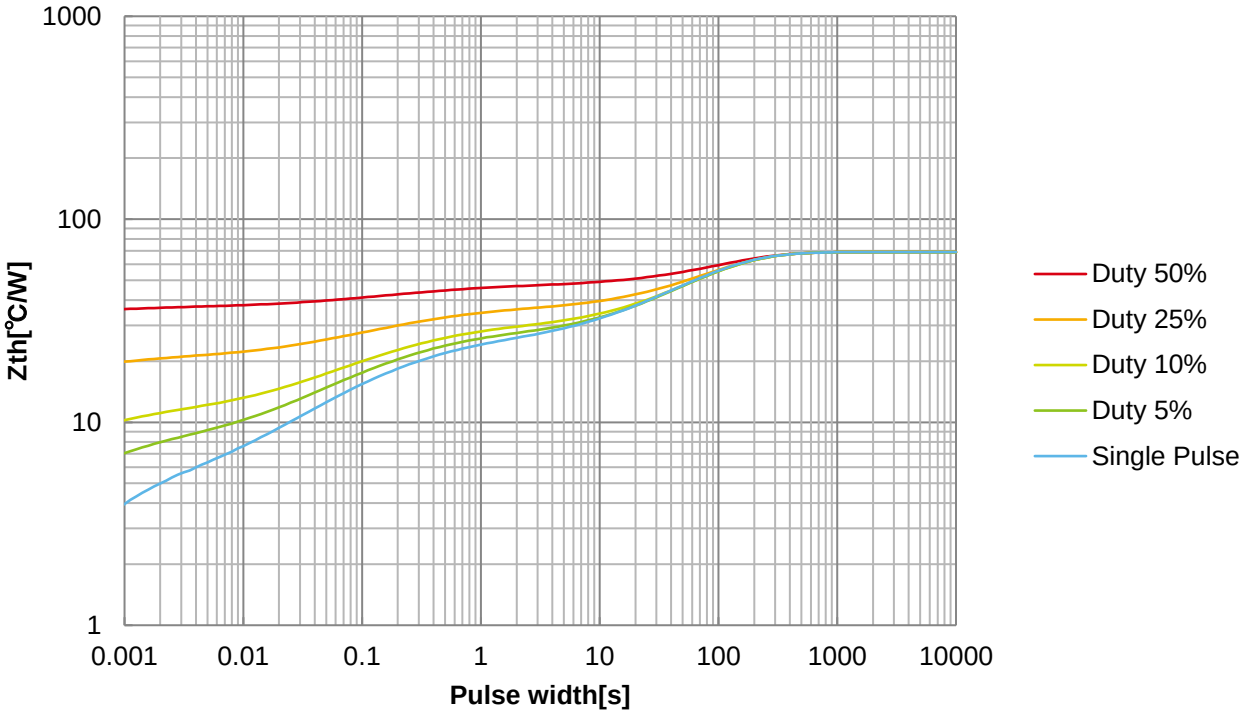


Figure 6. Transient thermal resistance, 1 layer, Copper foil surface area 300 mm^2

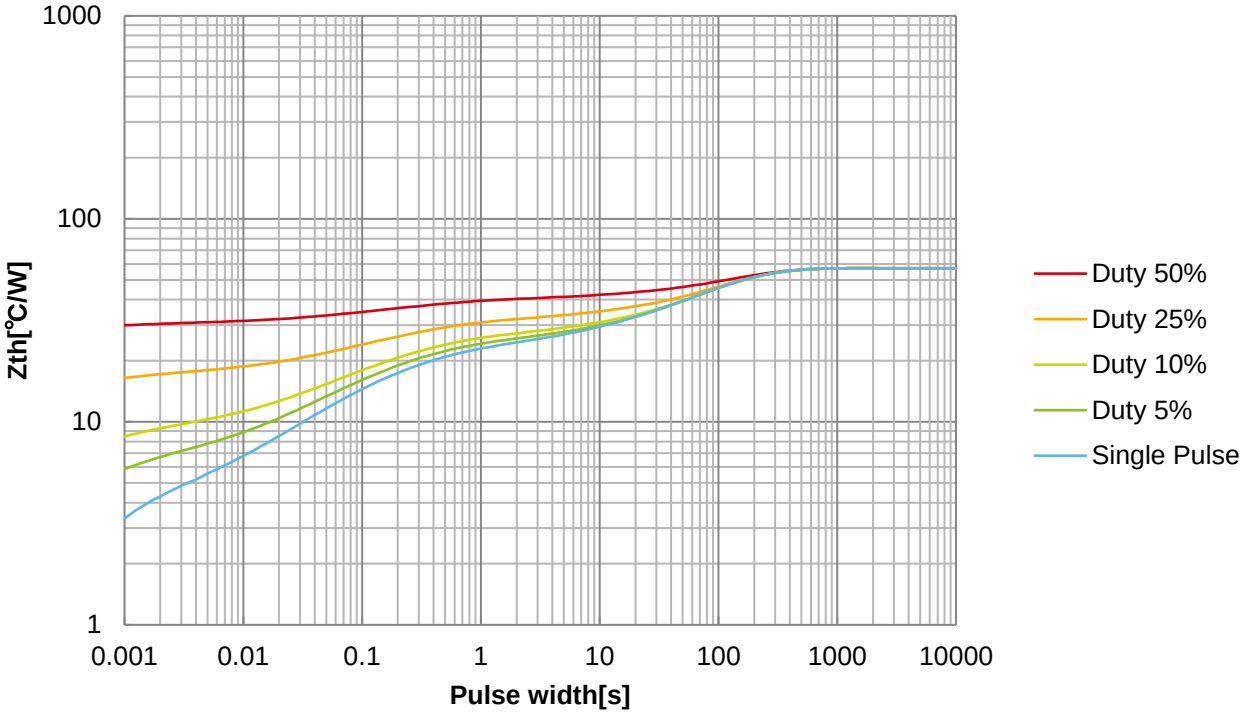


Figure 7. Transient thermal resistance, 1 layer, Copper foil surface area 600 mm^2

Transient thermal resistance data, 2 layers (2s)

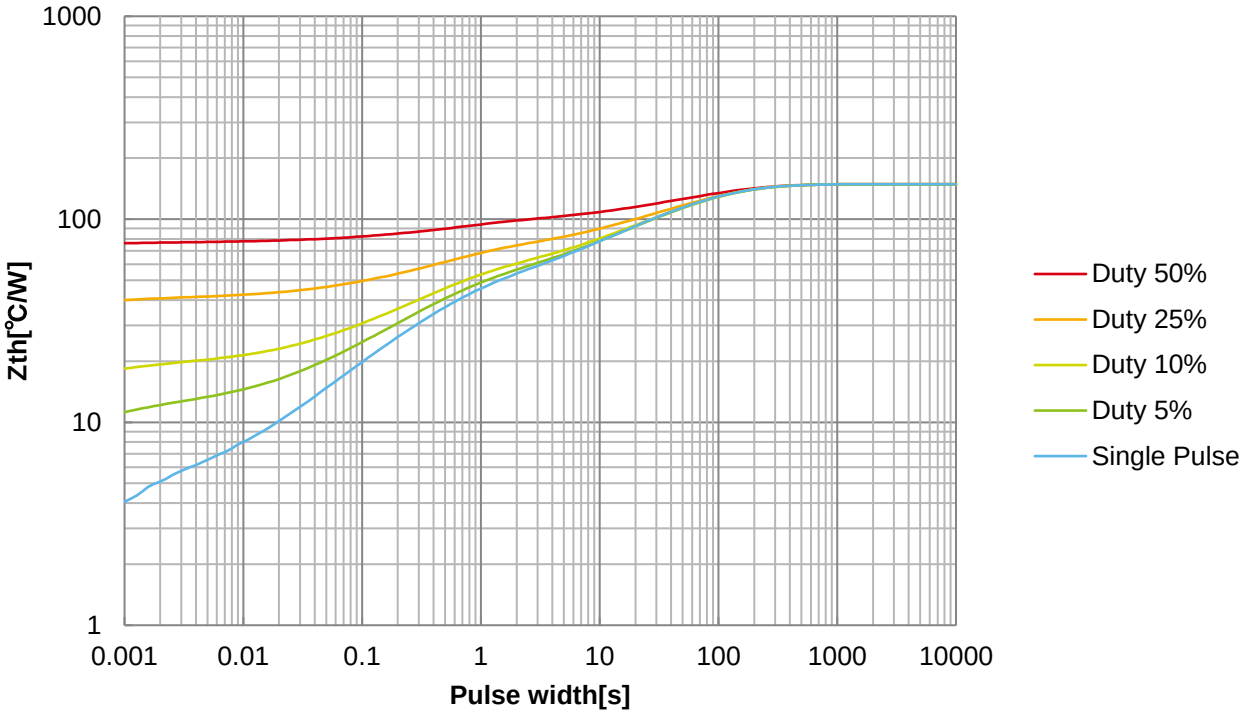


Figure 8. Transient thermal resistance, 2 layers, Copper foil bottom area 50 mm^2

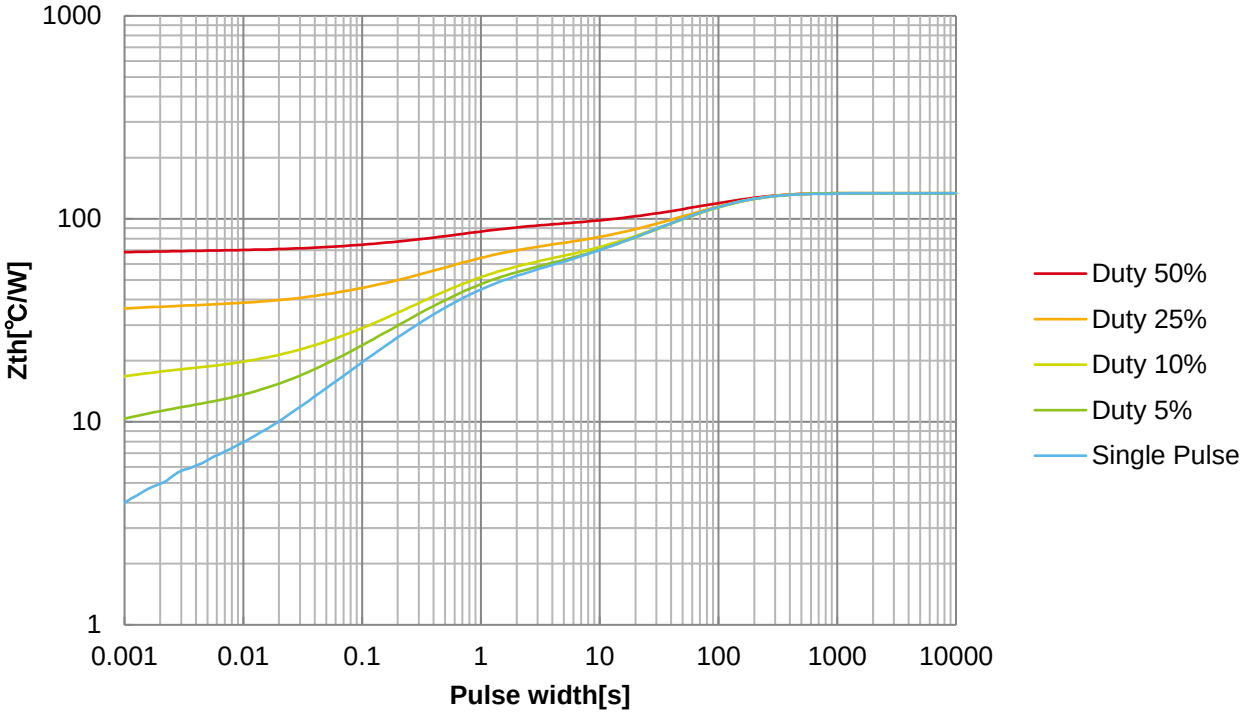


Figure 9. Transient thermal resistance, 2 layers, Copper foil bottom area 100 mm^2

Transient thermal resistance data, 2 layers (2s), continued

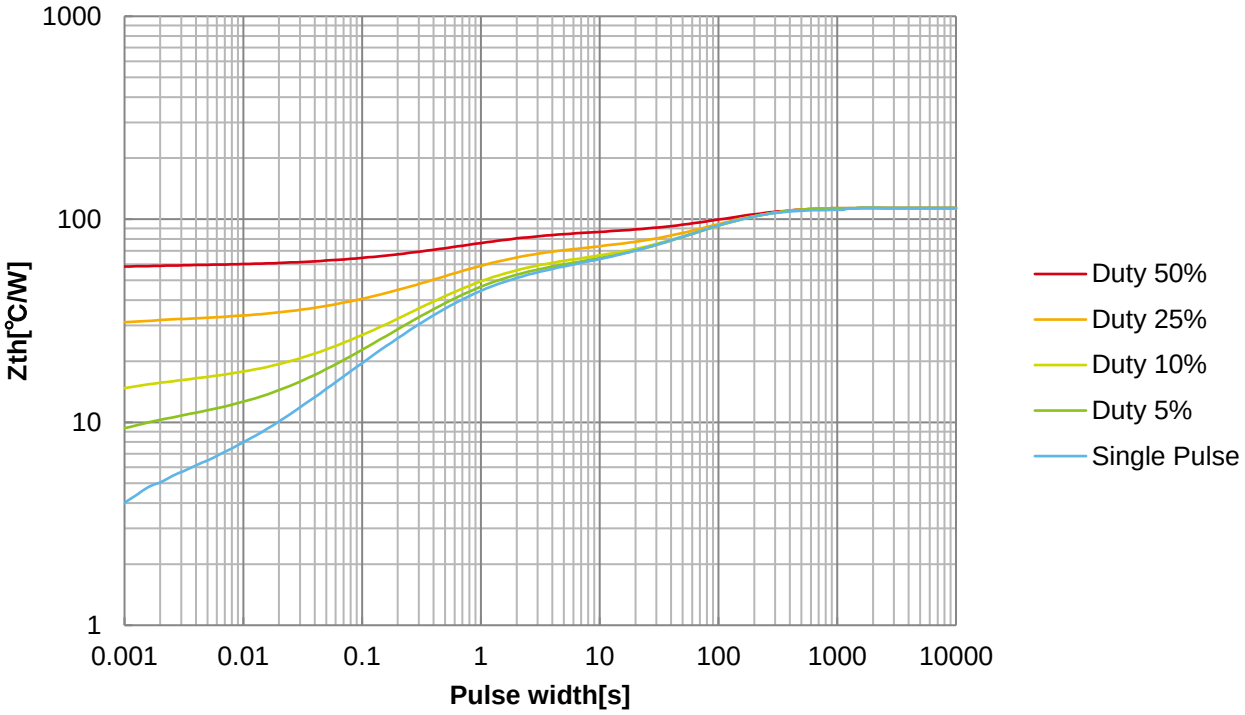


Figure 10. Transient thermal resistance, 2 layers, Copper foil bottom area 300 mm^2

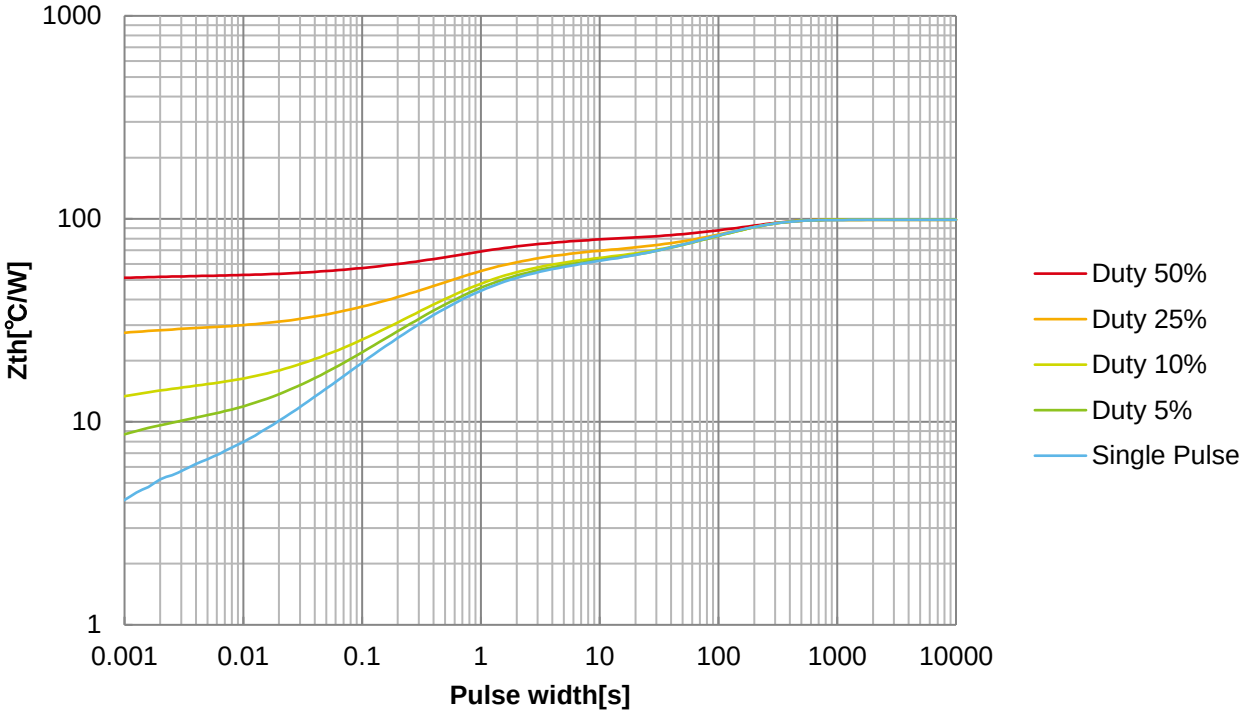


Figure 11. Transient thermal resistance, 2 layers, Copper foil bottom area 600 mm^2

Transient thermal resistance data, 2 layers (2s), continued

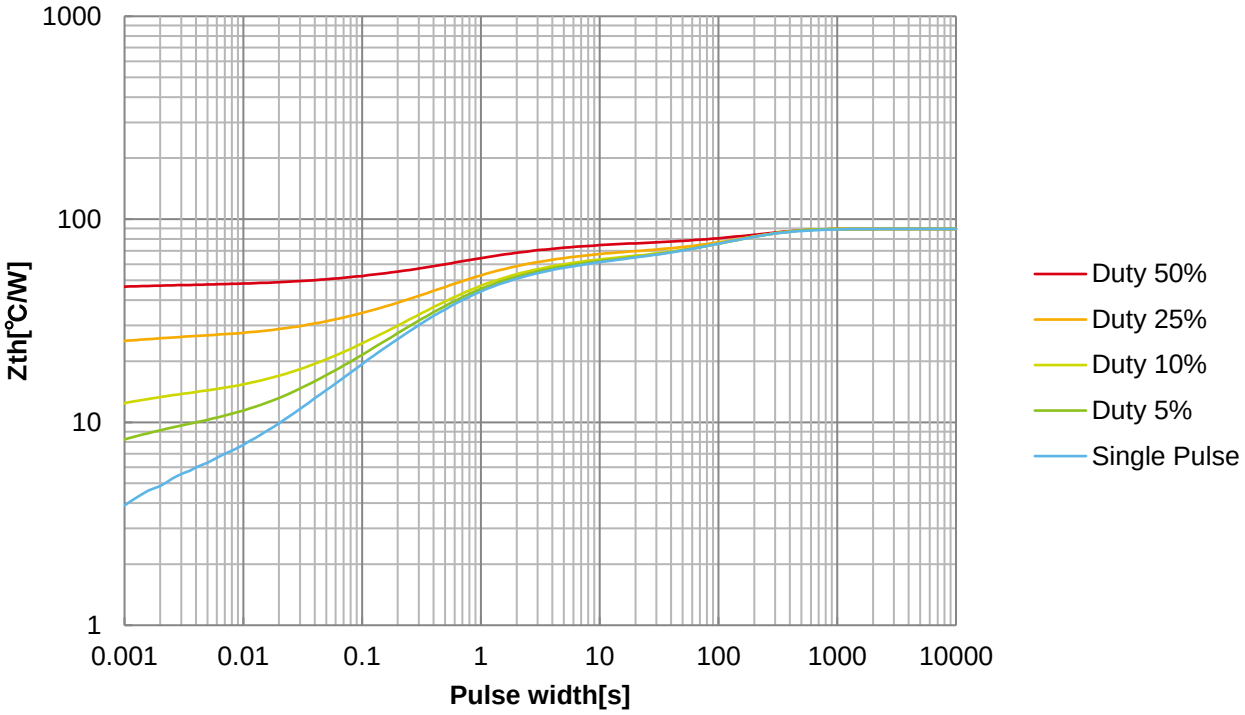


Figure 12. Transient thermal resistance, 2 layers, Copper foil bottom area 1200 mm^2

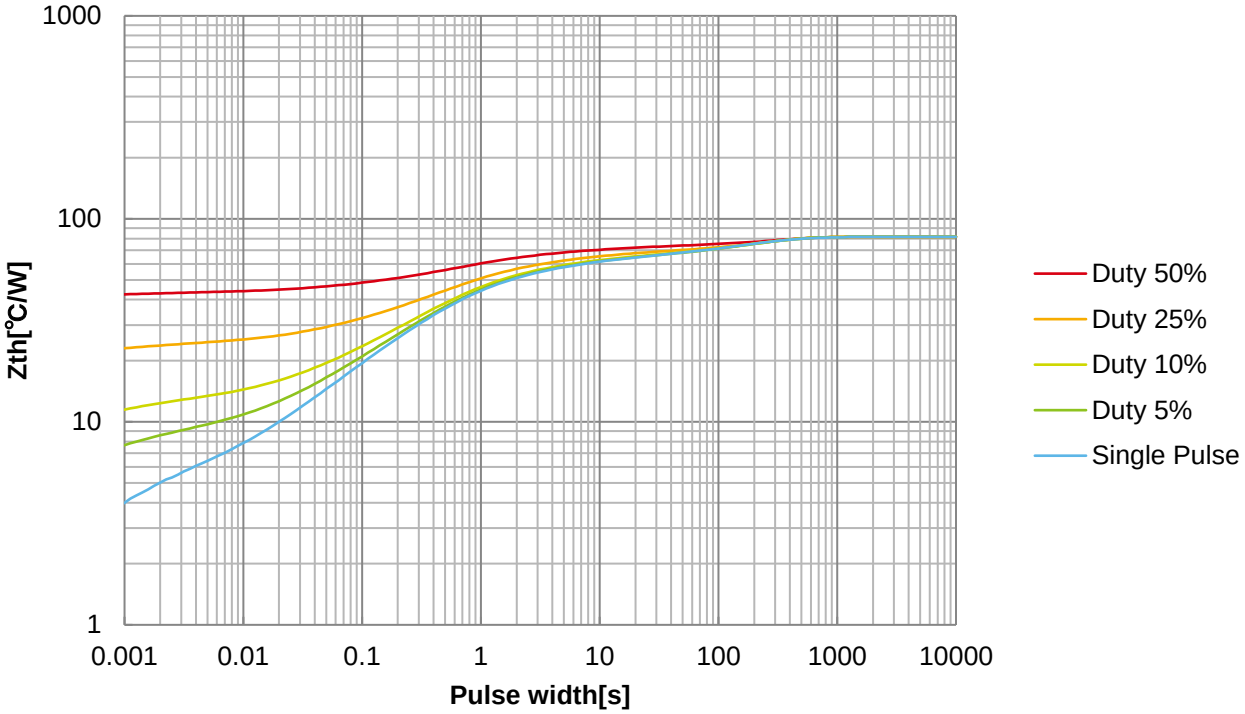


Figure 13. Transient thermal resistance, 2 layers, Copper foil bottom area 3000 mm^2

Transient thermal resistance data, 2 layers (2s) , continued

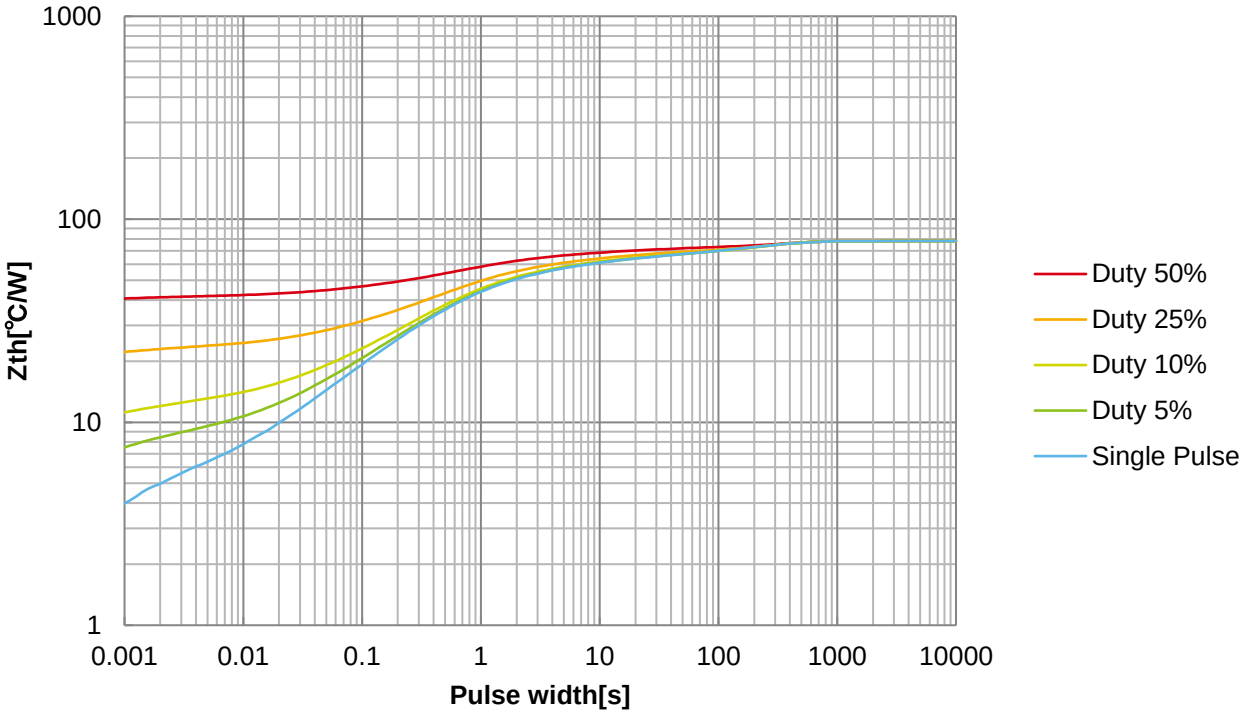


Figure 14. Transient thermal resistance, 2 layers, Copper foil bottom area 5505 mm^2

Transient thermal resistance data, 4 layers (2s2p)

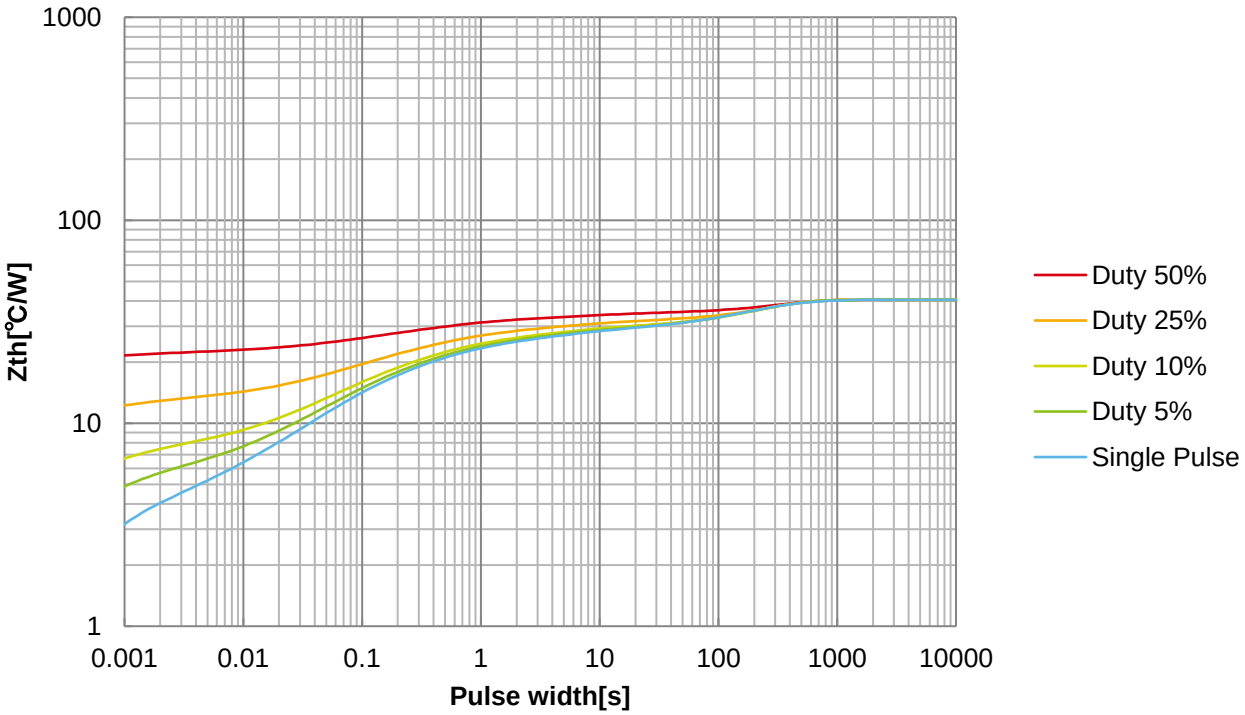


Figure 15. Transient thermal resistance, 4 layers

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