BD7F100HFN Isolated DCDC

External Components Dimensioning

This application note is a guideline to design an isolated DCDC converter based on the BD7F100HFN IC and to dimension the external components. The BD7F100HFN can implement a Flyback converter with a simple transformer (no auxiliary coil needed) and without an optocoupler using primary side control as shown below. It offers an effective, compact and cheap solution for any application requiring an isolated DCDC converter between two power domains.

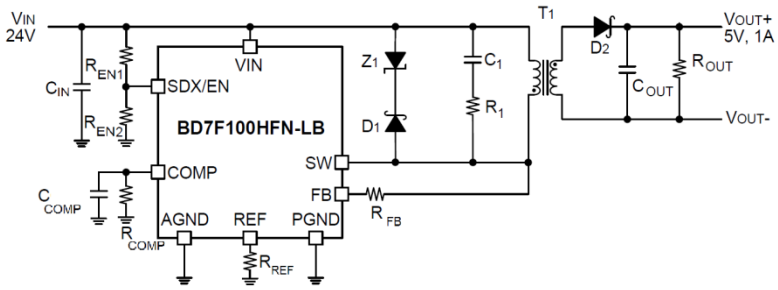
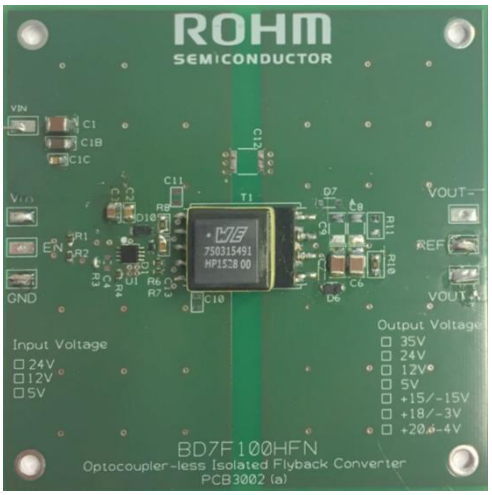


Figure 1: Typical DCDC Isolated application schematic and circuit board with optocoupler less BD7F100HFN DCDC converter



1. Application

This document contains a tutorial for the design and dimensioning of an isolated DCDC converter based on the following specifications: These specifics correspond to the evaluation board: BD7F100HFN_EVK_00X that is available from Rohm and its distributors

Input voltage:	24Vdc
Output voltage:	5Vdc
Output current:	1A
Output power:	5W
Efficiency target:	0.8
Output Accuracy target:	10%
Output diode drop:	0.7V

2. Input Block

2.1 Input Capacitor

It is recommended to use a ceramic capacitor as the_input capacitor (C_{IN}). The capacitor value should be chosen based on the maximum power output and on the input voltage. Ripple on V_{IN} pin should be below 4% of input voltage. An additional capacitor of 100nF can be used to filter high frequency noises although usually this is not necessary.

LAYOUT GUIDELINES: *position the capacitor as close as possible to V_{IN} and GND pins of the IC.*

Note 1. For this application at 5W an input capacitor of 10uF has been chosen.

2.2 Enabling Signal

IC starts up when the following conditions are all satisfied:

1. V_{IN} needs to be above UVLO value at 2,5V(Typ.)
2. V_{IN} has to be higher than the reflected output voltage (where N_p is the number of turns in the primary winding and N_s is the number of turns in the secondary winding):

$$V_{IN} > \frac{N_P}{N_S} \cdot (V_{OUT} + V_F) \qquad (1)$$

3. Enable pin voltage above 2V

Instead of an external enable signal an internal pull up signal can be used to allow the circuit to start when the input voltage reaches the right level. This is done by an additional resistor divider at the input (R_{EN1}, R_{EN2}). These resistors are dimensioned with the following equations: to set the V_{IN} start voltage (V_{IN_EN}), for a 2.0V (Typ.) threshold voltage at the EN pin :

$$V_{IN\_EN} = \frac{2.0V \cdot (R_{EN1} + R_{EN2})}{R_{EN2}} \qquad (2)$$

To set the shutdown input voltage (V_{IN_DIS}) at 1.8V with a Hysteresis voltage of 0.2V (Typ.):

$$V_{IN\_DIS} = \frac{1.8V \cdot (R_{EN1} + R_{EN2})}{R_{EN2}} \qquad (3)$$

$$R_{EN1} = R_{EN2}\left(\frac{V_{IN\_EN}}{2} - 1\right) \qquad (4)$$

Note 2. For V_{IN_EN}=22V and setting R_{EN2} at 100kOhm,
we calculate: R_{EN1} = *1MOhm*
V_{IN_DIS} *Calculated with (3) is: 19.8V*

Note that with a pull-down signal at 0V it is possible to force the IC disable also with the mounted resistor divider.

3. Transformer Dimensioning

3.1 Turns ratio calculation

Transformer dimensioning starts from the calculation of the turn ratio under the condition that the Duty Cycle (D) is <0.5 to ensure the stability of the system:

The Flyback converter duty cycle is given by the formula:

$$D = \frac{V_{Refl}}{V_{IN} + V_{Refl}} = \frac{\frac{N_P}{N_S} \cdot (V_{OUT} + V_F)}{V_{IN} + \frac{N_P}{N_S} \cdot (V_{OUT} + V_F)} \qquad (5)$$

In which V_{Refl} is the secondary voltage reflected to the primary.

From (5) we can calculate:

$$\frac{N_P}{N_S} = \frac{D \cdot V_{IN}}{(1-D) \cdot (V_{OUT} + V_F)} \qquad (6)$$

Correct functionality requires D<0.5 giving the following condition from (6):

$$\frac{N_P}{N_S} < \frac{V_{IN}}{V_{OUT} + V_F} \qquad (7)$$

The minimum Ton is 350ns, so for a max frequency of 400kHz (2.5us period) duty cycle Dmin >0.14. Considering margin and tolerances, let's select Dmin > 0.20, which gives for the formula (6):

$$\frac{N_P}{N_S} > \frac{1}{4} \cdot \frac{V_{IN}}{V_{OUT} + V_F} \qquad (8)$$

the conditions (7) and (8) imply:

$$\frac{1}{4} \cdot \frac{V_{IN}}{V_{OUT} + V_F} < \frac{N_P}{N_S} < \frac{V_{IN}}{V_{OUT} + V_F} \qquad (9)$$

Note 3. From the application data indicated in chapter 1 the constraint becomes:

$$1.05 < \frac{N_P}{N_S} < 4.2$$

is chosen:

$$\frac{N_P}{N_S} : \qquad 3 : 1$$

This value provides a D max (from (5)): 0.43

3.2 Primary Inductance calculation

To maintain the stability in the feedback loop, the maximum inductance value is given by the following formula:

$$L_P < \frac{2 \cdot D_{MAX} \cdot V_{IN}^2}{(V_{OUT} + V_F) \cdot I_{OMAX} \cdot \pi \cdot f_{SWmax}} \qquad (10)$$

where I_{OMAX} = Maximum load current (also $I_{OMAX} = \frac{P_{max}}{V_{out}}$)

and $f_{SWmax} = 400kHz$, η : power efficiency.

L_P has to be higher than the minimum value needed to transfer the requested max power P_{OUTMAX}:

$$P_{OUTMAX} = V_{OUT} \cdot I_{OUTMAX} < \eta \cdot V_{IN} \cdot I_{IN} \qquad (11)$$

that gives:

$$I_{IN} > \frac{V_{OUT} \cdot I_{OUTMAX}}{\eta \cdot V_{IN}} \qquad (12)$$

With $I_{IN}\ (average)$:

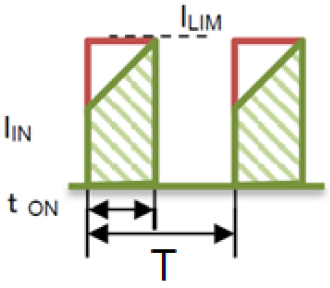


Figure 2: Current in primary winding

From figure 2 I_{IN} can be calculated as:

$$I_{IN} = \frac{\frac{I_{Lim}+I_{min}}{2} \cdot t_{on}}{T} \qquad (13)$$

Substituting $I_{min} = I_{Lim} - \frac{V_{in}DT}{L_P}$:

$$I_{IN} = I_{LIM} \cdot D - \frac{1}{2} \cdot \frac{V_{IN}}{L_P} \cdot T \cdot D^2$$

inserted in the equation (13) and solved for L_P :

$$L_P > \frac{1}{2} \cdot \frac{V_{IN}^2 \cdot T \cdot D^2 \cdot \eta}{I_{LIM} \cdot D \cdot V_{IN} \cdot \eta - V_{OUT} I_{OUTMAX}} \qquad (14)$$

Note 4. For the application from equations (10) and (14):

$22uH < L_P < 65uH$, Chosen Lp value: 63uH

TRANSFORMER GUIDELINES: *Primary-secondary leakage inductance causes_overshoot when the switch turns off. To reduce this_it is suggested to couple as best as possible the two windings, separating the primary winding in two half with the secondary winding in between. Check the leakage inductance by measuring primary inductance with shorted secondary winding. A good result for leakage inductance is 1 ~ 10% of the primary inductance.*

LAYOUT GUIDELINES: *the flyback transformer is the site of high dV/dt and can be a source of noise. Therefore please refer to the Datasheet layout section to optimize the board layout around the flyback transformer.*

4. Feedback Components dimensioning

4.1 Reflected Voltage

Analyzing the scope signal of MOSFET Drain voltage (Vsw) during DCM (Discontinuous conduction mode) in a Flyback circuit it is possible to easily identify the output reflected voltage on primary side:

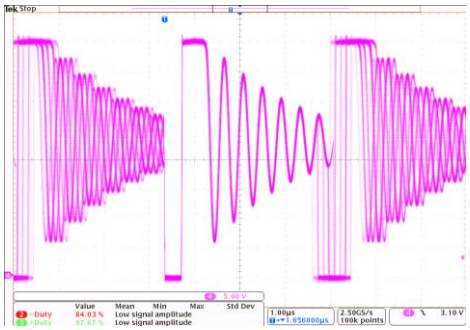


Figure 3: Vsw in DCM flyback

In DCM we can easily identify two times during MOSFET off time, one in which Vsw is constant while the current on the secondary winding decrease to zero and a second time while no current is flowing in the transformer windings and Vsw start to ring due to primary inductance and Drain source capacitance resonance. This oscillation is damped by internal resistances and tends to the input voltage level.

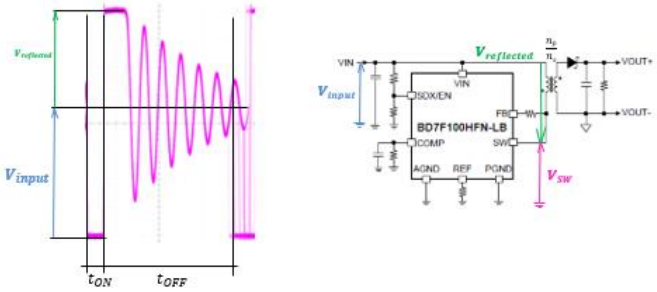


Figure 4: Vsw composition: Vin + Vrefl

During the period of time while secondary winding current is discharging, a constant level voltage is inducted at the secondary winding:

$$V_{sec} = L_S \frac{di_S}{dt} \qquad (15)$$

that reflects on primary winding as:

$$V_{secR} = V_{sec}\frac{N_p}{N_s} \qquad (16)$$

this is added to the V_{in} on the Drain of the MOSFET (Figure 4).

BD7F100HFN measures the reflected voltage to get information about the output voltage directly on primary winding voltage. This value is used as feedback to control the output voltage.

Analyzing more in detail: the output voltage depends on the secondary winding, but also depends on the output diode voltage drop (V_f) and ESR drop from C_{out} as shown in figure 5. These contributions increase as the output current increases. In chapter 4.3 we will analyze how BD7F100HFN compensates for this effect.

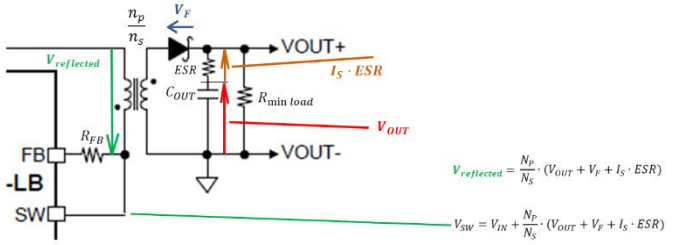


Figure 5: Reflected voltage detail

At nominal output power the BD7F100HFN works in CCM (continuous conduction mode), the Vsw shape is different but with the same composition of Vin and Vreflected:

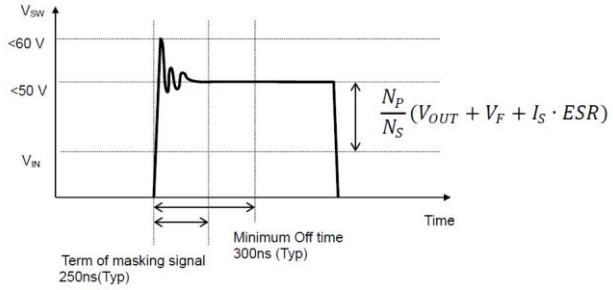


Figure 6: CCM functionality and masking time

Blanking time: The BD7F100HFN starts sampling Vsw for feedback after a blanking time of 250ns to avoid the switching noise. the snubber circuit has to be dimensioned to damp any noise in a time less than the blanking time. The minimum off time is 300ns to give the BD7F100HFN enough time to average a good number of Vsw samples.

For the further information on Transformer used for BD7Fx00xxx-LB Series, Please refer to ***BD7Fx00xxx-LB Series Reference Circuit, application note*** provided by Rohm in the web.

4.2 How the feedback works in details

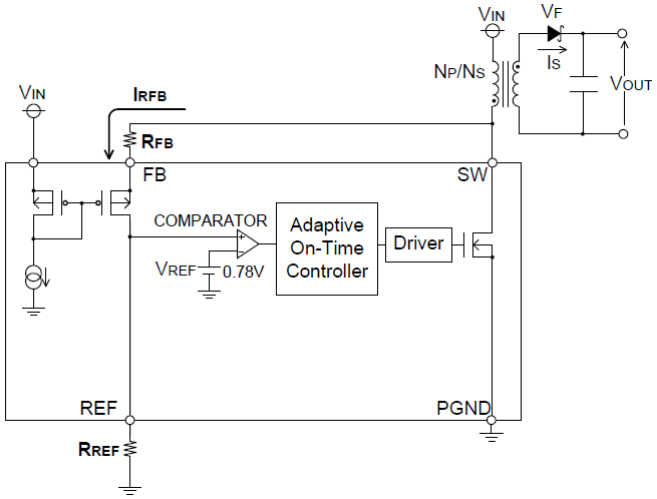


Figure 7: IC Block diagram

The FB pin is kept internally at Vin voltage, so the current (I_{RFB}) is (see Figure 5 for the formula of Vrefl):

$$I_{RFB} = \frac{V_{SW}-V_{IN}}{R_{FB}} = \frac{\frac{N_P}{N_S}(V_{OUT}+V_F+I_S\cdot ESR)}{R_{FB}} = \frac{V_{REF}}{R_{REF}} \qquad (17)$$

With:

V_{REF} - internal voltage reference at 0,78V (Typ.) is used for the feedback on Vout.

R_{REF} – external resistor connected to the pin REF. The BD7F100HFN is designed on the assumption that this resistor has a value of 3,9kOhm

Then R_{FB} is calculated as the following:

$$R_{FB} = \frac{R_{REF}}{V_{REF}}\cdot\frac{N_P}{N_S}\cdot(V_{OUT}+V_F+I_S\cdot ESR) \qquad (18)$$

Note 5. For the application, considering an ESR of 45mOhm it gives: R_{FB}=80.6kOhm

4.3 Load Compensation

If the feedback is setup for the previous paragraph at the maximum output Power/Current, then when the current reduces the output diode voltage and C_{out} ESR voltages reduce and the regulation may not work correctly. In practice without any current based compensation there can be an error in the feedback.

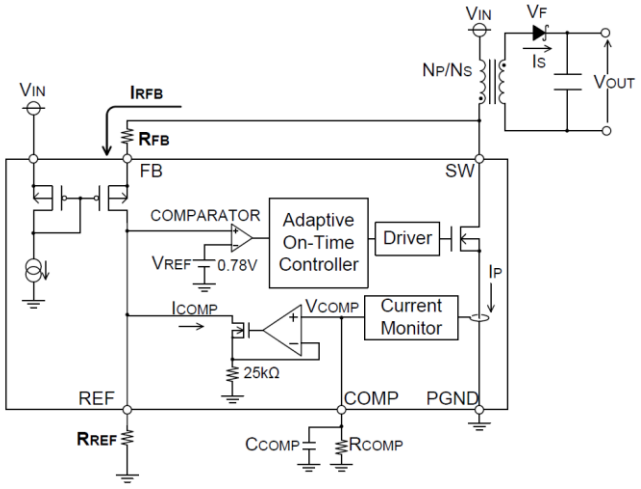


Figure 8: Compensation circuit

To prevent this, the BD7F100HFN internal compensation circuit sinks some current (I_{comp}) from I_{RFB} to change the feedback loop and compensate for the change in output diode and capacitor drops. The secondary current is sensed as function of the primary current by the current monitor block in figure 8:

$$I_P = I_S \cdot \frac{N_s}{N_p} \qquad (19)$$

The current monitor forces a current into Rcomp of I_P reduced by a factor K=1/50k. This increase the voltage at COMP pin. The max value of COMP pin voltage is 0,5V, so therefore the limit for Rcomp is:

$$R_{COMPMAX} = \frac{0.5V}{K \cdot I_P} \quad (20)$$

To avoid instability a compensation capacitor C_{COMP} is added with a value 0.01µF - 0.1 µF. With these values the current is averaged:

$$V_{COMP} = K \cdot I_{P\_AVE} \cdot R_{COMP} \quad (21)$$

The compensation of the output components drop (diode and Cout ESR) is performed by the current I_{COMP} flowing into the internal resistor of value of 25kΩ resistor, then the current value is:

$$I_{COMP} = \frac{V_{COMP}}{25k\Omega} = \frac{K \cdot I_{P\_AVE} \cdot R_{COMP}}{25k\Omega} \quad (22)$$

Now some of the current I_{RFB} flows into the 25kΩ resistor changing the feedback conditions. We will rewrite the equation (17) as:

$$I_{RFB} = \frac{V_{SW} - V_{IN}}{R_{FB}} = \frac{\frac{N_P}{N_S}(V_{OUT} + V_F + I_{S\_AVE} \cdot ESR)}{R_{FB}} = \frac{V_{REF}}{R_{REF}} + I_{COMP} \quad (23)$$

Inserting equation (22) in (23) and rewriting:

$$V_{OUT} + \{V_F + I_{S_{AVE}} \cdot ESR\} = \frac{N_S}{N_P} \cdot \frac{V_{REF}}{R_{REF}} \cdot R_{FB} + \{\frac{N_S}{N_P} \cdot \frac{K \cdot I_{P_{AVE}} \cdot R_{COMP}}{25k\Omega} \cdot R_{FB}\}$$

(24)

To compensate the effect of the output component's drop ($V_F + I_{S_{AVE}} \cdot ESR$) the two parts in the {..} should be equal:

$$V_F + I_{S_{AVE}} \cdot ESR = \frac{N_S}{N_P} \cdot \frac{K \cdot I_{P_{AVE}} \cdot R_{COMP}}{25k\Omega} \cdot R_{FB} \quad (25)$$

Introducing a linear approximation of the diode characteristic (R_{VF}) as the characteristic resistance and inserting the relation between $I_{P_{AVE}}$ and $I_{S_{AVE}}$ (19):

$$I_{S_{AVE}} \cdot R_{VF} + I_{S_{AVE}} \cdot ESR = \left(\frac{N_s}{N_p}\right)^2 \cdot \frac{K \cdot I_{S\_AVE} \cdot R_{COMP}}{25k\Omega} \cdot R_{FB} \quad (26)$$

R_{COMP} value is calculated by:

$$R_{COMP} = 25kohm \cdot \frac{R_{VF} + ESR}{K \cdot R_{FB}} \cdot \left(\frac{N_P}{N_S}\right)^2 \qquad (27)$$

This is a theorical value for Rcomp, but RVF, ESR, and RFB are not easy to determine due to their dependence on many variables including the frequency and PCB layout. Therefore, when determining the best value of RCOMP, monitor VOUT in the application over the full load range and adjust RCOMP

accordingly to minimize the error.

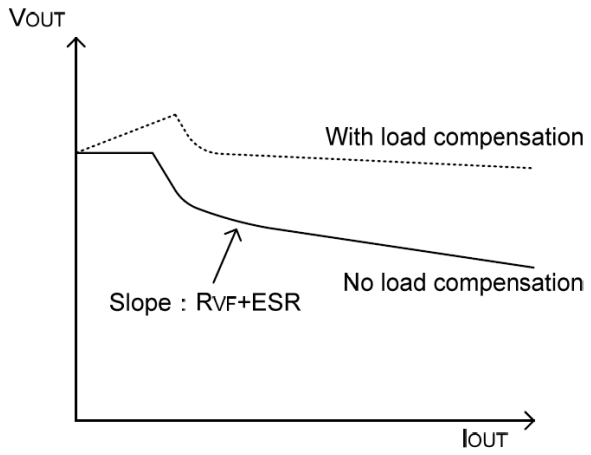


Figure 9: output compensation effect

The effect of load compensation is shown in Figure 9 with a reduction of the output voltage as the output current increases. When the output current is low, in many cases load compensation is not necessary. When load compensation is not required the COMP pin should be shorted to GND.

5. Output Components

5.1 Output Capacitor

For a stable operation select the output capacitor C_{OUT} value based on the following equation:

$$C_{OUT} > 1.6 \cdot 10^{-9} \cdot \frac{1}{L_P} \cdot \left(\frac{N_P}{N_S} \cdot D\right)^2$$

The formula gives 42uF and the value of 47uF is chosen.

Important: during startup the overcurrent protection should not being triggered. This is checked with the following condition:

$$C_{OUT} \leq \frac{1}{2} \cdot \frac{t_{SS} \cdot \left[I_{LIM} \cdot \frac{N_P}{N_S} \cdot (1-D) - I_{OUT\_MAX}\right]}{V_{OUT}}$$

Where: t_{ss}= off start time

Output and for 47uF is verified.

5.2 Output Diode

Since the forward voltage VF of the output diode affects the output voltage, a Schottky barrier diode with a small VF is recommended.

During on time the voltage on secondary diode is expressed by the following expression:

$$V_{ton} = V_{IN} \cdot \frac{N_S}{N_P} + V_{OUT}$$

When selecting a diode, the forward current and voltage must not exceed the rated values.

Note 6. For the application the reflected voltage is: V_{ton} = 15V and the selected diode is: ROHM RB160M-40

5.3 Minimum Load Current

To sense the output voltage at the primary side, a switching must occur. For this reason a minimum load is required.

The required minimum load current is:

$$I_{OUT\_MIN} = 7.5 \cdot 10^{-9} \cdot \frac{V_{IN}^2}{L_P \cdot V_{OUT}}$$

Note 7. The formula gives I_{OUT_MIN} of 13.7mA and a R_{out} of 328Ohm.

6. Snubber Components

The snubber dimensioning needs attention because it can affect the feedback loop in this application. The snubber has to prevent overshoot at the drain of the MOSFET that exceeds the maximum pulse voltage of the MOSFET and ensure that the oscillation will finish less than 250ns after MOSFET turn off. See Figure 6 for details.

Two different snubbers configurations can be added externally:

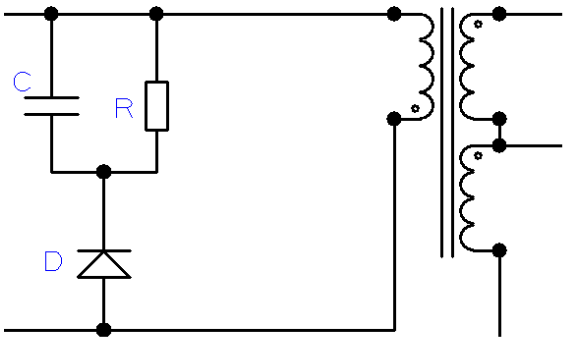


Figure 10: RCD Snubber dimensioning

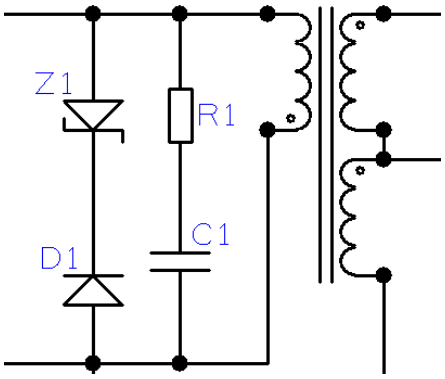


Figure 11: Diode-Zener Clamp

6.1 RCD Snubber Dimensioning

After MOSFET switch off the primary inductance energy is transferred to the secondary and then to the output capacitor, but the energy stored in the leakage capacitance of the transformer has to be dissipated before the next cycle starts.

Leakage inductance energy is given by:

$$E_{Lleak} = \frac{1}{2} L_{Leak} I_{pripeak}^2$$

$I_{pripeak}$ is the peak current in the internal MOSFET that is fixed at 1,25A_typ. The resistor R is very important in limiting the maximum voltage spike. A lower Rclamp will reduce the maximum admissible overvoltage spike (V_{spike}) but increases the power dissipation. This is given by:

$$R = \frac{4V_{spike}}{L_{Leak} I_{pripeak}^2 f_{sw}}$$

The capacitor C needs to be large enough to limit the overvoltage when all the leakage inductance energy is absorbed. The Diode should be a superfast or SBD type.

Note 8. For the application with an $L_{Leak} < 1{,}8\mu H$ it's calculated:

R = 2kOhm

C = 220nF

D = 1SS400SM

6.2 Diode Zener Clamp

The Zener voltage of the diode should be calculated to suppress any voltage that exceeds the maximum MOSFET Vds pulse voltage

$$V_{ZENER} = V_{DSmax\_pulse} - (V_{IN} + V_{refl})$$

The resistor and capacitor will filter the pulse to reduce EMI noise. The values should be chosen based on EMI measurement. The Diode should be a FRD or SBD type.

Z1 : KDZ18B

D1: 1SS400SM

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