

ROHM Solution Simulator

Input Voltage 5.0 V to 35 V

Output Switch Current 2 A

1 ch Step-Down Switching Regulator

BD9060HFP/BD9060F Simulation Guide

This document provides a guide for performing simulations on the BD9060HFP/BD9060F using the ROHM Solution Simulator. This document takes the BD9060HFP as an example for description. The pin layout should be replaced for the BD9060F.

Constant value setting and simulation

The item that can be simulated on the BD9060HFP/BD9060F using the ROHM Solution Simulator is confirmation of phase compensation on a Bode plot. For the design of the constant value settings, refer to the section of "Selection of components externally connected" in the data sheet. The simulation procedure is shown in the following pages.

Information • For more details on the products, see the following product information links.

▶ Product information links: [BD9060HFP](#), [BD9060F](#)

• For a comparison between the actual equipment and the simulation results, see the following modeling reports.

▶ Modeling reports: [BD9060HFP](#), [BD9060F](#)

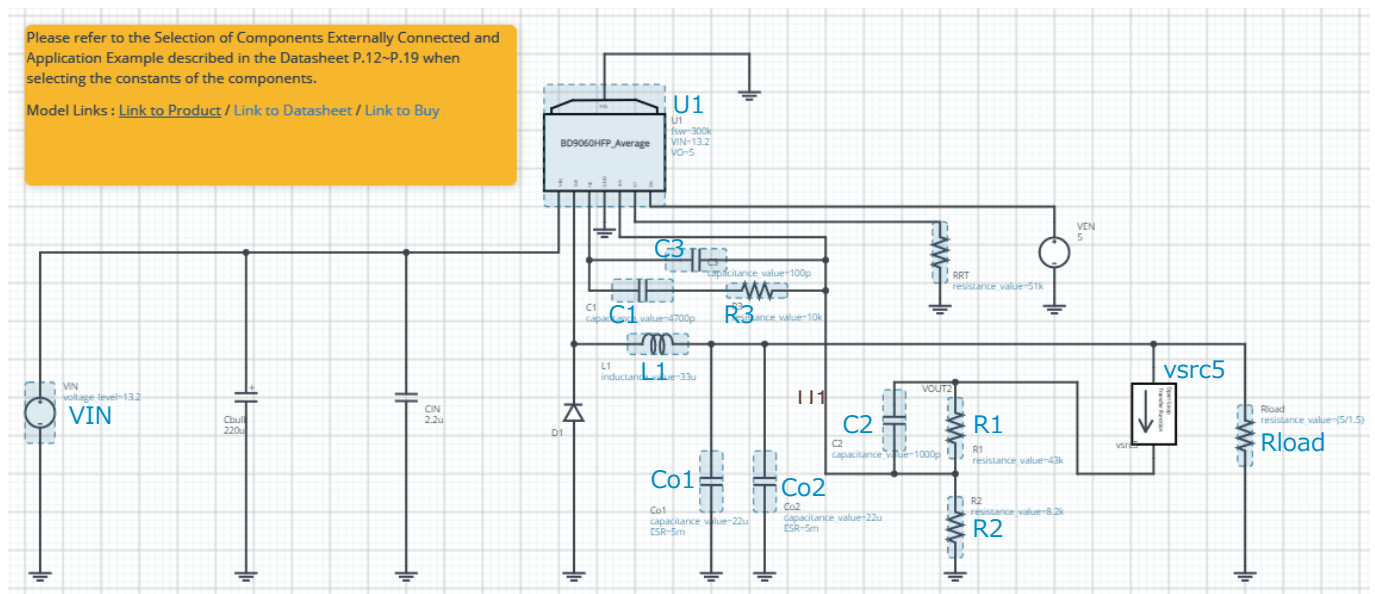
• The procedure in this document uses the simulator provided by ROHM. For those who have other simulators, we provide the SPICE models separately. They are available from the product information links above.

Detailed procedure

Phase compensation circuit: Phase margin, gain margin

Simulator used: ROHM Solution Simulator

Simulation type: Frequency Domain



To improve the response performance, it is necessary to increase zero cross frequency f_c of the loop gain. However, increasing the frequency decreases the phase margin due to the phase delay, reducing the stability. Therefore, there is a trade-off relationship between the response performance and the stability. In addition, since the switching regulator application performs sampling at the switching frequency, it is necessary to suppress the gain at the switching frequency. Therefore, as the design values, it is necessary to set zero cross frequency f_c to no more than $1/10$ of switching frequency f_{SW} .

The phase compensation is set with R3, C1, and C3 connected to the FB pin as well as C2 connected to feedback resistor R1. The point for achieving the stability with the phase compensation is to cancel the phase delay due to the two poles, f_{P1} and f_{P2} , that are formed in the system by inserting the phase advance due to the two zeros, f_{Z1} and f_{Z2} .

The phase margin, the gain margin, and the zero cross frequency are checked with the simulation below.

Detailed procedure

Phase compensation circuit: Phase margin, gain margin (continued)

Calculation formulas for the various frequencies

- The frequencies of the two poles (phase delay) and the two zeros (phase advance) described above as well as the frequencies of the poles produced by the circuit can be calculated with the following equations. Note that, in this circuit example, it is not necessary to set f_{p2} with R4 because f_{ESR} is located higher than the switching frequency.

$$f_{p1} = \frac{C1 + C3}{2\pi \cdot R3 \cdot C1 \cdot C3} \quad [Hz] \qquad f_{p2} = \frac{1}{2\pi \cdot R4 \cdot C2} \quad [Hz]$$

$$f_{z1} = \frac{1}{2\pi \cdot R3 \cdot C1} \quad [Hz] \qquad f_{z2} = \frac{1}{2\pi \cdot (R1 + R4) \cdot C2} \quad [Hz]$$

$$f_{LC} = \frac{1}{2\pi} \sqrt{\frac{R_o + DCR}{L1 \cdot C_o(R_o + ESR)}} \quad [Hz] \qquad f_{ESR} = \frac{1}{2\pi \cdot ESR \cdot C_o} \quad [Hz]$$

where

 C_o : Capacitance of the output capacitor^(NOTE 1) [F]

$$R_o: \text{Load resistance } [\Omega] = \frac{\text{Output voltage } [V]}{\text{Load current } [A]} \quad (1)$$

DCR : Direct current resistance of the inductor [Ω]

ESR : Equivalent series resistance of the output capacitor [Ω]

(NOTE 1) Multilayer ceramic capacitors (MLCCs) show a lower capacitance than the nominal value due to the DC bias characteristics and the AC voltage characteristics. To perform simulations accurately, use the actual capacitances instead of the nominal capacitances.

- Calculate the various frequencies using the values from an example of the design parameters. Here, the calculations are performed under the assumption that MLCCs with the nominal capacitance of 22 μF are used for output capacitances Co1 and Co2 and their actual capacitance is 13.8 μF. R_o is calculated from Ohm's law (Equation 1). f_{LC} is calculated at the maximum load current. In this example, the value is set to 1.5 A. Although DCR is the direct resistance of the inductor L1, it is set to zero for this calculation because its effect is insignificant.

$$f_{p1} = \frac{C1 + C3}{2\pi \cdot R3 \cdot C1 \cdot C3} = \frac{4700pF + 100pF}{2\pi \times 10k\Omega \times 4700pF \times 100pF} = 163 \text{ kHz}$$

$$f_{p2} = \frac{1}{2\pi \cdot R4 \cdot C2} = \frac{1}{2\pi \times 0 \times 1000pF} = \infty \text{ Hz}$$

$$f_{z1} = \frac{1}{2\pi \cdot R3 \cdot C1} = \frac{1}{2\pi \times 10k\Omega \times 4700pF} = 3.39 \text{ kHz}$$

$$f_{z2} = \frac{1}{2\pi \cdot (R1 + R4) \cdot C2} = \frac{1}{2\pi \times (43k\Omega + 0) \times 1000pF} = 3.70 \text{ kHz}$$

$$f_{LC} = \frac{1}{2\pi} \sqrt{\frac{R_o + DCR}{L1 \cdot C_o(R_o + ESR)}} = \frac{1}{2\pi} \sqrt{\frac{\frac{5V}{1.5A} + 0\Omega}{33\mu H \cdot 13.8\mu F \times 2 \left(\frac{5V}{1.5A} + \frac{5m\Omega}{2} \right)}} = 5.27 \text{ kHz}$$

$$f_{ESR} = \frac{1}{2\pi \cdot ESR \cdot C_o} = \frac{1}{2\pi \cdot \frac{5m\Omega}{2} \cdot 13.8\mu F \times 2} = 2.31 \text{ MHz}$$

Detailed procedure

Phase compensation circuit: Phase margin, gain margin (continued)

Checking the standards for the stable operation

- If the relations among the various frequencies satisfy the following expressions as the standards, the frequency characteristics can be considered to be optimized. Apply the calculation results in the previous page to the relational expressions.

1. $0.2 f_{LC} \leq f_{Z1} \leq f_{LC}$

$$1.14kHz \leq 3.39kHz \leq 5.72kHz$$

It is confirmed that the condition of the standard is satisfied.

2. $0.5 f_{LC} \leq f_{Z2} \leq 2 f_{LC}$

$$2.86kHz \leq 3.70kHz \leq 11.4kHz$$

It is confirmed that the condition of the standard is satisfied.

3. $f_{P1} \approx 0.5 f_{SW}$

$$163kHz \approx 150kHz$$

At a switching frequency of 300 kHz, it is confirmed that the condition of the standard is satisfied.

4. $f_{P2} \approx f_{ESR}$

$$\infty Hz \approx 2.31MHz$$

For f_{P2} , it is not necessary to set f_{P2} with R4 if f_{ESR} is located higher than the switching frequency.

$f_{ESR} 2.31 MHz > \text{Switching frequency } 300 kHz$

Detailed procedure

Phase compensation circuit: Phase margin, gain margin (continued)

Setting the IC properties

- Set the properties of switching regulator IC U1.
 1. Parameter FSW: Sets the switching frequency.
 2. Parameter VIN: Sets the input voltage.
 3. Parameter VO: Sets the output voltage.

Setting the simulation frequency

- Set "Start Frequency" and "End Frequency" to 0.1 Hz and 1 MHz, respectively, so that the whole picture of a Bode plot can be observed.

Performing the simulation

- Click ► to perform the simulation. Wait until the simulation is completed.

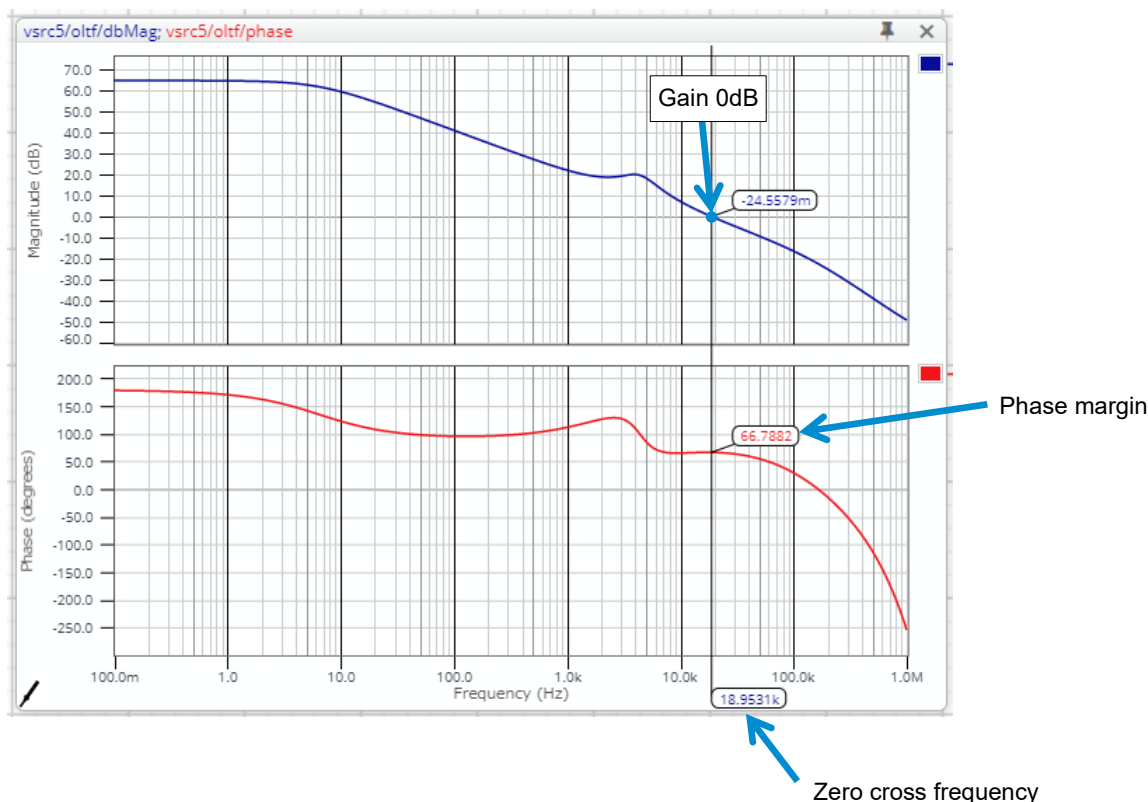
Detailed procedure

Phase compensation circuit: Phase margin, gain margin (continued)

Displaying the characteristics and checking the values

- On the graph displayed in the initial screen, the characteristics of the magnitude and the phase are plotted. If the graph is closed, follow the next procedure to display the graph.
 - Drag and drop "Waveform Probe" onto the symbol of vsrc5 in the circuit diagram.
 - When the waveform dialog box is opened, go to folder vsrc5 and then oltf. Then, select dbMag to display the magnitude characteristics.
 - Drag and drop the probe symbol on the lower left of the graph onto the symbol of vsrc5 again.
 - When the waveform dialog box is opened again, go to folder vsrc5 and then oltf. Then, select phase to display the phase characteristics.
- Right-click on the graph and select "Multi Trace" in "Display Mode" from the pop-up menu. The magnitude characteristics and the phase characteristics are displayed on the top and bottom graphs, respectively.
- Right-click on the graph and select "Add Cursor" from the pop-up menu.
- When the cursor is displayed, move the cursor over the point where the magnitude characteristics are zero. In practice, the point will be the closest to zero due to the limitation of the simulation resolution.
- Read the cursor value for the phase characteristics. This is the value of the phase margin.
- Read the cursor value for the frequency axis. This is the zero cross frequency.

Phase margin and zero cross frequency, when the load current is at the maximum (= 1.5 A)

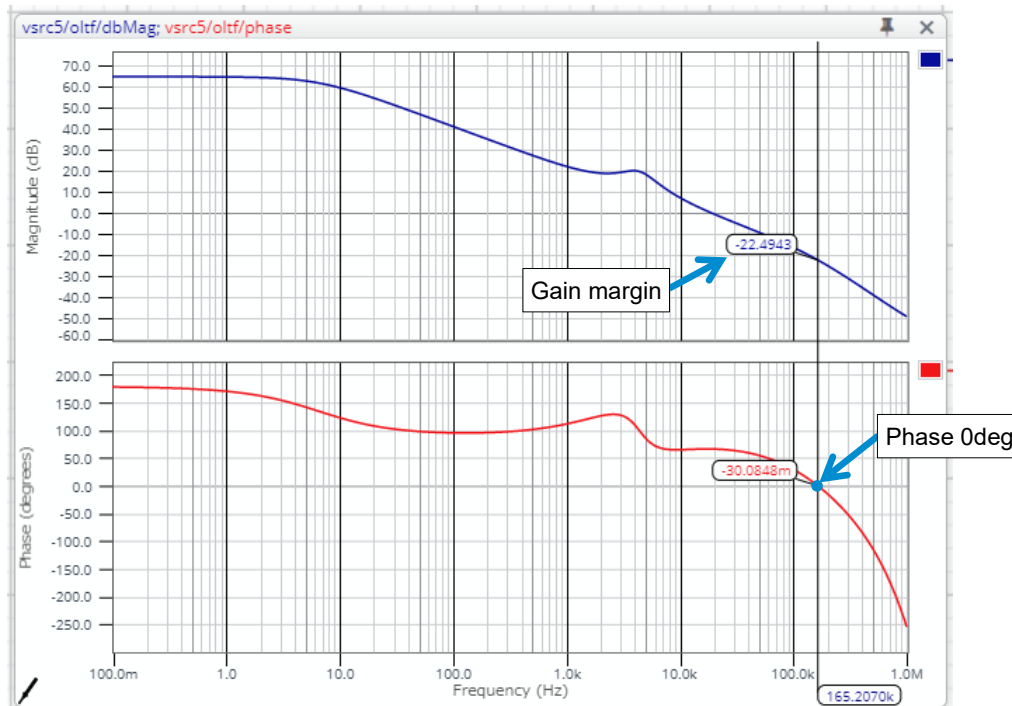


Detailed procedure

Phase compensation circuit: Phase margin, gain margin (continued)

7. Next, move the cursor over the point where the phase characteristics are zero. In practice, the point will be the closest to zero due to the limitation of the simulation resolution.
8. Read the cursor value for the magnitude characteristics. This is the value of the gain margin.

Gain margin, when the load current is at the maximum (= 1.5 A)



Checking the requirements for the stable operation

- Check whether the following requirements are satisfied. If they are satisfied, the operation can be judged to be stable.

1. Zero cross frequency $f_c < \frac{\text{Switching frequency } f_{sw}}{10}$

$$18.9\text{kHz} < 30\text{kHz}$$

It is confirmed that the requirement is satisfied.

2. Phase margin: 45° or greater

$$66.7^\circ > 45^\circ$$

It is confirmed that the requirement is satisfied.

3. Gain margin: -10 dB or less

$$-22.5\text{dB} < -10\text{dB}$$

It is confirmed that the requirement is satisfied.

Notes

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