ROHM Solution Simulator

Input Voltage 3.5 V to 36 V
Output Switch Current 2.5 A
1ch Step-Down Switching Regulator

BD90620EFJ/BD90620HFP Simulation Guide

This material provides a guide for performing simulations on the BD90620EFJ/BD90620HFP using the ROHM Solution Simulator.
This user's guide describes the BD90620EFJ of the HTSOP-J8 package, but there is also the BD90620HFP of the HRP7 package.
Please refer to the terminal layout of the data sheet and read as appropriate.

Contents

Information • For more details on the product, see the following product information link.

- Product information link: BD90620EFJ, BD90620HFP

• For a comparison between the actual equipment and the simulation results, see the following modeling reports.

- Modeling reports: Modeling report 1, Modeling report 2

Constants and simulations

Since the BD90620EFJ has several external components, it is necessary to determine the constants to match a design parameter. Table 1 shows the procedure for the designs and the simulations.

The constants are determined in order from the first item in the Design item column.

The Related parts name column shows the parts symbols.

The Simulator (NOTE 1) and the analysis type column shows a simulator environment and the analysis type. The "Frequency Domain" and the "Time Domain" are available with ROHM Solution Simulator in ROHM Official Site. Only limited constants are changeable. To make the schematic change, use "SystemVision®Cloud". Clicking [Edit in systemvision.com] button in ROHM Solution Simulator environment, it is available to change the circuit and to simulate. Same as ROHM Solution Simulator, the "Frequency Domain" and the "Time Domain" are available.

Checkpoints and the characteristics column show the location where the waveform displayed, and the characteristics checked.

For more details, see the page in the page column.

Since each component influence individually, simulation items need to simulate again, to determine all the parts constants, all the characteristics need to simulate again.

Table 1. List of the design procedures and the operation check methods

Design item	Related parts name	Simulator (NOTE 1) and the analysis type	Checkpoints and the characteristics	Page
1. Output voltage	R1, R2	Time Domain	Output pin Output voltage	5
2. Switching frequency	RRT	Time Domain	Switching pin Switching frequency	8
3. Inductor	L1	Time Domain	Inductor Inductor current	11
4. Output capacitor	CO1, CO2	Time Domain	Output pin, output capacitor Output ripple voltage, capacitor ripple current	16
5. Input capacitor	Cin	Calculation equation	Input capacitor Ripple current	21
6. Schottky barrier diode	D1	Calculation equation	Schottky barrier diode Diode current, loss	22
7-1. Phase compensation circuit Phase margin, gain margin	R3, C1 CO1, CO2	Frequency Domain	Feedback circuit Phase margin, gain margin	24
7-2. Phase compensation circuit Load transient response	R3, C1 CO1, CO2	SystemVision®Cloud Time Domain	Output pin Load transient response	31
8. Soft start	RRT	Time Domain	Output pin Output voltage	36

(NOTE 1) See the next page

Constants and simulations (continued)

(NOTE 1) Simulator and the analysis type

- Frequency Domain : The frequency analysis to be performed in the ROHM Solution Simulator environment.
- Time Domain : The transient analysis to be performed in the ROHM Solution Simulator environment.
- SystemVision®Cloud Frequency Domain : The frequency analysis to be performed in the SystemVision®Cloud environment.
- SystemVision®Cloud Time Domain : The transient analysis to be performed in the SystemVision®Cloud environment.
- Mathematical equation : Use mathematical equation instead of simulators to determine the characteristics.

Information Detailed procedures are shown below. For more detail simulation, it is able to get the SPICE model provided following link to perform in other simulation environment.

- SPICE model: BD90620EFJ, BD90620HFP

SystemVision® is a registered trademark of Mentor Graphics Corp.

Design parameter

The schematic can set some parameters. Table 2 is a sample. Famous items and values are shown below, situations of mounting devices or its functions change them.

Table 2. Example of the design parameter

Item	Value
Input voltage	min 6 V, nominal 13.2 V, max 18 V
Output voltage	5 V ±10%
Output ripple voltage	20 mV p-p or less
Output voltage, load transient response	±3% or less (when I_{OUT} = 0.8 A → 1.5 A → 0.8 A)
Output current	min 0.3 A, nominal 0.8 A, max 1.5 A
Switching frequency	500 kHz
Soft start time	1.38 ms

Detailed procedures

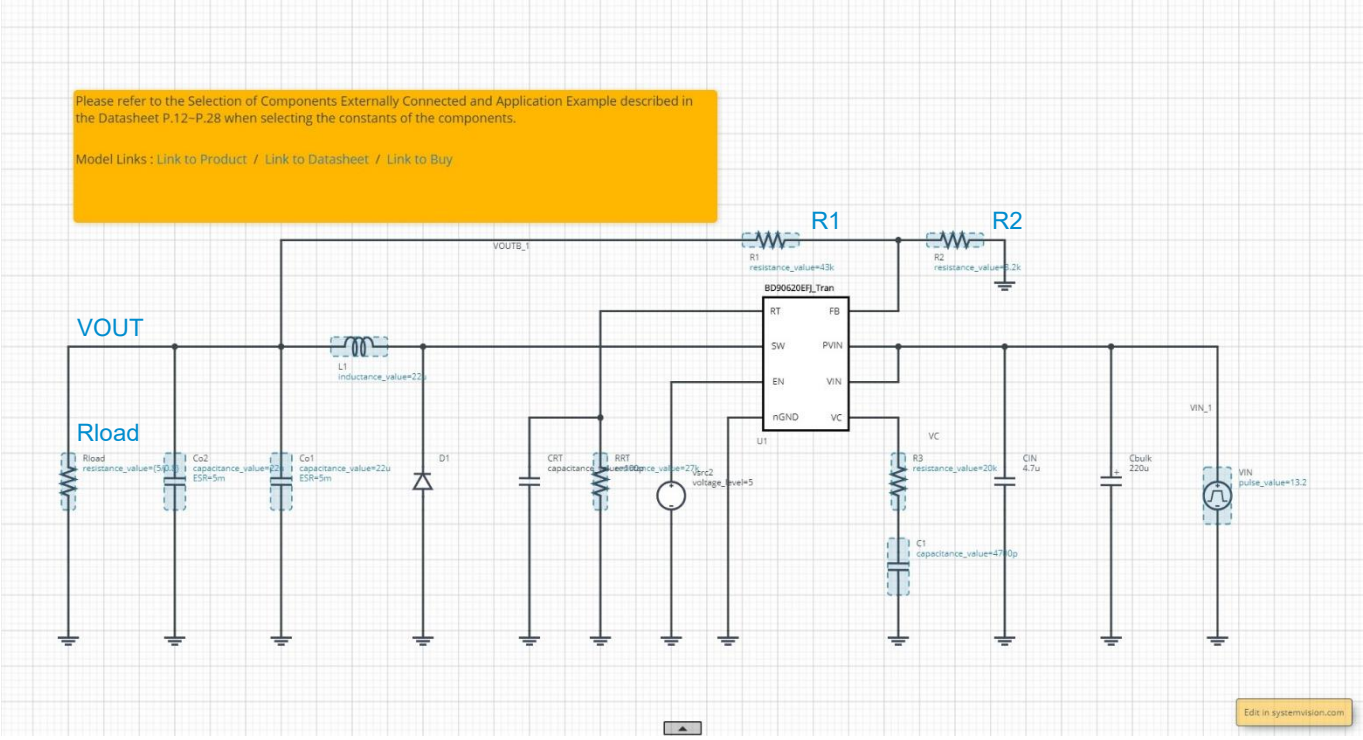
1. Output voltage

Simulator to be used: ROHM Solution Simulator

Simulation type: Time Domain

External component to be designed: R1, R2

Monitoring point: VOUT



Calculate the output voltage

● The output voltage can be calculated with the following equation.

$$V_{OUT} = 0.8 \cdot \frac{R1 + R2}{R2} \qquad [V]$$

Substituting R1 of 43kΩ, R2 of 8.2kΩ, the output voltage is around 5V.

$$V_{OUT} = 0.8 \times \frac{43k + 8.2k}{8.2k} = 4.995 \qquad [V]$$

Detailed procedures

1. Output voltage (continued)

Place the load resistance

● The load resistance Rload describes from Ohm's law, and calculates below equation.

$$Rload = \frac{V_{OUT}}{I_{LOAD}} \quad [\Omega]$$

With low current load, then high load resistance, an overshoot is observed. It makes convergence time and simulation time long because of low negative feedback. This time, set 0.8A load to shorten convergence time and simulation time. Above equation, load resistance is 6.25Ω.

$$Rload = \frac{5}{0.8A} = 6.25 \quad [\Omega]$$

Optimize simulation time

● It is necessary to set longer time than softstart time that this IC mounts. Setting RRT=27kohm, the softstart time is 1.38ms, and considering output convergence time, set simulation time 4ms.

Perform the simulation

● Click ▶ to perform the simulation and wait until the simulation is completed.

Information	The simulation takes approximately 14 minutes. The time varies with the server usage rate. For Advanced Options, "Balanced" is recommended.

Detailed procedures

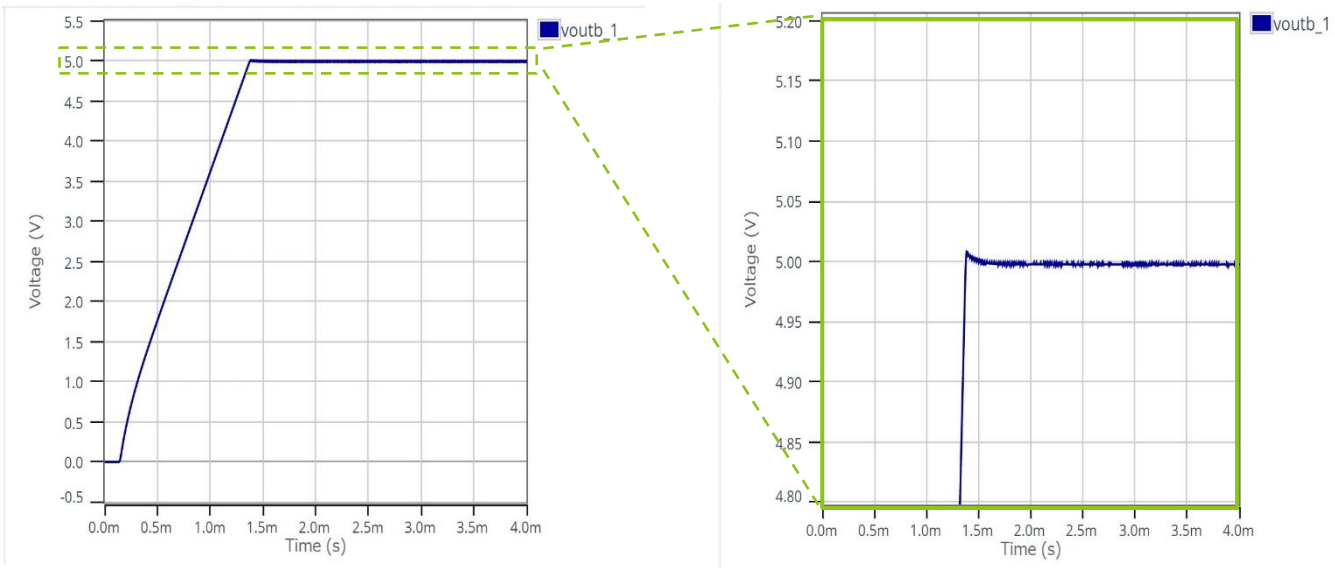
1. Output voltage (continued)

Display and check the voltage

1. Drag and drop the "Waveform Probe" onto VOUT to display.

2. Check stability of its voltage with zooming the wave.

3. Display a cursor at voltage, check if its value within the value of design parameter example.



Detailed procedures

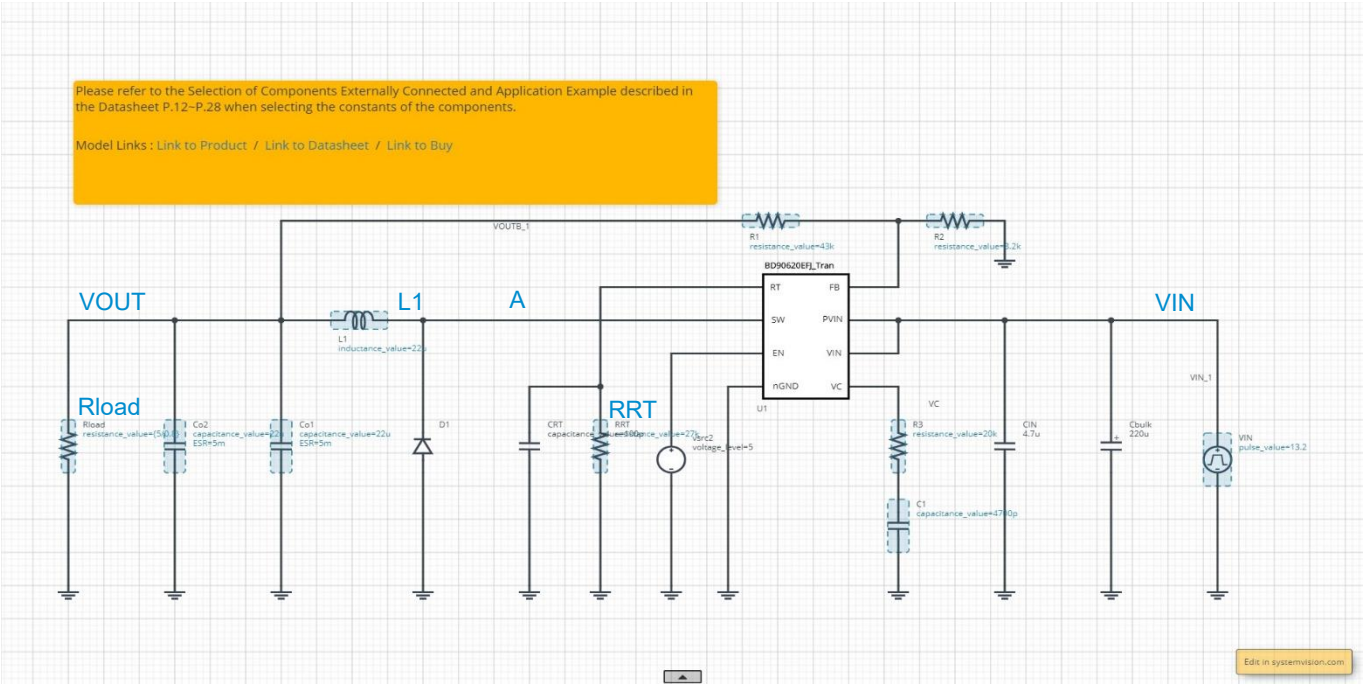
2. Switching frequency

Simulator to be used: ROHM Solution Simulator

Simulation type: Time Domain

External component to be designed: RRT

Monitoring point: A in the figure below



Set the switching frequency

● The switching frequency is set with the value of resistance RRT.

To set the value, see the graph and table provided in the "Selection of the switching frequency setting resistor R_{RT}, C_{RT}" section of the Datasheet.

Check the load current

● Since the waveform should be loaded for continuous operation, it can be simple and readable switching frequency during the operation that is calculated with the following inequality.

$$I_{LOAD} > \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{2 \cdot V_{IN} \cdot f_{SW} \cdot L1} > \frac{(18V - 5V) \times 5V}{2 \times 18V \times 500kHz \times 22\mu H} = 164m \quad [A]$$

Setting I_{LOAD} to 0.8A that is satisfied with above, check if it is within the value of design parameter example.

Detailed procedures

2. Switching frequency (continued)

Optimize simulation time

● It is necessary to set longer time than softstart time that this IC mounts. Setting RRT=27kohm, the softstart time is 1.38ms, and considering output convergence time, set simulation time 4ms.

Perform the simulation

● Click ▶ to perform the simulation and wait until the simulation is completed.

Information	The simulation takes approximately 14 minutes. The time varies with the server usage rate. For Advanced Options, "Balanced" is recommended.

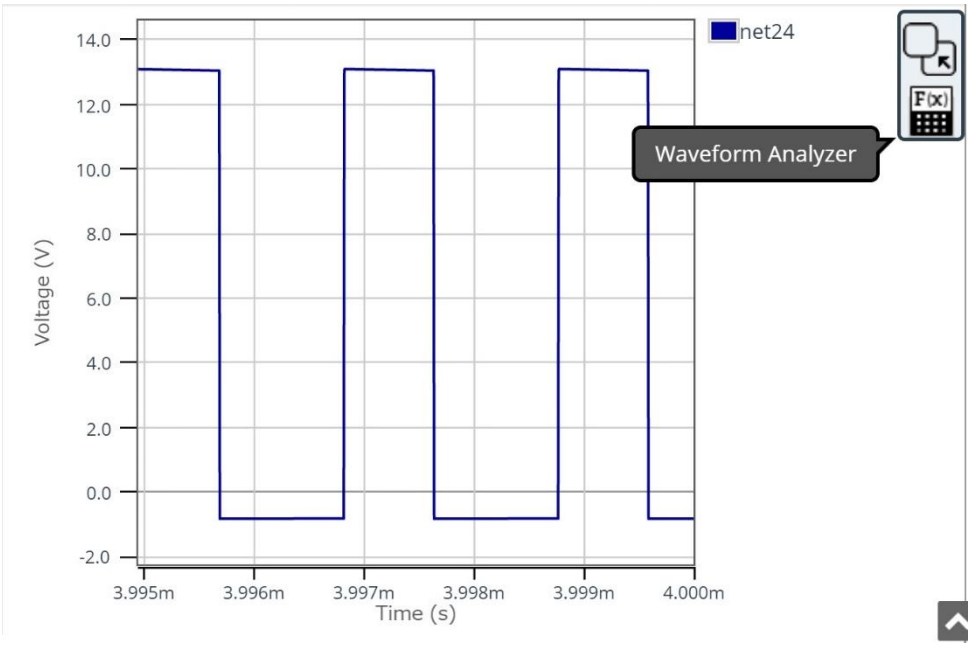
Display the waveform and read the frequency

1. Drag and drop the "Waveform Probe" onto A to display.

2. Move the cursor over the waveform and right click.

3. Select "Plot in Viewer" from the pop-up menu.

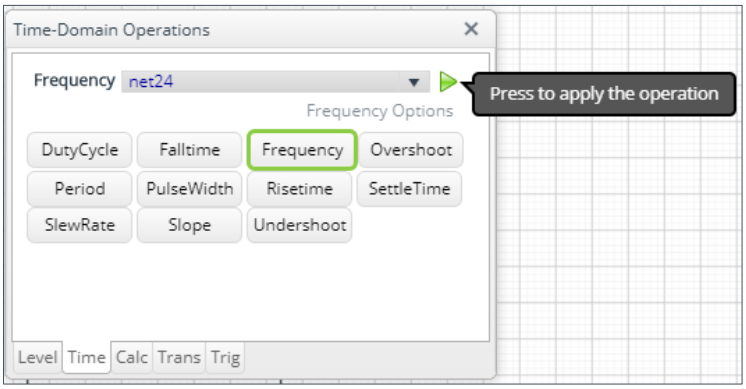
4. Zoom the waveform around the end with the viewer, and click the "Waveform Analyzer" icon on the right.



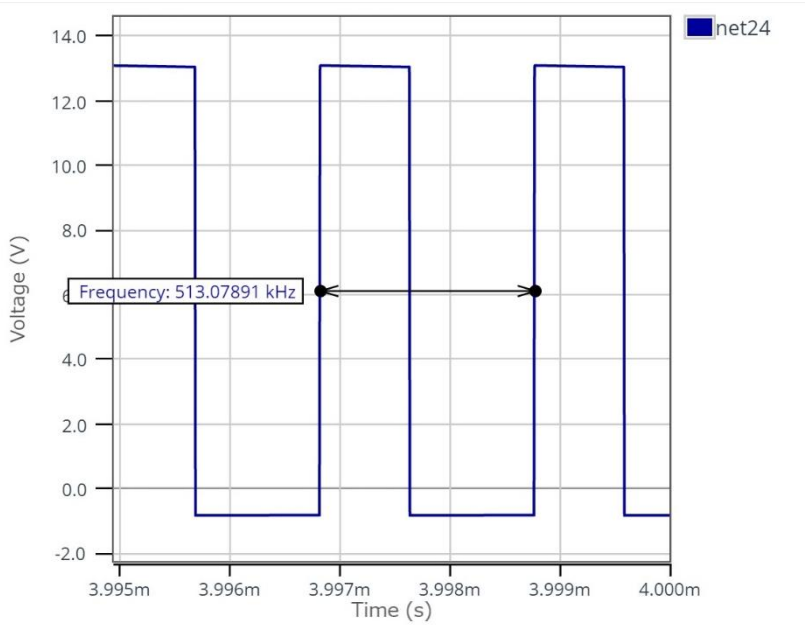
Detailed procedures

2. Switching frequency (continued)

5. When the "Operations window" is displayed, select the "Time" tab at the bottom and click the [Frequency] button. Finally, clicking ▶ displays the frequency on the waveform.



6. Check that the frequency is within the design target value.



Detailed procedures

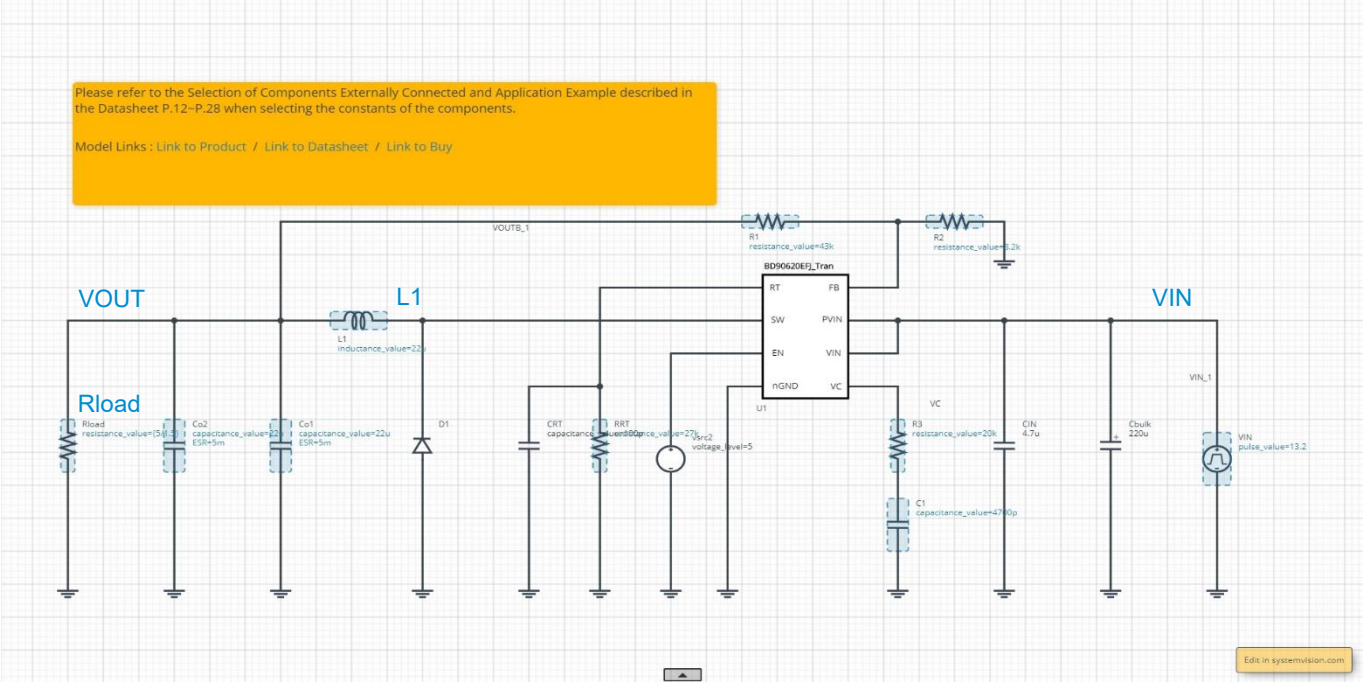
3. Inductor

Simulator to be used: ROHM Solution Simulator

Simulation type: Time Domain

External component to be designed: L1

Monitoring point: L1



Calculate the inductance value

● The inductance value is calculated with the following equation. Set the inductor ripple current to approximately 30% of the IC allowable current.

$$L1 = \frac{(V_{IN(Max)} - V_{OUT}) \cdot V_{OUT}}{V_{IN(Max)} \cdot f_{SW} \cdot \Delta I_L} \quad [H]$$

$V_{IN(Max)}$: Maxmum input voltage of the value of the design parameter example

ΔI_L: Inductor ripple current = allowable current × 0.3

The inductance value is calculated as follows using the values of the design parameter example.

$$L1 = \frac{(18V - 5V) \times 5V}{18V \times 500kHz \times 2.5A \times 0.3} = 9.63 \ \mu H$$

Select a 10 µH inductor from commercial products.

Detailed procedures

3. Inductor (continued)

Check discontinuous load current

- Low current load occurs discontinuous operation. Following inequality calculates continuous load current situation. When the load current is small, to avoid discontinuous operation, it may make inductance value large.

$$I_{LOAD} > \frac{\left(V_{IN(Max)} - V_{OUT}\right) \cdot V_{OUT}}{2 \cdot V_{IN(Max)} \cdot f_{SW} \cdot L1} \quad [A]$$

Substituting the values of design parameter example to the above inequality, the current under 0.36A causes discontinuous operation.

$$I_{LOAD} > \frac{(18V - 5V) \times 5V}{2 \times 18V \times 500kHz \times 10\mu H} \quad [A]$$

$$I_{LOAD} > 0.36 \ A$$

Now, minimum load current (0.3A) of the design parameter example occurs discontinuous operation. Then, to operate continuously, it is necessary to make inductance value large to 0.2A load current with a margin. The inequality transforms to below.

$$L1 > \frac{\left(V_{IN(Max)} - V_{OUT}\right) \cdot V_{OUT}}{2 \cdot V_{IN(Max)} \cdot f_{SW} \cdot I_{LOAD}} \quad [H]$$

$$L1 > \frac{(18V - 5V) \times 5V}{2 \times 18V \times 500kHz \times 0.2A} \quad [A]$$

$$L1 > 18.1 \ \mu H$$

Select a 22μH inductor from commercial products.

Detailed procedures

3. Inductor (continued)

Check the maximum output current

- Check inductor current cannot over the minimum value of the over current protection. The relationship describes following inequality.

$$I_{SWLIMIT(Min)} \geq I_{OUT(Max)} + \frac{\Delta I_L}{2} \qquad [A]$$

$I_{OUT(Max)}$: Maximum output current of the value of the design parameter example

ΔI_L:Inductor ripple current

At the beginning of this chapter, calculated inductance value is 9.63uH with IC allowable current × 0.3. To make the discontinuous operation current smaller, the inductance value is now 22uH. Therefore, inductor ripple current is smaller than initial calculation. Recalculate inductance ripple current as same as before.

$$\Delta I_L = \frac{\left(V_{IN(Max)} - V_{OUT}\right) \cdot V_{OUT}}{V_{IN(Max)} \cdot f_{SW} \cdot L1} \qquad [A]$$

$$\Delta I_L = \frac{(18V - 5V) \times 5V}{18V \times 500kHz \times 22\mu H} = 328mA$$

Recalculating inductance ripple current with that value of 22uH, recheck to be satisfied the inequality.

$$2.5\ [A] \geq 1.5A + \frac{328mA}{2} \qquad [A]$$

$$2.5\ [A] \geq 1.664\ [A]$$

This example shows the inequality satisfied that maximum output current is not over the minimum over current protection.

Detailed procedures

3. Inductor (continued)

Prevent the subharmonic oscillation

- The current mode DC/DC converters in continuous operation with an OnDuty ratio over 50% may cause a subharmonic oscillation. The oscillation can be prevented in the inequality. Larger inductance value may be easily satisfied the inequality.

$$L1 \geq \frac{2 \cdot D - 1}{2 \cdot (1 - D)} \cdot R_S \cdot \frac{V_{IN(Min)} - V_{OUT}}{m} \quad [H]$$

D: OnDuty of the switching pulse $= \dfrac{V_{OUT}}{V_{IN(Min)}}$

$V_{IN(Min)}$: Minimum source voltage of the design parameter example

R_S: Current feedback coefficient = 4.0 μ $[A/A]$

m: Inclination of the slope compensation current $= 6 \times 10^{-6} f_{SW}$

f_{SW}: Switching frequency $[Hz]$

The value of 22μH calculated before satisfies the inequality with the values of design parameter example.

$$L1 \geq \frac{2 \cdot \frac{5V}{6V} - 1}{2 \cdot \left(1 - \frac{5V}{6V}\right)} \times 4\mu A/A \times \frac{6V - 5V}{6 \times 10^{-6} \times 500kHz} \quad [H]$$

$L1 \geq 2.7$ μH

Place the load resistor

- To check the maximum value of the inductor current, set the load current to the maximum value of the design target example. In this example, since the load current is set to 1.5 A, load resistor Rload is 3.33Ω (= 5 V/1.5 A).

Optimize simulation time

- It is necessary to set longer time than softstart time that this IC mounts. Setting RRT=27kohm, the softstart time is 1.38ms, and considering output convergence time, set simulation time 4ms.

Detailed procedures

3. Inductor (continued)

Perform the simulation.

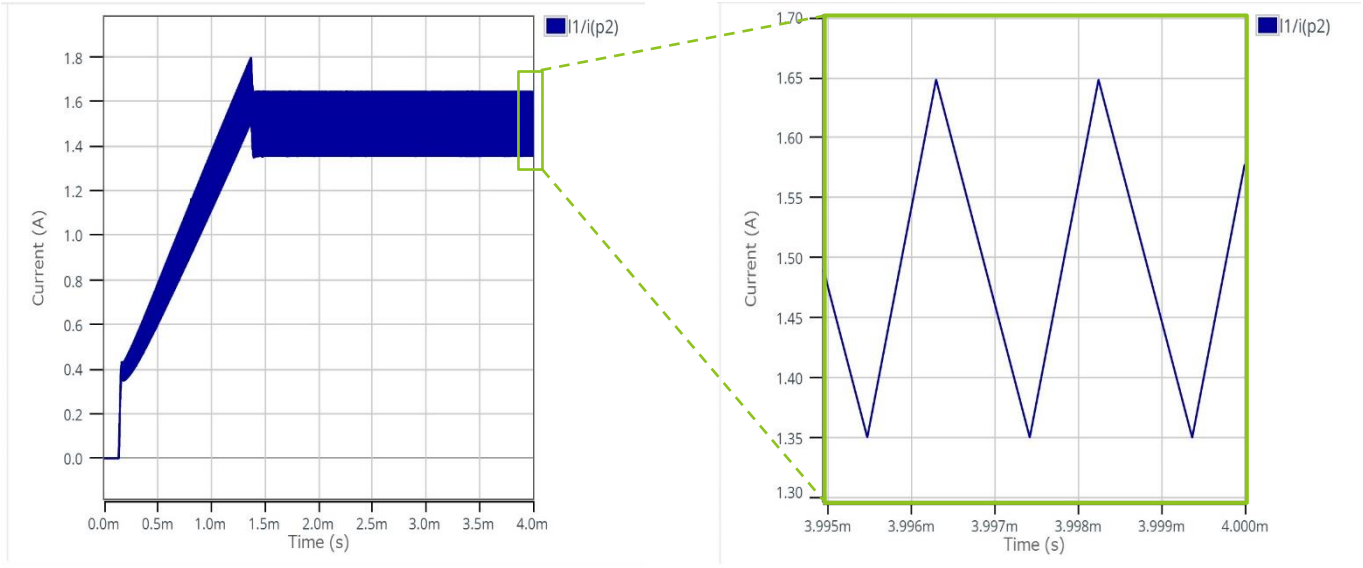
● Click ▶ to perform the simulation and wait until the simulation is completed.

Information	The simulation takes approximately 14 minutes. The time varies with the server usage rate. For Advanced Options, "Balanced" is recommended.

Display the waveform and check the inductor current.

1. Drag and drop "Waveform Probe" onto the symbol of L1 in the circuit diagram. When the waveform dialog box is opened, select the current waveform "i (p2)" to display the waveform.

2. Zoom the area where the current is stable and read the peak current with the cursor. Check if the reading value matches the maximum output current calculated before.



Detailed procedures

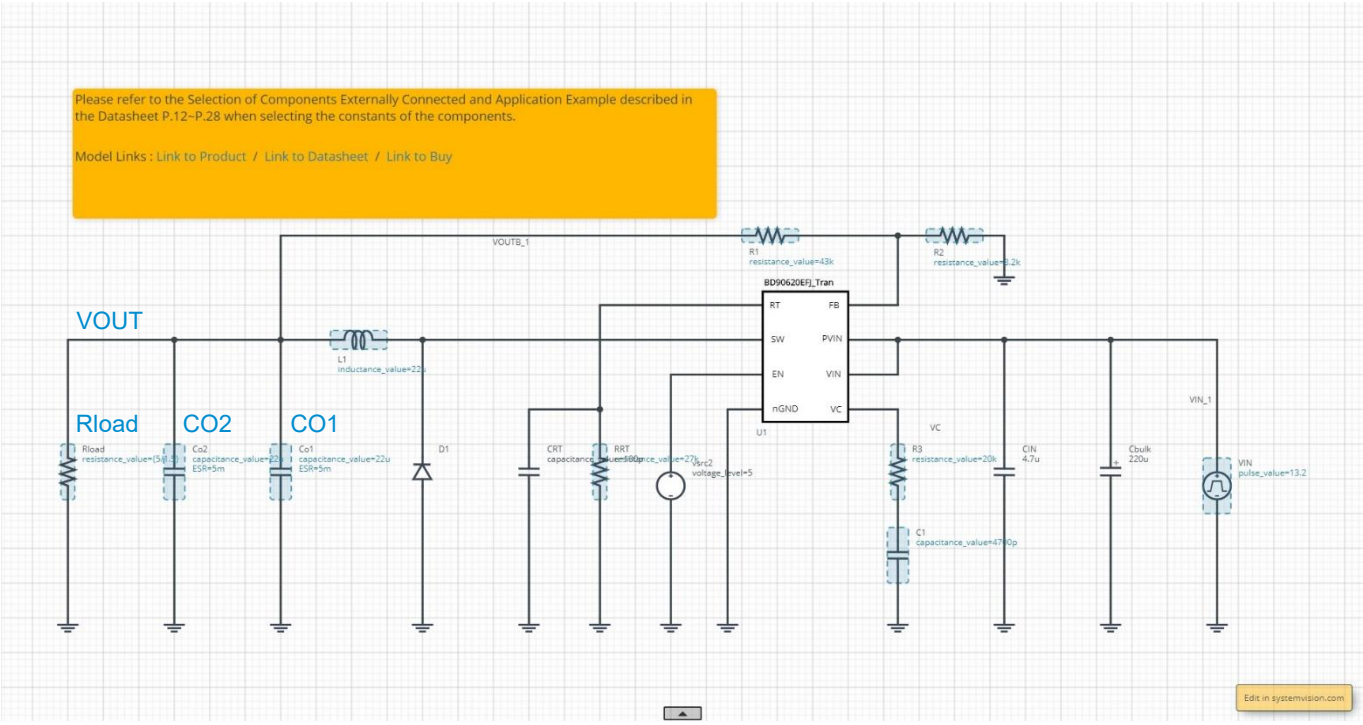
4. Output capacitor

Simulator to be used: ROHM Solution Simulator

Simulation type: Time Domain

External component to be designed: CO1, CO2

Monitoring point: VOUT, CO1



Calculate the ripple voltage.

● The output ripple voltage can be calculated with the following equation.

$$\Delta V_{PP} = \Delta I_L \cdot \mathrm{ESR} + \frac{\Delta I_L}{8 \cdot C_{OUT} \cdot f_{SW}} \quad [V]$$

Where

ΔI_L: Ripple current of the inductor $[A]$

ESR: Equivalent series resistance of the output capacitor $[\Omega]$

C_{OUT}: Capacitance of the output capacitor(NOTE 1) $[F]$

f_{SW}: Switching frequency $[Hz]$

(NOTE 1) The MultiLayer Ceramic Capacitor (MLCC) is decreased from the nominal capacitance due to the DC bias characteristics and the AC voltage characteristics. To simulate accurately, let the property of the capacitor be the actual capacitance of 13.8μF instead of the nominal capacitance of 22μF.

Detailed procedures

4. Output capacitor (continued)

The output ripple voltage is calculated with the actual capacitance of 13.8μF for CO1, CO2. As a guideline, ESR is 2.5mΩ from two 5mΩ capacitors connected in parallel.

$$\Delta V_{PP} = 328mA \times \frac{5m\Omega}{2} + \frac{328mA}{8 \times 13.8\mu F \times 2 \times \ 500kHz} = 3.79 \ mV$$

Calculate the ripple current of the output capacitor.

● The ripple current of the output capacitor can be calculated with the following equation.

$$I_{CO(RMS)} = \frac{\Delta I_L}{\sqrt{12}} \qquad [A_{rms}]$$

Where
ΔI_L: Ripple current of the inductor $[A]$

All Capacitors should be used within its ripple current rating. Substitute inductor ripple current to above equation.

$$I_{CO(RMS)} = \frac{328 \ mA}{\sqrt{12}} = 94.7 \ mA_{rms}$$

The ripple current per capacitor is 47.3mA$_{rms}$ since two capacitors, CO1 and CO2 are connected in parallel in this schematic.

Detailed procedures

4. Output capacitor (continued)

Confirm the maximum value of the output capacitance.

- Operating on the rush current in the startup time, too much capacitance causes output not startup. Whole caps in later stage included CO1, CO2 must be satisfied the inequality.

$$C_{OUT} < \frac{T_{SS(Min)} \cdot \left(I_{SW\ LIMIT(Min)} - I_{SW\ START(Max)}\right)}{V_{OUT}}$$

Where

$T_{SS(Min)}$: Minimum value of the soft start time $= \frac{690.8}{f_{SW}} \times 0.819 \quad [s]$

$I_{SW\ LIMIT(Min)}$: Minimum value of the output switching current of the over current protection $= 2.5$ A

$I_{SW\ START(Max)}$: Maximum value of the load current flowing through the output switch during startup $[A]$

V_{OUT}: Output voltage $[V]$

f_{SW}: Switching frequency $[Hz]$

Substitute the values (of 1.5A $I_{SW\ START\ (Max)}$, et al.) to the inequality, and according to the calculation whole output capacitance must be under 101.8μF.

$$C_{OUT} < \frac{\frac{690.8}{500kHz} \times 0.819 \times (2.5A - 1.5A)}{5V}$$

$$C_{OUT} < 226.3\ \mu F$$

Place the load resistor

- To check the maximum value of the inductor current, set the load current to the maximum value of the design target example. In this example, since the load current is set to 1.5 A, load resistor Rload is 3.33Ω (= 5 V/1.5A).

Optimize simulation time

- It is necessary to set longer time than softstart time that this IC mounts. Setting RRT=27kohm, the softstart time is 1.38ms, and considering output convergence time, set simulation time 4ms.

Detailed procedures

4. Output capacitor (continued)

Perform the simulation.

● Click ▶ to perform the simulation and wait until the simulation is completed.

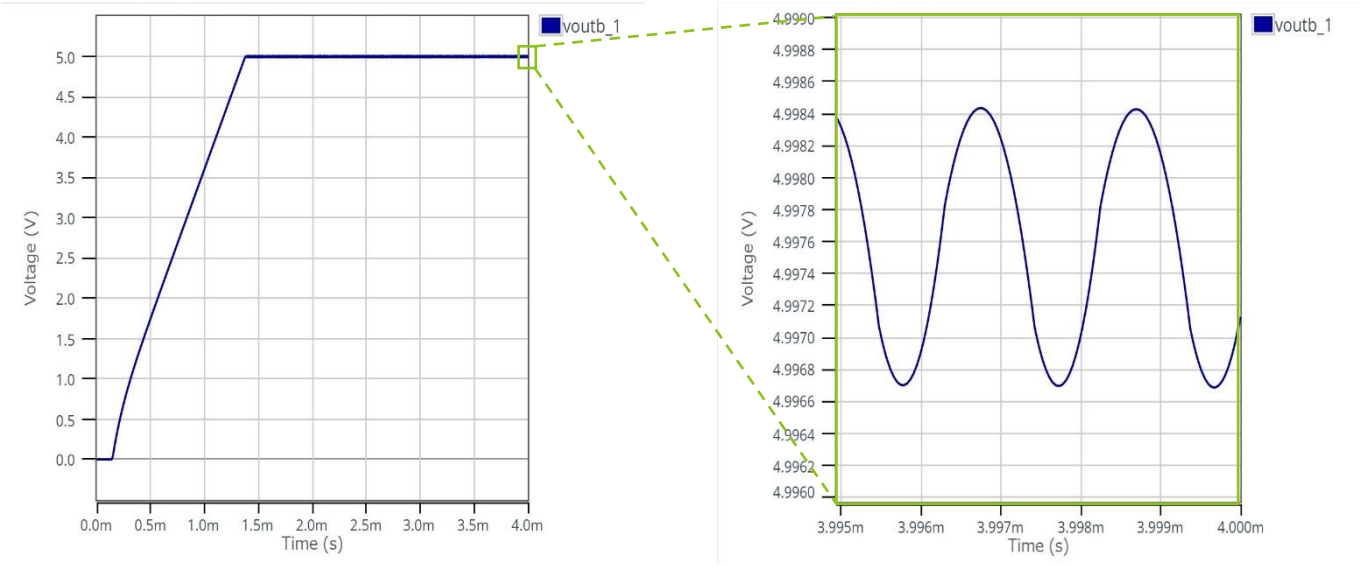
Information	The simulation takes approximately 14 minutes. The time varies with the server usage rate. For Advanced Options, "Balanced" is recommended.

Display the waveform and check the ripple voltage.

1. Drag and drop "Waveform Probe" onto the VOUT in the schematic to display the waveform.

2. Zoom the waveform until you can read the ripple voltage.

3. Display the cursor and read the voltage amplitude.



Detailed procedures

4. Output capacitor (continued)

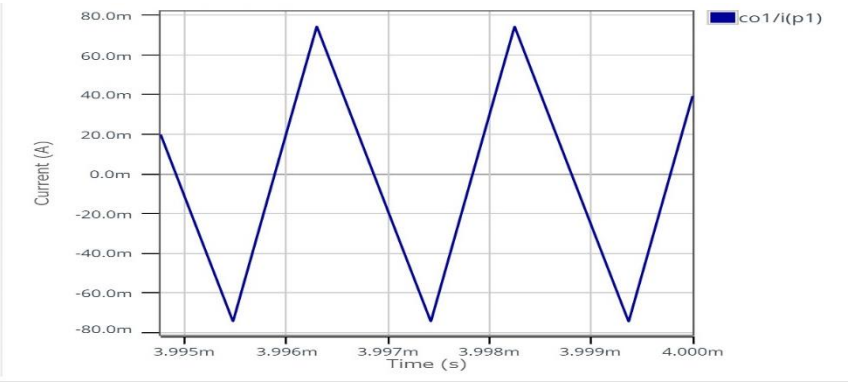
Check the ripple current of the output capacitor.

1. Drag and Drop "Waveform Probe" onto the Co1 symbol in the schematic. Select the current waveform "i (p1)" to be displayed from the dialog.

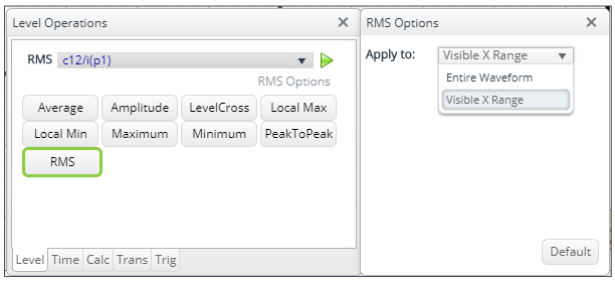
2. Move the cursor onto the waveform and right click there.

3. Select "Plot in Viewer" element in the popup menu.

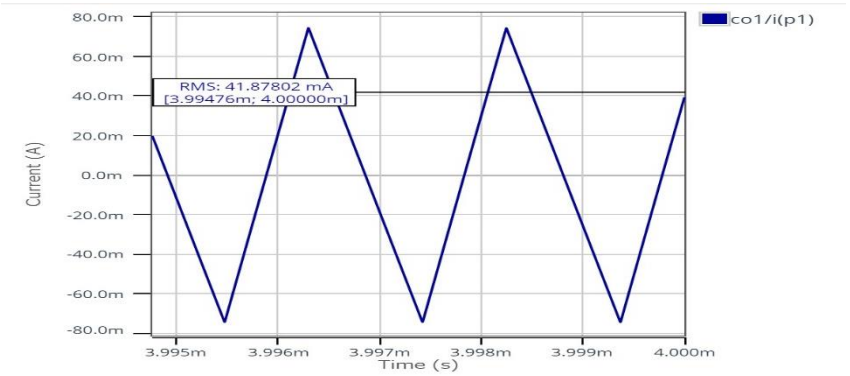
4. Zoom the waveform around the end with the viewer, and click the "Waveform Analyzer" icon on the right.



5. The "Operation window" dialog will be displayed. Click the "RMS" button that appears when the "Level" tab at the bottom is selected. Select "Visible X Range" element included the pull-down menu "Apply to:" in the "RMS Options" dialog that expands to the right. Click ▶ to display the Root Mean Square value (RMS) of the ripple current on the waveform.



6. Make sure that the RMS of ripple current is close to the calculated value.



Detailed procedures

5. Input capacitor

Ripple current of the input capacitor

● The ripple current of the input capacitor becomes maximum when the switching duty ratio is 50%, that is, 1/2 of the input voltage = output voltage.

$$I_{CIN(RMS)} = I_{OUT(Max)} \cdot \frac{\sqrt{V_{OUT} \cdot \left(V_{IN(50\%)} - V_{OUT}\right)}}{V_{IN(50\%)}} \qquad [A_{rms}]$$

Where

$I_{OUT(Max)}$: Maximum current of design parameter example $[A]$

$V_{IN(50\%)}$: Input voltage giving the duty ratio of 50% $= \frac{V_{OUT}}{0.5}$ $[V]$

V_{OUT}: Output voltage $[V]$

All Capacitors should be used within its ripple current rating. Substitute the values of the design parameter example to above equation.

$$I_{CIN(RMS)} = 1.5A \times \frac{\sqrt{5V \times \left(\frac{5V}{0.5} - 5V\right)}}{\frac{5V}{0.5}} = 0.75 \ A_{rms}$$

Detailed procedures

6. Schottky barrier diode

Guideline of the average rectified current

● This product uses a Schottky barrier diode with low forward voltage and short reverse recovery time. The average rectified current flowing in the diode can be calculated by the following equation.

$$I_{F(AVE)} = I_{OUT(Max)} \cdot \frac{V_{IN(Max)} - V_{OUT}}{V_{IN(Max)}} \quad [A]$$

Where
$I_{OUT(Max)}$: Maximum output current of the value of the design parameter example $[A]$
$V_{IN(Max)}$: Maximum input voltage of the value of the design parameter example $[V]$
V_{OUT}: Output voltage $[V]$

As a guideline, the absolute maximum rating of the diode should be 1.2 times or more of the average rectified current calculated above. Substitute the values of the design parameter example to the equation.

$$I_{F(AVE)} = 1.5A \times \frac{18V - 5V}{18V} = 1.08 \text{ A}$$

Absolute maximum rating for the average rectification current of the diode $> I_{F(AVE)} \times 1.2$
Absolute maximum rating for the average rectification current of the diode > 1.30 A $\quad (= 1.08A \times 1.2)$

Dissipate power loss

● When current flows through the diode, a forward voltage is generated, resulting in loss. If you use a product of 0.65V or less, you can reduce loss, increase efficiency, and protect IC internal elements. The following equation is the diode loss calculation.

$$P_{Diode} = I_{OUT(Max)} \cdot \frac{V_{IN(Max)} - V_{OUT}}{V_{IN(Max)}} \cdot V_F \quad [W]$$

Where
$I_{OUT(Max)}$: Maximum output current of the value of the design parameter example $[A]$
$V_{IN(Max)}$: Maximum input voltage of the value of the design parameter example $[V]$
V_{OUT}: Output voltage $[V]$
V_F: Forward voltage of the diode $[V]$

Detailed procedures

6. Schottky barrier diode (continued)

Substitute the forward voltage V_F=0.5V and the value of the design parameter example.

$$P_{Diode} = 1.5A \times \frac{18V - 5V}{18V} \times 0.5\text{V} = 0.54 \text{ W}$$

To withstand overcurrent protection and output short circuit, the absolute maximum rating of the diode should be about 1.5 times the overcurrent detection value as a guideline.

Select the diode from reverse voltage

● As a guideline, the reverse voltage of the diode should be 1.2 times or more the maximum input voltage.

Reverse voltage $> V_{IN(Max)} \times 1.2$

Substitute the values of the design parameter example to the equation.

Reverse voltage > 21.6 V $\quad (= 18V \times 1.2)$

Detailed procedures

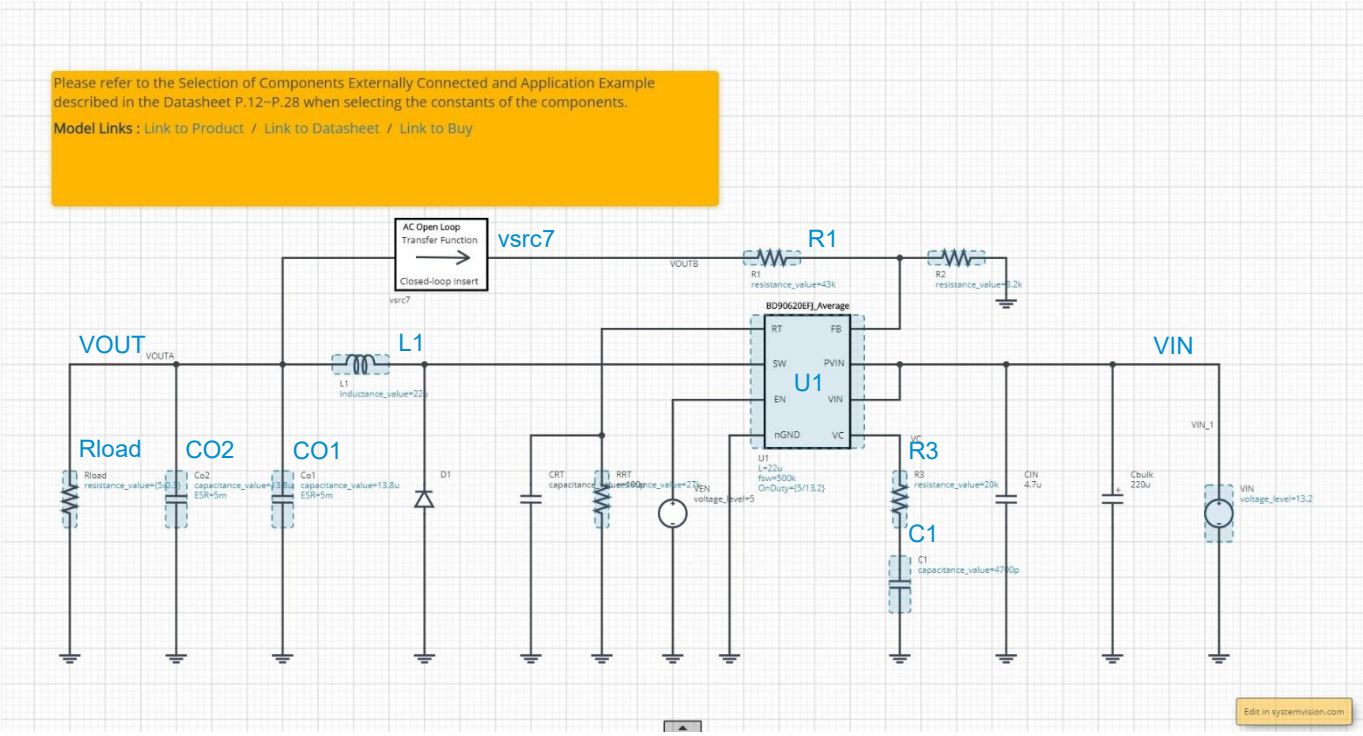
7-1. Phase compensation circuit: Phase margin, gain margin

Simulator to be used: ROHM Solution Simulator

Simulation type: Frequency Domain

External component to be designed: R3, C1, CO1, CO2

Monitoring point: vsrc7



The zero-cross frequency fc of the loop gain improve the frequency response, but reduce the stability due to the phase delay. Since opposite is also true, it can be said that the two have a trade-off relationship. The switching regulator is sampling at the switching frequency. As a guideline, set the zero-cross frequency fc to 1/10 or less of the switching frequency fsw in order to suppress the gain during sampling and stabilize the system.

Phase compensation is made with the system including R3 and C1 connected to the VC pin. The phase delay due to the two poles fp1, fp2 is canceled by the phase lead due to zero fz1. Only for introduction, another zero fz2 can be inserted for increasing the zero-cross frequency to the high frequency range and ensuring the phase margin. Inserting C2 in parallel with feedback resistor R1 in this way is called lead compensation, and stability can be improved.

The phase margin and zero cross frequency, Gain Margin will be checked later by simulation.

Detailed procedures

7-1. Phase compensation circuit: Phase margin, gain margin (continued)

Cancel the pole with zero

● The frequency of two poles (phase delay) and two zeros (phase lead) is calculated by the following equation.

$$f_{P1} = \frac{1}{2\pi \cdot C_{OUT} \cdot R_{load}} \quad [Hz]$$

$$f_{P2} = \frac{G_{EA}}{2\pi \cdot C1 \cdot A_V} \quad [Hz]$$

$$f_{Z1} = \frac{1}{2\pi \cdot R3 \cdot C1} \quad [Hz]$$

$$(f_{Z2} = \frac{1}{2\pi \cdot R1 \cdot C2} \quad [Hz])$$

Where

C_{OUT}: Capacitance of the output capacitor(NOTE 1) $[F]$

R_{load}: Load resistance $[\Omega] = \frac{\text{Output voltage } [V]}{\text{Load current } [A]}$ (1)

G_{EA}: Transconductance of the error amplifier $= 270\ [\mu A/V]$

A_V: Voltage gain of the error amplifier $= 7943\ (= 78\ dB)$

(NOTE 1) The MultiLayer Ceramic Capacitor (MLCC) is decreased from the nominal capacitance due to the DC bias characteristics and the AC voltage characteristics. To simulate accurately, let the property of the capacitor be the actual capacitance of 13.8μF instead of the nominal capacitance of 22μF.

● Substitute the values of the design parameter example into the equation. For the output capacitors Co1 and Co2, use the MLCC mentioned in the example of NOTE1. The load resistance R_{load} is obtained from Ohm's law (1). Check the phase margin and gain margin with two patterns that substitute the output voltage and the minimum load current or the maximum load current into this law.

When the load current is at the minimum$(= 0.3\ A)$, $f_{P1} = \frac{1}{2\pi \cdot C_{OUT} \cdot R_{OUT}} = \frac{1}{2\pi \times 13.8\mu F \times 2 \times \frac{5V}{0.3A}} = 346\ Hz$

When the load current is at the maximum$(= 1.5\ A)$, $f_{P1} = \frac{1}{2\pi \cdot C_{OUT} \cdot R_{OUT}} = \frac{1}{2\pi \times 13.8\mu F \times 2 \times \frac{5V}{1.5A}} = 1.73k\ Hz$

$$f_{P2} = \frac{G_{EA}}{2\pi \cdot C1 \cdot A_V} = \frac{270}{2\pi \times 4700pF \times 7943} = 1.15\ MHz$$

$$f_{Z1} = \frac{1}{2\pi \cdot R3 \cdot C1} = \frac{1}{2\pi \times 20k\Omega \times 4700pF} = 1.69\ kHz$$

$$(f_{Z2} = \frac{1}{2\pi \cdot R1 \cdot C2} = \frac{1}{2\pi \times 43k\Omega \times 180pF} = 20.6\ kHz)$$

Detailed procedures

7-1. Phase compensation circuit: Phase margin, gain margin (continued)

Input IC properties

● Input the values from the design parameter example and from the constant of external part to the three properties needed this product U1.

1. Parameter L: Input the value of inductor L1
2. Parameter fsw: Input the value of design parameter example
3. Parameter OnDuty: Input OnDuty ratio= output voltage / input voltage

Optimize simulation frequency range

● In order to observe the whole Bode plot of this product, simulation is performed from "Start Frequency" 0.01Hz and to "End Frequency" 1Meg Hz.

Perform the simulation.

● Click ▶ to perform the simulation and wait until the simulation is completed.

Information	The simulation takes approximately 20 seconds. The time varies with the server usage rate. For Advanced Options, "Balanced" is recommended.

Detailed procedures

7-1. Phase compensation circuit: Phase margin, gain margin (continued)

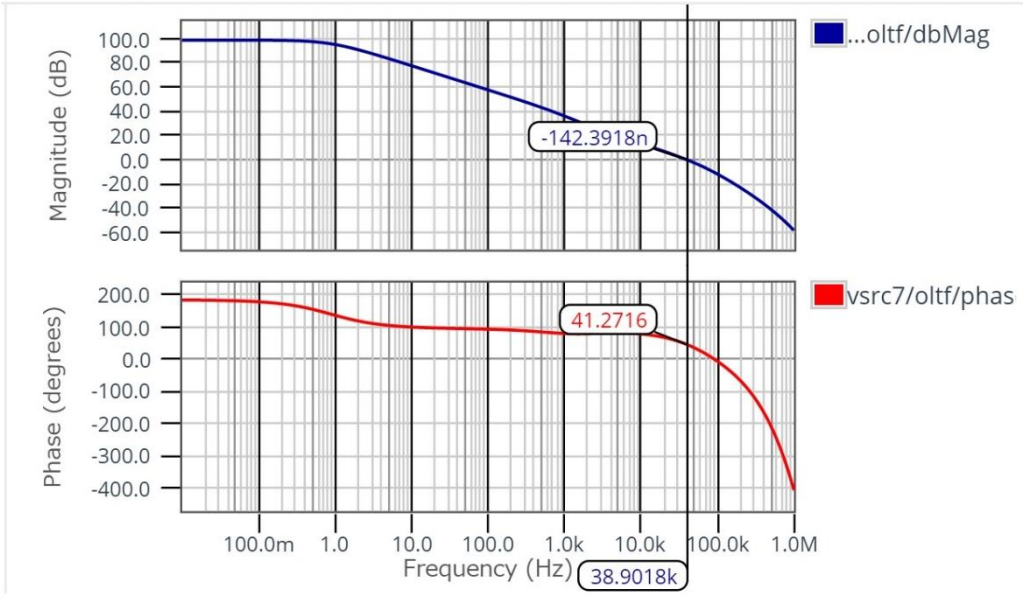
Display the characteristics and check the values.

1. 1. After simulation, the amplitude and phase characteristics are drawn on the graph displayed on the initial screen. If you close the graph, redisplay it by the following procedure.
   a. Drag and drop "Waveform Probe" onto the symbol of vsrc7 in the circuit diagram.
   b. When the waveform dialog box is opened, go to folder vsrc7 and then oltf. Then, select "dbMag" to display the amplitude characteristics.
   c. Drag and drop the probe symbol at the lower left on the graph onto the symbol of vsrc7 again.
   d. When the waveform dialog box is opened, go to folder vsrc7 and then oltf. Then, select "phase" to display the phase characteristics.
2. Right-click on the graph and select "Multi Trace" in "Display Mode" from the pop-up menu. The amplitude characteristics and the phase characteristics are displayed on the top and bottom graphs, respectively.
3. Right-click on the graph and select "Add Cursor" from the popup menu to display the cursor.
4. Move the cursor to the frequency where the amplitude characteristic becomes 0. In practice, the resolution of the simulation set the value close to 0. At this time, the value displayed on the frequency axis is the zero-cross frequency.
5. The value displayed on the phase characteristics on the zero cross frequency is the phase margin.

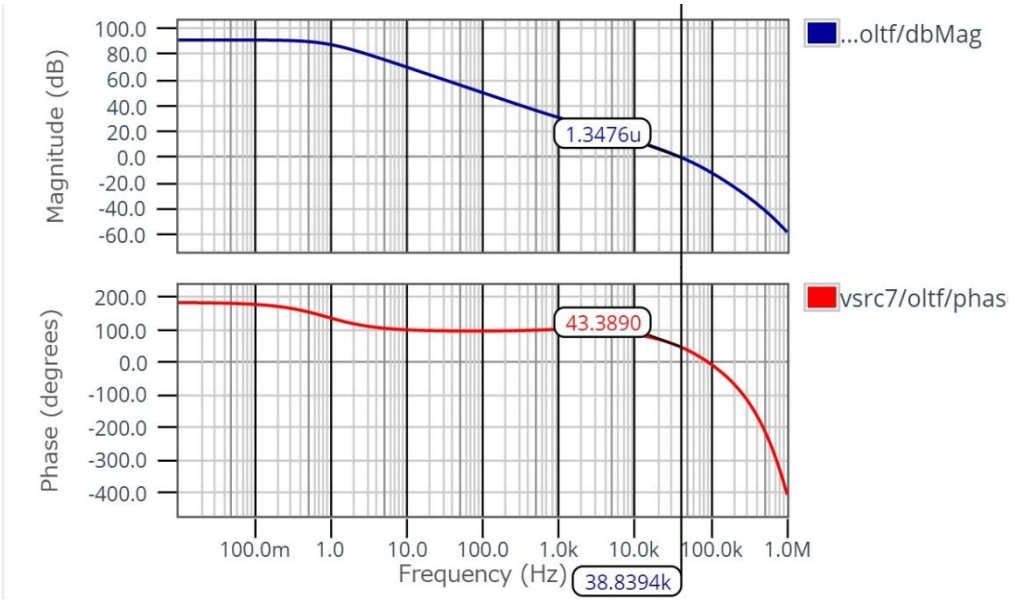
Detailed procedures

7-1. Phase compensation circuit: Phase margin, gain margin (continued)

Zero cross frequency and phase margin at minimum load current (=0.3A)



Zero cross frequency and phase margin at maximum load current (= 1.5A)



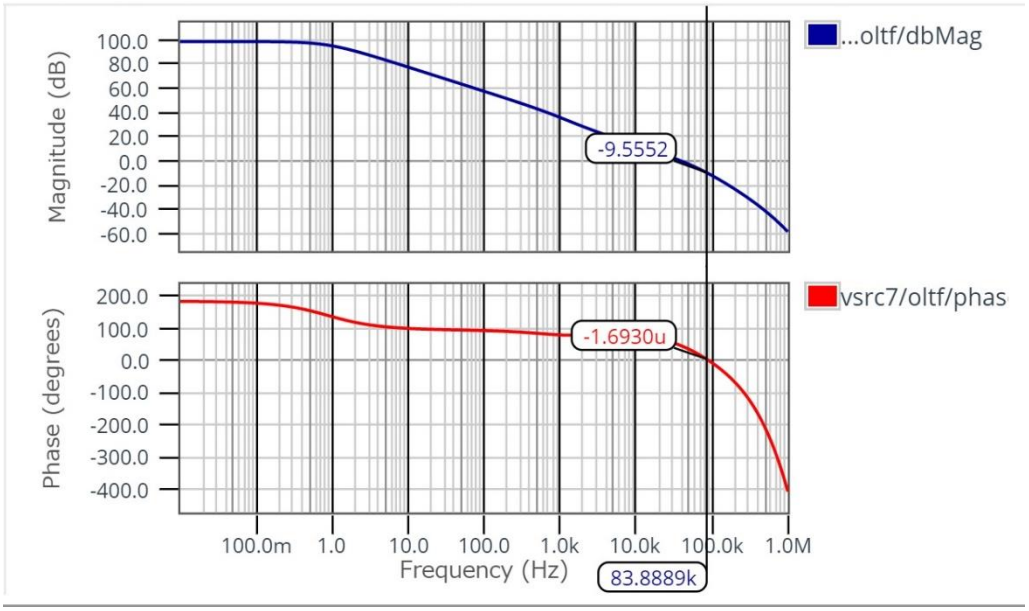
Detailed procedures

7-1. Phase compensation circuit: Phase margin, gain margin (continued)

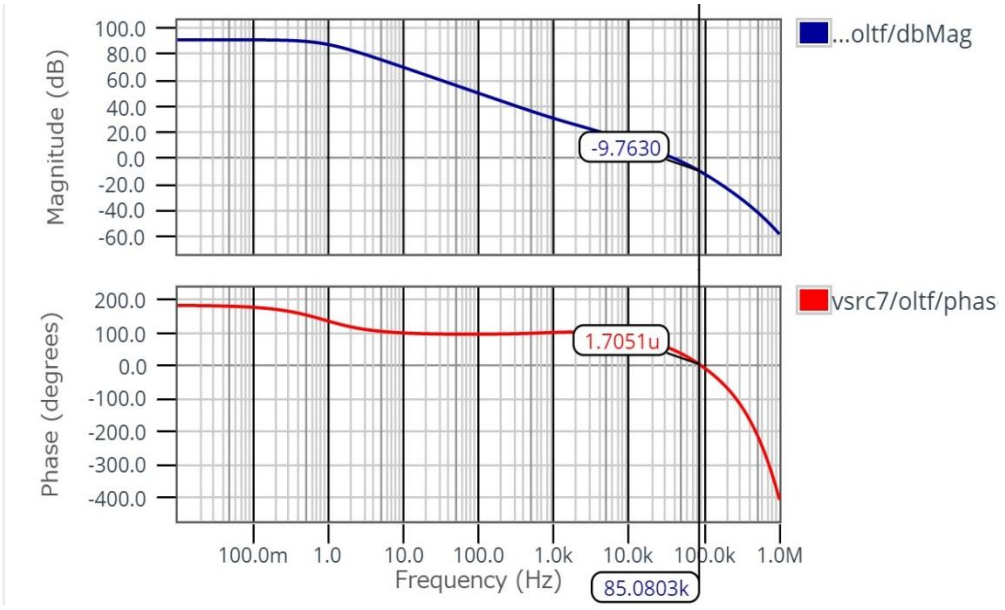
7. Next, move the cursor to the frequency where the phase characteristic becomes 0. In practice, the resolution of the simulation set the value close to 0.

8. The value displayed on the amplitude characteristic on the frequency is the gain margin.

Gain margin at minimum load current (=0.3A)



Gain margin at maximum load current (= 1.5A)



Detailed procedures

7-1. Phase compensation circuit: Phase margin, gain margin (continued)

Stable operation satisfying the standard conditional inequality

● Once the pole and zero frequencies satisfy the following inequality, it can be judged that stable operation is achieved.

1. $0.5\ f_{P1} \leq f_{Z1} \leq\ 5\ f_{P1}$

   When the load current is at the minimum$(= 0.3\ A)$, $173\ Hz\ \leq\ 1.69\ kHz\ \leq\ 1.73\ kHz$
   When the load current is at the maximum$(= 1.5\ A)$, $865\ Hz\ \leq\ 1.69\ kHz\ \leq\ 8.65\ kHz$

   The standard conditional inequality is satisfied. In detail, the stable operation can be achieved if all following three requirements are met.

For introduction, insert f_{Z2} to the schematic.

2. $0.5\ f_C \leq f_{Z2} \leq\ 2\ f_C$

   When the load current is at the minimum $(= 0.3\ A)$, $19.5\ kHz\ \leq\ 20.6\ kHz \leq\ 77.8\ kHz$
   When the load current is at the maximum $(= 1.5\ A)$, $19.4\ kHz\ \leq\ 20.6\ kHz \leq\ 77.7\ kHz$

   The standard conditional inequality is satisfied.

Meet requirements and operate stably

● Stable operation will be achieved if the following three requirements are met by substituting the values of design parameter example.

1. Zero cross frequency $f_C < \frac{Switching\ \ frequency\ \ f_{SW}}{10}$

   When the load current is at the minimum $(= 0.3\ A)$, $38.9\ kHz < 50\ kHz$

   When the load current is at the maximum $(= 1.5\ A)$, $38.8\ kHz < 50\ kHz$

   It is checked that this requirement is satisfied.

2. Phase margin: The typical value shall be 45° or more, and the worst value shall be 30° or more.

   When the load current is at the minimum (= 0.3 A), 41.3° > 30°

   When the load current is at the maximum (= 1.5 A), 43.4° > 30°

   It is checked that this requirement is satisfied.

3. Gain margin: The typical value shall be -10 dB or less, and the worst value shall be -6 dB or less.

   When the load current is at the minimum (= 0.3 A), -9.56dB < -6dB

   When the load current is at the maximum (= 1.5 A), -9.76dB < -6dB

   It is checked that this requirement is satisfied.

Detailed procedures

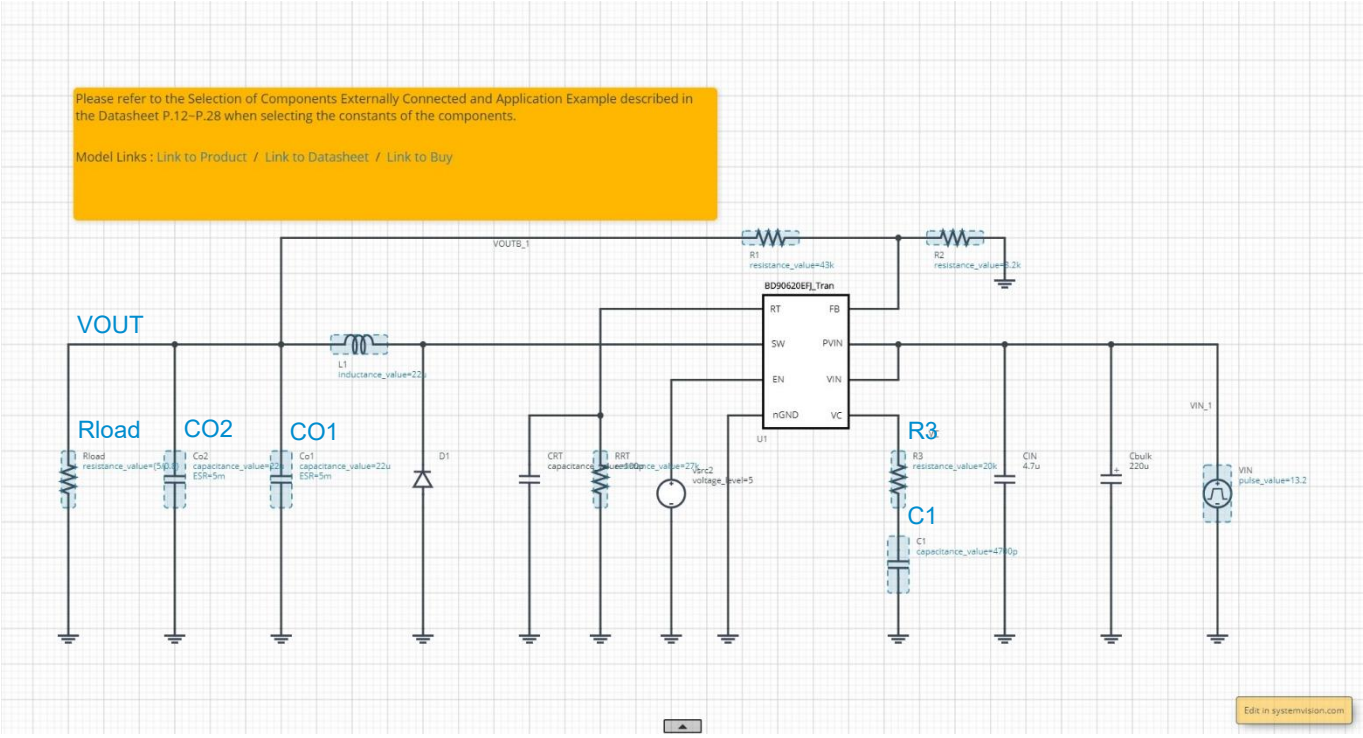
7-2. Phase compensation circuit: Load transient response

Simulator to be used: SystemVision®Cloud

Simulation environment and type: SystemVision®Cloud Time Domain

External component to be designed: R3, C1, CO1, CO2

Monitoring point: VOUT



Open the circuit diagram for Time Domain from the ROHM Solution Simulator. To perform the simulation of the load transient response, a variable current source is required for the load. Since the circuit diagram cannot be changed in the ROHM Solution Simulator environment, move to the SystemVision®Cloud environment to conduct the procedure. As shown in the figure above, clicking the [Edit in systemvision.com] button on the circuit diagram in the ROHM Solution Simulator environment allows you to access the SystemVision®Cloud environment, where you can edit the circuit diagrams and perform the simulations.

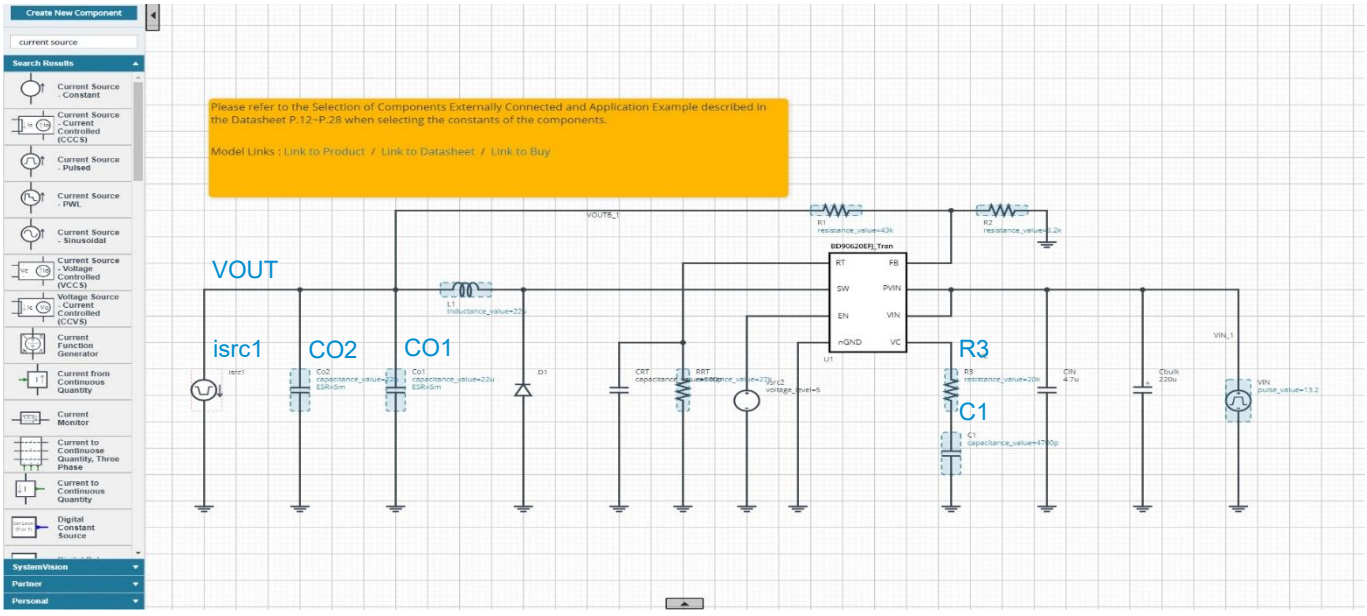
Detailed procedures

7-2. Phase compensation circuit: Load transient response (continued)

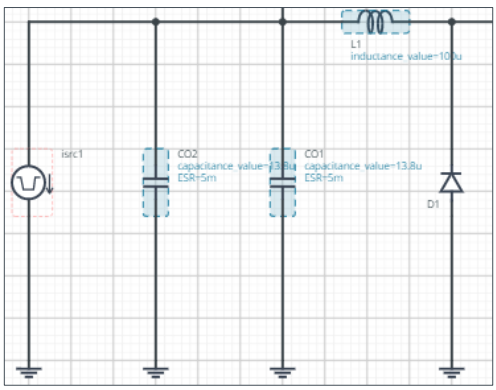
Change schematic

- When moving to SystemVision®Cloud, the parameters of each element are set to the initial values, so change them to the values designing so far.
- The procedure to replace the load resistance Rload with a pulse current source to check the load transient response is as follows.

1. When you move to SystemVition®Cloud, the menu related to components is displayed on the left side of the schematic.
2. Input "current source" in "Search Components" to display a list of current sources.
3. Press the delete key to delete selected load resistance Rload.
4. Drag and drop "Current Source - Pulsed" from the list at the location where Rload was and connect to the schematic.



5. This current source isrc1 is arranged so that current flows from GND to the IC. To let the current flow from the IC to GND, click "Flip Vertical" that appears when you click the current source (or you can place original flow and set the property negative).

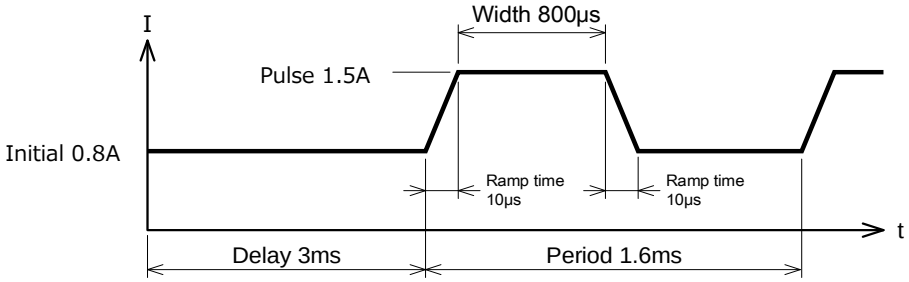


Detailed procedures

7-2. Phase compensation circuit: Load transient response (continued)

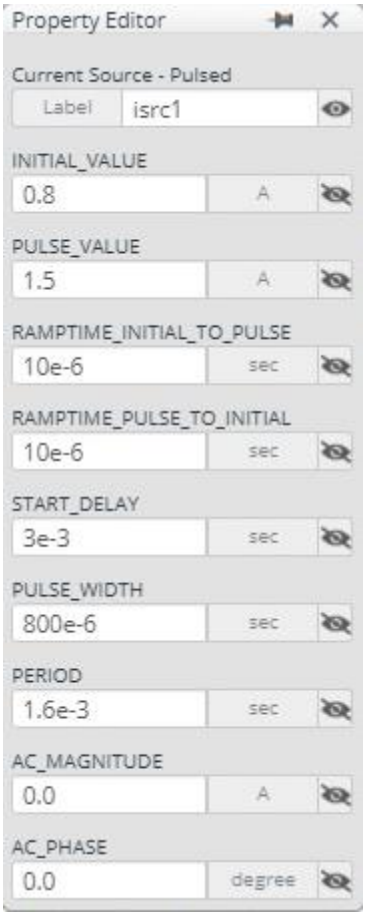
Input the load current properties

- The pulse current source isrc1 is changed transiently as shown below. Double-click isrc1 to display its properties. Input each value according to the waveform.



Example of the load current

Property values



Detailed procedures

7-2. Phase compensation circuit: Load transient response (continued)

Optimize simulation time.

- It is necessary to set longer time than softstart time that this IC mounts. Setting RRT=27kohm, the softstart time is 1.38ms, considering output convergence time and transient time, set simulation time 4ms.

Display the waveform and read the fluctuation value

- Click ▶ to perform the simulation and wait until the simulation is completed.

Information	The simulation takes approximately 12 minutes. The time varies with the server usage rate. For Advanced Options, "Balanced" is recommended.

Display the waveform and check the load fluctuation voltage.

1. Drag and drop "Waveform Probe" onto the VOUT in the circuit diagram to display the voltage waveform.

2. Select i (p1) (i (p2) if the "Current Source - Pulsed" is not flipped vertically) from the list to display the load current waveform.

3. To observe the fluctuation due to load transient response, zoom the x-axis from 2.8ms to 4ms and the y-axis from 4.9V to 5.1V.

4. Right-click on the graph and select "Add Cursor" from the popup menu to display the cursor.

5. Place the cursor at the steady state around 2.8ms, at the minimum value of undershoot, and at the maximum value of overshoot.

6. The undershoot rate (a) and overshoot rate (b) obtained from the cursor values satisfy the values of the design parameter example.

(A) The amount of undershoot relative to the output voltage is expressed as follows.

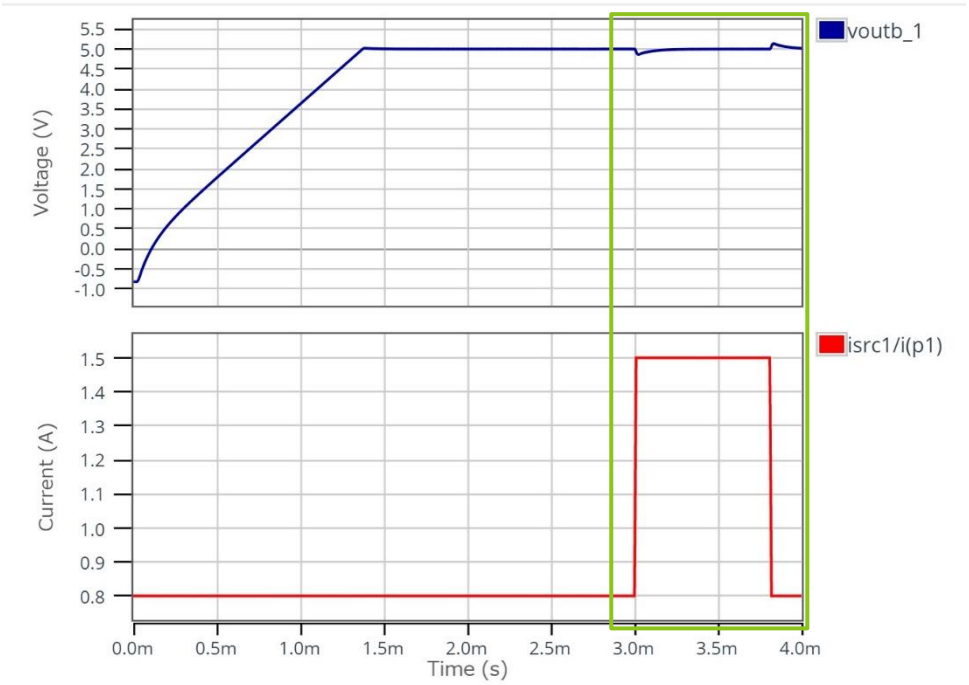
(4.8602 V - 4.9970 V)/4.9970 V × 100 = -2.74%

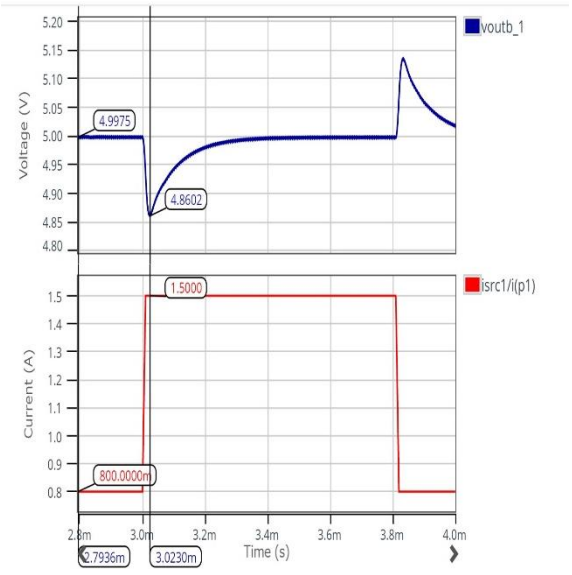
(B) The amount of overshoot relative to the output voltage is expressed as follows.

(5.1350 V - 4.9970 V)/4.9970 V × 100 = +2.76%

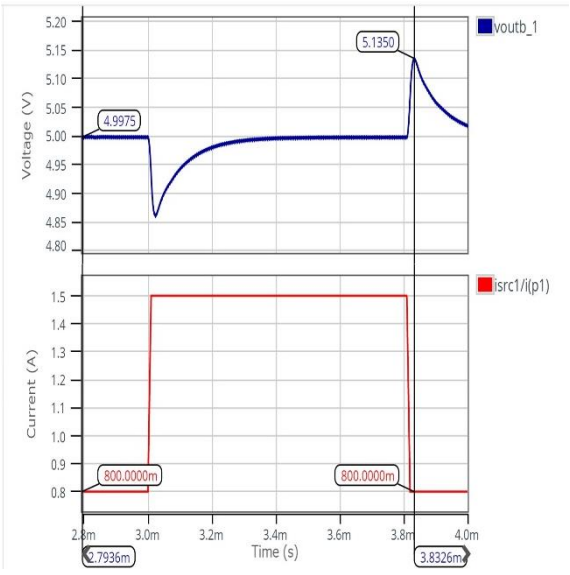
Detailed procedures

7-2. Phase compensation circuit: Load transient response (continued)





Check the undershoot



Check the overshoot

Detailed procedures

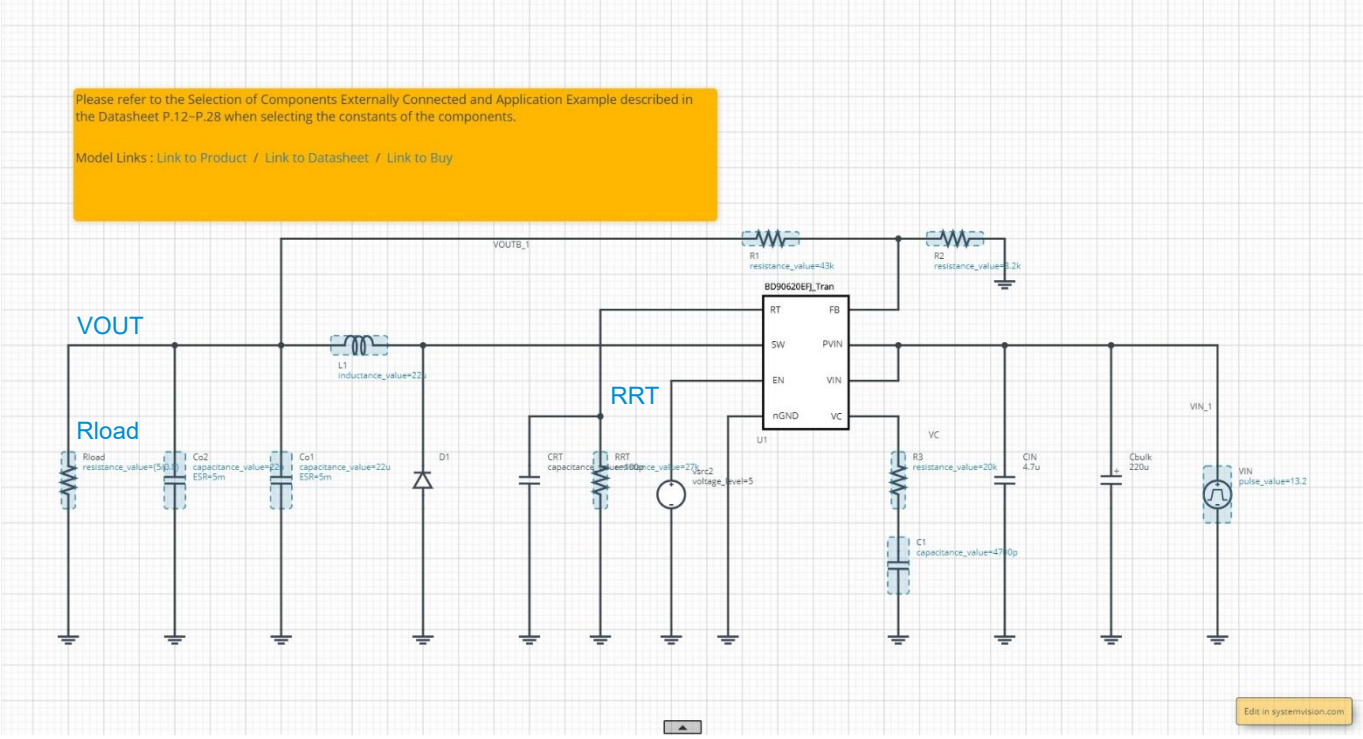
8. Soft start

Simulator to be used: ROHM Solution Simulator

Simulation type: Time Domain

External component to be designed: RRT

Monitoring point: VOUT



Calculate the soft start time.

- The soft start time is calculated by the following formula using the switching frequency. The variation is ±18.1%. The switching frequency is determined by RRT as described before. For details, refer to the "Switching frequency" section.

$$T_{SS} = \frac{690.8}{f_{SW}} \quad [s]$$

Substituting 500kHz according to the value of the design parameter example to the equation, the softstart time is 1.38ms.

$$T_{SS} = \frac{690.8}{500\ kHz} = 1.38\ \text{m} \quad [s]$$

Detailed procedures

8. Soft start (continued)

Place the load resistor

● The load resistance is calculated with the output voltage and the output current according to Ohm's law.

$$I_{LOAD} = \frac{V_{OUT}}{Rload} \quad [A]$$

Substituting the output voltage 5V, and the standard current 0.8A from the values of the design parameter example, the load resistance is 6.25Ω.

$$R_{Load} = \frac{5}{0.8A} = 6.25 \quad [\Omega]$$

Optimize simulation time

● It is necessary to set longer time than softstart time that this IC mounts. Setting RRT=27kohm, the softstart time is 1.38ms, and considering output convergence time, set simulation time 4ms. The advantage is that it can perform simultaneously with other simulations.

Perform the simulation.

● Click ▶ to perform the simulation and wait until the simulation is completed.

Information	The simulation takes approximately 14 minutes. The time varies with the server usage rate. For Advanced Options, "Balanced" is recommended.

Detailed procedures

8. Soft start (continued)

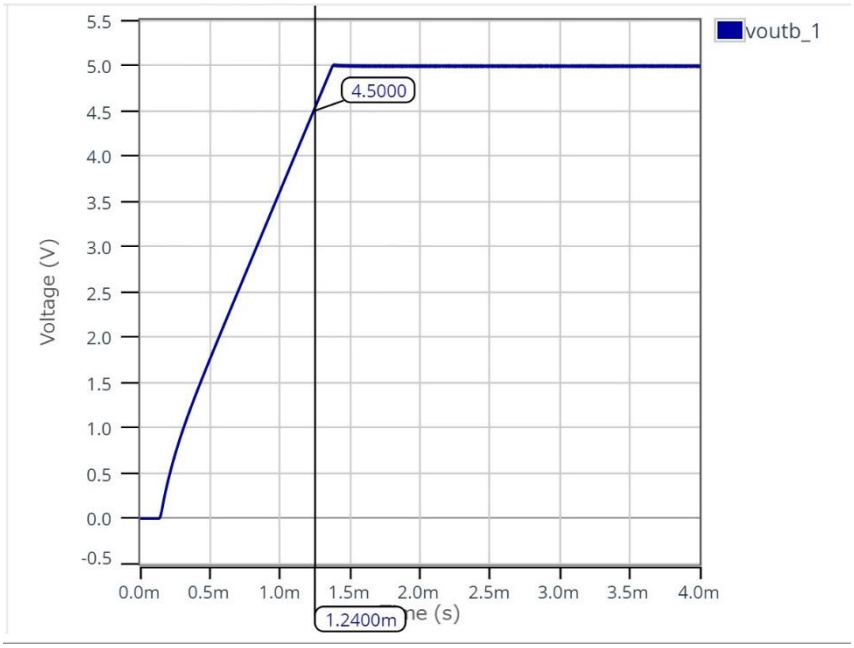
Display the waveform and read the voltage value with the cursor.

1. Drag and drop "Waveform Probe" onto the VOUT in the circuit diagram to display the waveform.

2. Right-click on the graph and select "Add Cursor" from the popup menu to display the cursor.

3. Move the cursor to the voltage 4.5V that multiply 90% by 5V of the value of the design parameter example. In practice, there is a limit to the resolution of the simulation, and we tune to the voltage closest to 4.5V.

4. X-axis of the cursor is softstart time, and met the design value.



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