Application Note

ROHM Switching Regulator Solutions

Evaluation Board for ROHM's BD9109FVM Synchronous Buck DC/DC Converter with Integrated FET

BD9109FVMEVK-101 (3.3V | 0.8A Output)

USAP58-A-0004

- **Introduction**

This application note will explain the steps necessary to operate and evaluate ROHM's BD9109FVM synchronous buck DC/DC converter using the BD9109FVMEVK-101 evaluation board. Component selection, board layout recommendations, operating procedures, and application data are included.

- **Description**

This evaluation board has been specifically developed to evaluate the BD9109FVM synchronous buck DC/DC converter with integrated 350mΩ Pch and 250mΩ Nch MOSFETs. Features include an input voltage range of 4.5V to 18.0V, 3.3V output, and a switching frequency of 1MHz. Multiple protection functions are also built in, including a soft start circuit that prevents inrush current during startup, UVLO (Under Voltage Lock Out), TSD (Thermal Shutdown), OCP (Over Current Protection), and timer latch short-circuit protection. An EN pin allows for simple ON/OFF control to reduce standby current consumption, while current mode PWM provides fast response to sudden load changes.

- **Applications**

Power supplies for ICs, including DSPs, MCUs, and ASICs

- **Evaluation Board Operating Limits and Absolute Maximum Ratings**

Parameter		Symbol	Limit			Unit	Conditions
			MIN	TYP	MAX		
Supply Voltage							
	BD9109FVM	V_{CC}	4.5	5	5.5	V	
Output Voltage / Current							
	BD9109FVM	V_{OUT}	3.234	3.300	3.366	V	
		I_{OUT}	-	-	0.8	A	

- **Evaluation Board**

Below is an image of the BD9109FVMEVK-101 evaluation board.

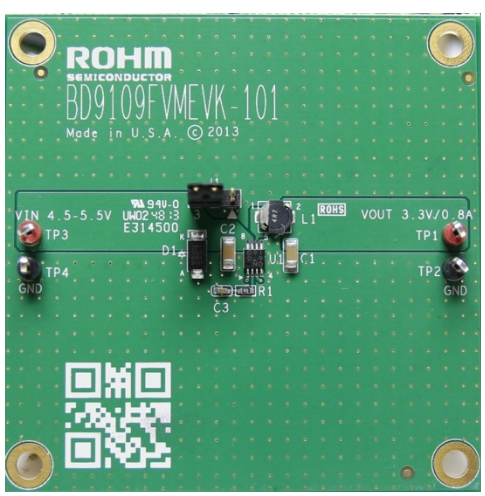

Fig 1: BD9109FVMEVK-101 Evaluation Board

- **Board Schematic**

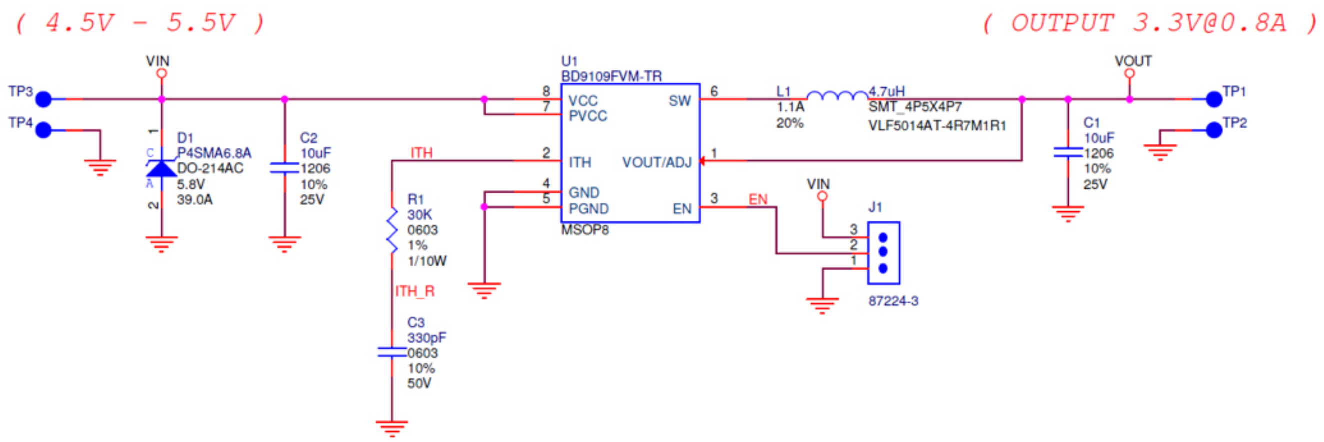

Fig 2: BD9109FVMEVK-101 Evaluation Board Schematic

- **Board I/O**

Below is a reference application circuit showing the inputs V_{IN}, EN and output V_{OUT}.

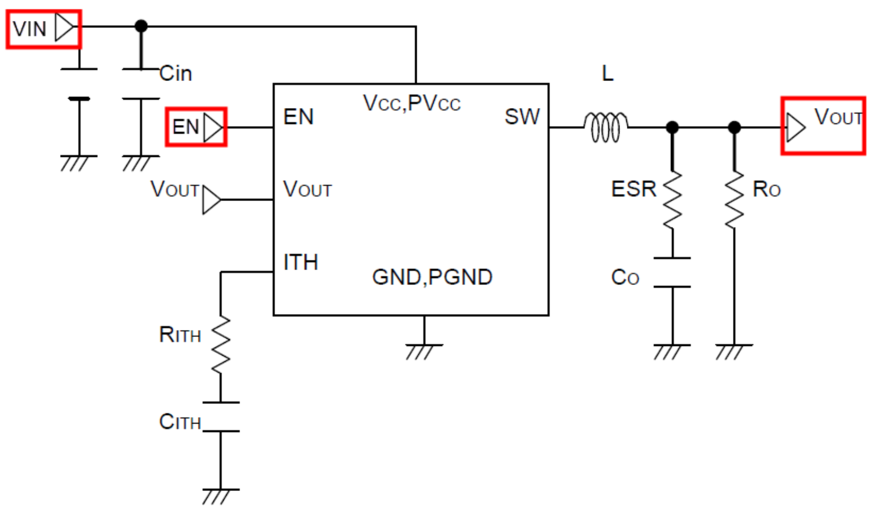

Fig 3: Evaluation Board I/O

- **Operating Procedures**

1. Connect the power supply's GND terminal to GND test point TP4 on the evaluation board.
2. Connect the power supply's V_{CC} terminal to V_{IN} test point TP3 on the evaluation board. This will provide V_{IN} to the IC U1. Please note that V_{CC} should be in the range from 4.5V to 5.5V.
3. Check that the shunt jumper J1 is in the ON position (connect Pin 2 to Pin 3, the EN pin of IC of U1 is pulled high as a default).
4. Now the output voltage V_{OUT} (+3.3V) can be measured at test point TP1 on the evaluation board with a load attached. The load can be increased up to 0.8A MAX.

- **Reference Application Data**
  The following are graphs of the hot plugging test, quiescent current, efficiency, load response, and output voltage ripple response of the BD9109FVMEVK-101 evaluation board.

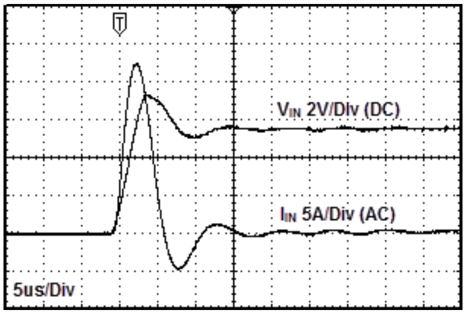

Fig 4: Hot Plug-in Test with Zener Diode SMAJ5.0A, V_{IN}=5.5V, V_{OUT}=3.3V, I_{OUT}=0.8A

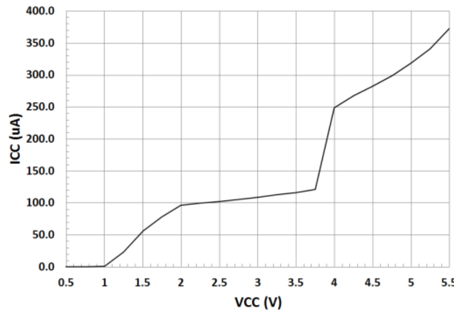

Fig 5: Circuit Current vs. Power Supply Voltage (Temp=25°C)

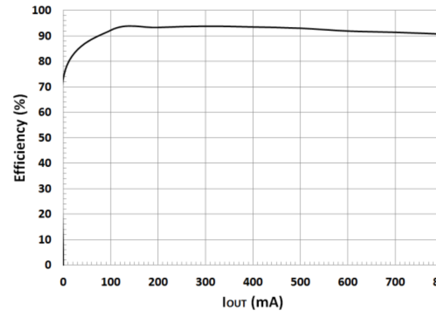

Fig 6: Electric Power Conversion Rate (V_{OUT}=3.3V)

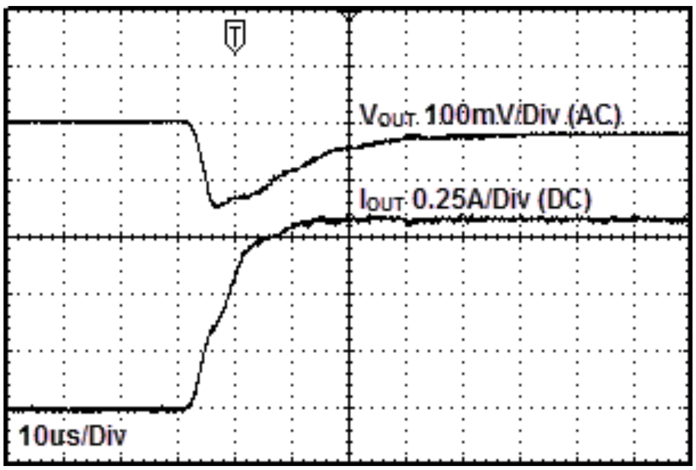

Fig 7: Load Response Characteristics (V_{IN}=5V, V_{OUT}=3.3V, L=4.7uH, C_{OUT}=10uF, I_{OUT}=0A→0.8A)

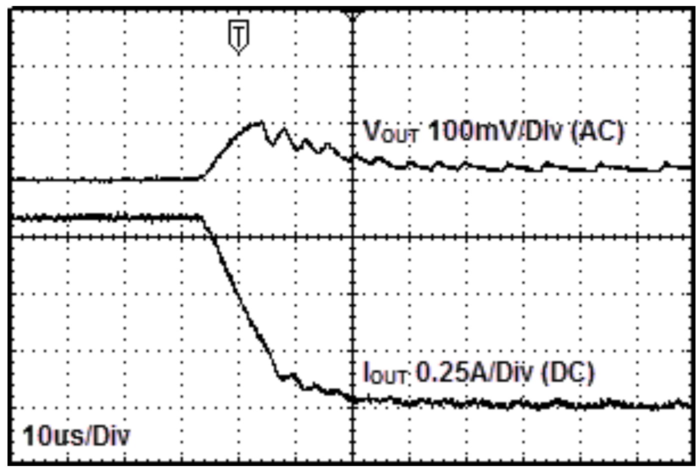

Fig 8: Load Response Characteristics (V_{IN}=5V, V_{OUT}=3.3V, L=4.7uH, C_{OUT}=10uF, I_{OUT}=0.8A→0A)

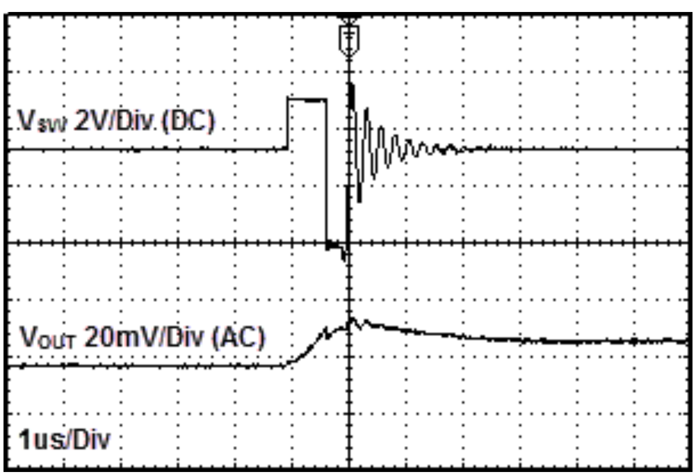

Fig 9: Output Voltage Ripple Response Characteristics (V_{IN}=5V, V_{OUT}=3.3V, L=4.7uH, C_{OUT}=10uF, I_{OUT}=0A)

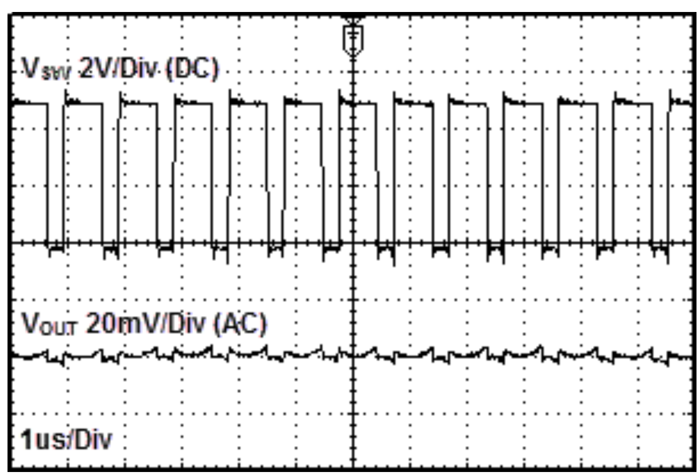

Fig 10: Output Voltage Ripple Response Characteristics (V_{IN}=5V, V_{OUT}=3.3V, L=4.7uH, C_{OUT}=10uF, I_{OUT}=0.8A)

- **Evaluation Board Layout Guidelines**

  Below are guidelines that have been tested and recommended for BD9109FVM designs.
  Layout is a critical element of good power supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductances and parasitic capacitances to generate noise or degrade power supply performance. To help eliminate these problems, the V_{CC} pin should be bypassed to ground with a low ESR ceramic bypass capacitor with B dielectric.

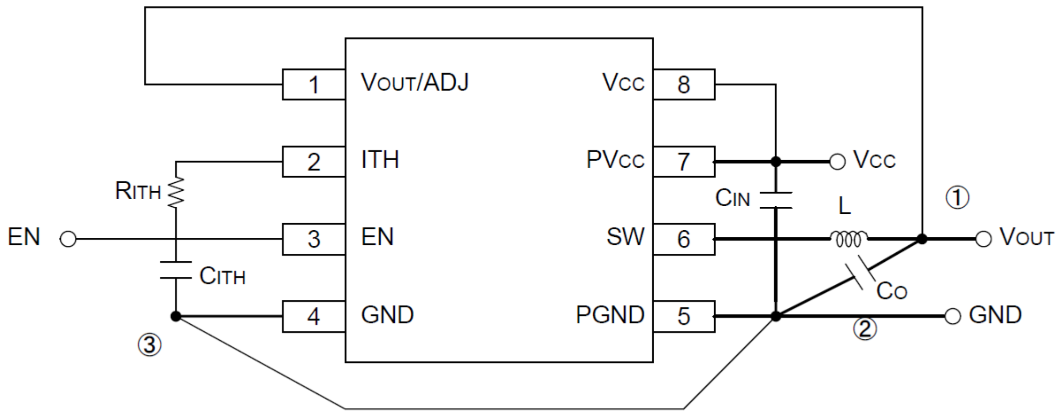

Fig 11: BD9109FVM Layout Diagram

① For the areas drawn with a heavy line, use a thick conductor pattern and make it as short as possible.
② Lay out the input ceramic capacitor C_{IN} closer to the pins PVCC and PGND and the output capacitor C_O closer to the PGND pin.
③ Connect C_{ITH} and R_{ITH} between the pins ITH and GND as cleanly as possible with the least amount of wiring.

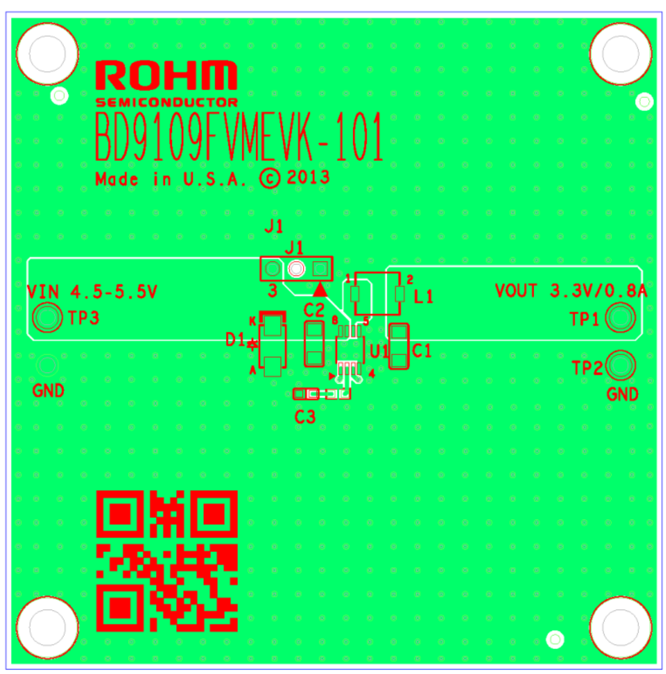

Fig 12: BD9109FVMEVK-101 PCB Layout

• Application Circuit Component Selection

1. Inductor (L)

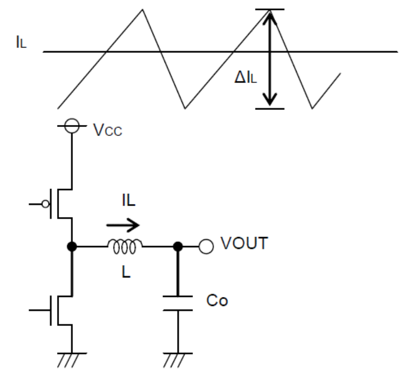

Fig 13: Output Ripple Current

The inductance has a significant effect on the output ripple current.
As seen in the equation (1) below, the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{L \times V_{CC} \times f} \ [A] \qquad (1)$$

The appropriate ripple current at output should be 30% of the maximum output current.

$$\Delta I_L = 0.3 \times I_{OUT\ MAX} \ [A] \qquad (2)$$

$$L = \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{CC} \times f} \ [H] \qquad (3)$$

(Where ΔIL is the Output Ripple Current and f is the Switching Frequency)

* Current exceeding the current rating of the inductor will result in magnetic saturation of the inductor, decreasing efficiency.
The inductor must be selected to allow sufficient margin so that the peak current does not exceed the rated current of the coil.

For example, if VCC=5V, VOUT=3.3V, f=1MHz, and ΔIL=0.3x0.8A=0.24A:

$$L = \frac{(5-3.3) \times 3.3}{0.24 \times 5 \times 1M} = 4.675[uH] \rightarrow 4.7[uH]$$

* Select an inductor with low resistance component (such as DCR and ACR) to minimize inductor loss and improve efficiency.

2. Output Capacitor (C_O)

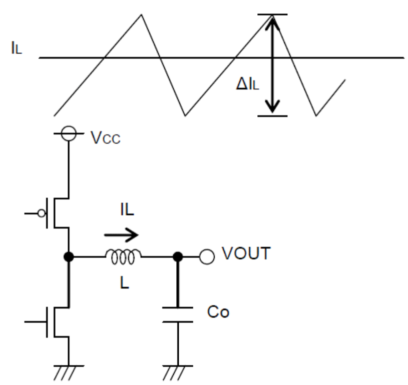

Fig 14: Output Capacitor

The output capacitor should be selected taking into consideration the output voltage stability region and the equivalent series resistance required to smooth the ripple voltage. The output ripple voltage is determined by:

$$\Delta V_{OUT} = \Delta I_L \times ESR \ [V] \quad (4)$$

(Where ΔIL is the Output Ripple Current and ESR is the Equivalent Series Resistance of the output capacitor)

* The capacitor rating should be determined to allow sufficient margin against output voltage. The lower the ESR the lower the output ripple voltage.

As the output rise time must be set to fall within the soft-start time, the capacitance of the output capacitor should be calculated taking into account the conditions of the equation (5) below:

$$C_O \leq \frac{T_{SS} \times (I_{LIMIT} - I_{OUT})}{V_{OUT}} \ [F] \qquad (5)$$

[Where t_{SS} is the Soft Start time and I_{LIMIT} is the Overcurent Detection level (2A typ.)]

For instance, if V_{OUT}=3.3V, I_{OUT}=0.8A, and T_{SS}=1ms:

$$C_O \leq \frac{1m \times (2-0.8)}{3.3} = 364[uF]$$

Please note that inappropriate capacitance may cause problems during startup. A 10uF to 100uF ceramic capacitor is recommended.

3. Input Capacitor (C_{IN})

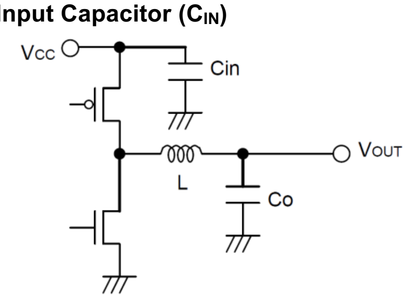

Fig 15: Input Capacitor

A low ESR input capacitor with sufficient size to handle large ripple current in order to prevent large transient voltages is required. The ripple current I_{RMS} can be calculated by:

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{CC} - V_{OUT})}}{V_{CC}} \ [A] \qquad (6)$$

< Worst Case > $I_{RMS(max.)}$

When VCC is twice V_{OUT}, $I_{RMS} = \frac{I_{OUT}}{2}$

If V_{CC}=5V, V_{OUT}=3.3V, and $I_{OUT\ max}$=0.8A,

$$I_{RMS} = 0.8 \times \frac{\sqrt{3.3(5-3.3)}}{5} = 0.38[A]$$

Therefore, a low ESR 10uF/10V ceramic capacitor is recommended to reduce ESR loss of the input capacitor to improve efficiency.

4. Phase Compensation Circuit R_{ITH}, C_{ITH}

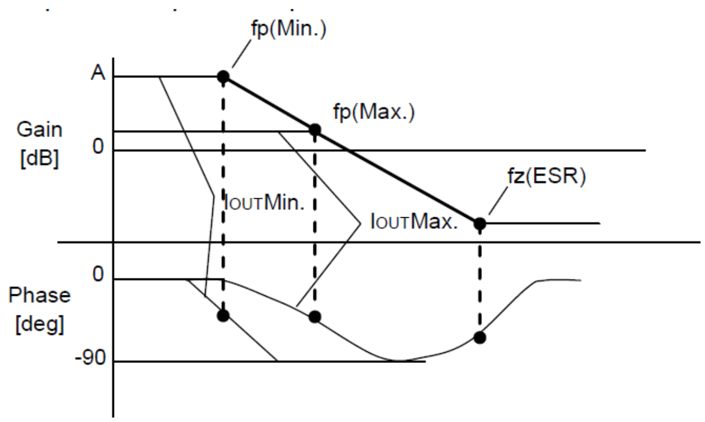

Fig 16: Open Loop Gain Characteristics

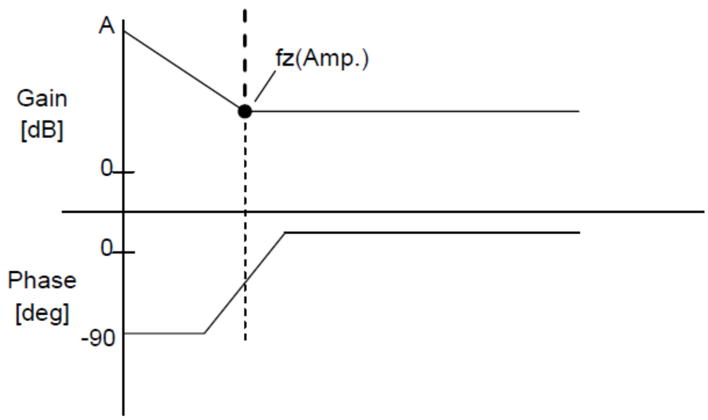

Fig 17: Error Amp Phase Compensation Characteristics

With current mode control, since the inductor current is restricted, a pole (phase lag) appears in the low-frequency region due to the CR filter made up of an output capacitor and load resistor, while a zero (phase lead) appears in the high-frequency region due to the output capacitor and ESR. Compensation in order to cancel the pole of the power amplifier can easily be achieved by adding a zero point using a C and R at the error amp output as described below.

$$\mathbf{fp} = \frac{1}{2\pi \times Ro \times Co}$$

$$\mathbf{fz\ (ESR)} = \frac{1}{2\pi \times ESR \times Co}$$

Pole at the power amplifier

When the output current decreases, the load resistance R_O increases and the pole frequency is reduced.

$$\mathbf{fp\ (Min.)} = \frac{1}{2\pi \times Romax \times Co}$$ [Hz] ← At lighter loads

$$\mathbf{fp\ (Max.)} = \frac{1}{2\pi \times Romin \times Co}$$ [Hz] ←At heavier loads

Zero at the power amplifier

Increasing the capacitance of the output capacitor reduces the pole frequency while the zero frequency does not change. (This is because when the capacitance doubles, the capacitor ESR is reduced by half.)

$$\mathbf{fz\ (Amp)} = \frac{1}{2\pi \times R_{ITH} \times C_{ITH}}$$

Stable feedback loop can be achieved by canceling the pole fp (Min.) produced by the output capacitor and load resistance with the CR zero correction of the error amplifier.

fx (Amp) = fp (Min)

$$\rightarrow \frac{1}{2\pi \times R_{ITH} \times C_{ITH}} = \frac{1}{2\pi \times Romax \times Co}$$

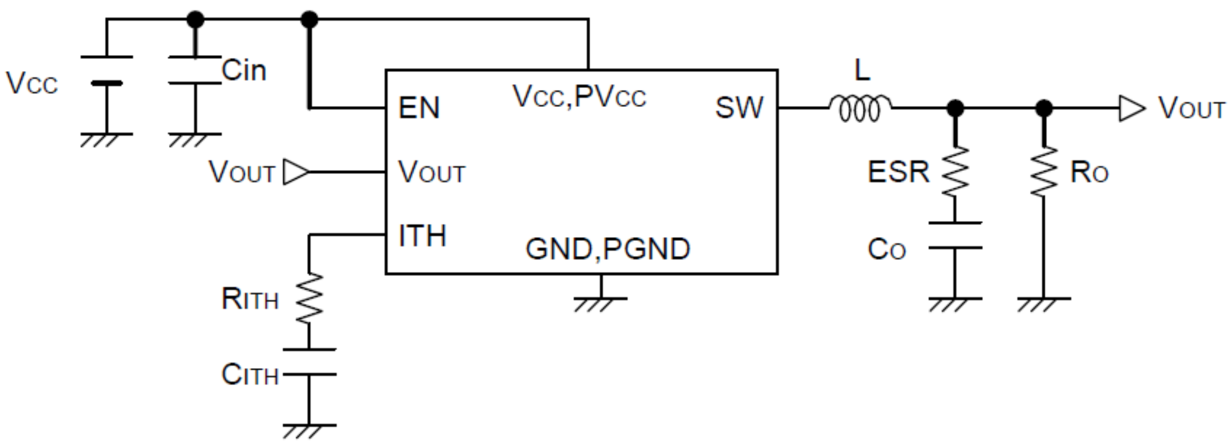

Fig 18: Typical Application Circuit

- **Evaluation Board BOM**
  Below is a table showing the bill of materials. Part numbers and supplier references are also provided.

No.	Qty.	Ref	Description	Manufacturer	Part Number
1	2	C1,C2	CAP CER 10UF 25V 20% X5R 1206	Murata	GRM31CR61E106MA12L
2	1	C3	CAP CER 330PF 50V 10% X7R 0603	Murata	GRM188R71H331KA01D
3	1	D1	DIODE TVS 400W 6.8V UNI 5% SMD	Littelfuse	P4SMA6.8A
4	1	J1	CONN HEADER VERT .100 3POS 15AU	TE Connectivity	87224-3
5	1	L1	INDUCTOR POWER 4.7UF 1.1A SMD	TDK Corporation	VLF5014AT-4R7M1R1
6	1	R1	RES 30K OHM 1/10W 1% 0603 SMD	Rohm	MCR03ERTF3002
7	2	TP1,TP3	TEST POINT PC MULTI PURPOSE RED	Keystone Electronics	5010
8	2	TP2,TP4	TEST POINT PC MULTI PURPOSE BLK	Keystone Electronics	5011
9	1	U1	IC REG BUCK SYNC 3.3V 0.8A 8MSOP	ROHM	BD9109FVM-TR
10	1		Shunt jumper for header J1 (item #4), CONN SHUNT 2POS GOLD W/HANDLE	TE Connectivity	881545-1

Notes

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