ROHM Switching Regulator Solutions

Evaluation Board for ROHM's BD9D321EFJ Synchronous Buck Converter with Integrated FET

BD9D321EFJ-E2EVK-101 (1.8V | 3A Output) USAP58-A-0003

- **Introduction**

This application note will explain the steps necessary to operate and evaluate ROHM's BD9D321EFJ synchronous buck DC/DC converter using the BD9D321EFJ-E2EVK-101 evaluation board. Component selection, board layout recommendations, operating procedures, and application data are included.

- **Description**

This evaluation board has been specifically developed to evaluate the BD9D321EFJ synchronous buck DC/DC converter with integrated 100mΩ high-side Pch and 70mΩ low-side Nch MOSFETs. Features include a wide input voltage range (4.5V to 18.0V), 1.8V output, and a switching frequency of 700kHz. Multiple protection functions are also built in, including a fixed Soft Start circuit that prevents inrush current during startup, UVLO (Under Voltage Lock Out), TSD (Thermal Shutdown), OCP (Over Current Protection), and SCP (Short-Circuit Protection). An EN pin allows for simple ON/OFF control to reduce standby current consumption.

- **Applications**

Step-Down Power Supplies for DSPs FPGAs, and MCUs
Set-Top Boxes
LCD TVs
DVD / Blu-ray Players / Recorders
Entertainment Devices

- **Evaluation Board Operating Limits and Absolute Maximum Ratings**

Parameter		Symbol	Limit			Unit	Conditions
			MIN	TYP	MAX		
Supply Voltage							
	BD9D321EFJ	V_{CC}	4.5	-	18.0	V	
Output Voltage / Current							
	BD9D321EFJ	V_{OUT}	-	1.8	-	V	
		I_{OUT}	-	-	3	A	

- **Evaluation Board**

Below is an image of the BD9D321EFJ-E2EVK-101 evaluation board.

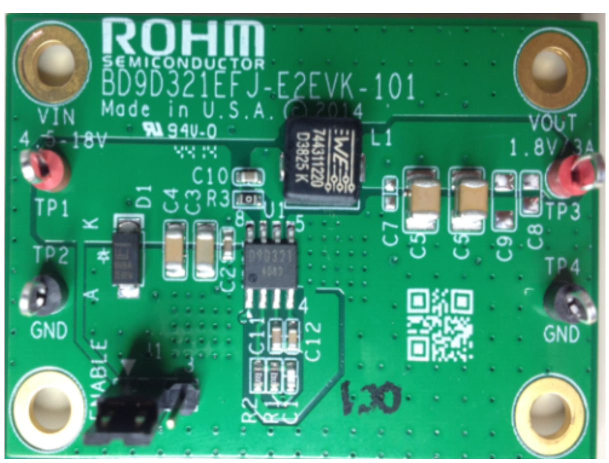
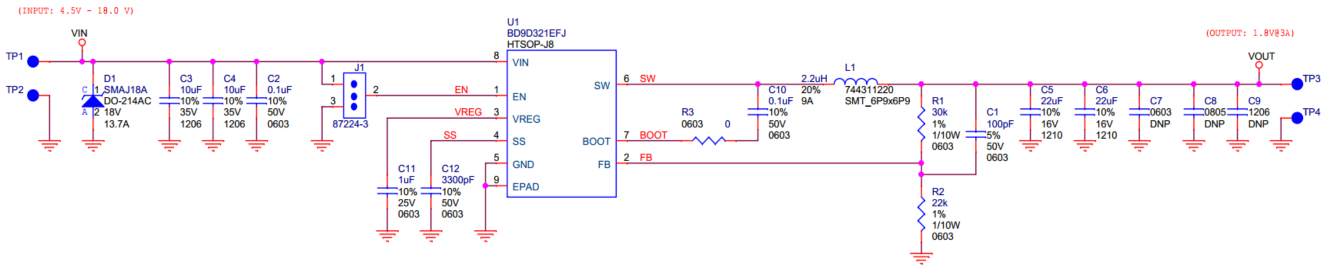


Fig 1: BD9D321EFJ-E2EVK-101 Evaluation Board

- **Board Schematic**



BD9D321EFJ EVM Jumper Positions

Reference Designator	Position	Description
J1	2 - 1	Enable U1
	2 - 3	Disable U1

VOUT = 0.765*(R1+R2)/R2

Note:

1. 0.07xVIN =< VOUT =< 0.65xVIN

Fig 2: BD9D321EFJ-E2EVK-101 Evaluation Board Schematic

- **Board I/O**

Below is a reference application circuit showing the inputs V_{IN} and EN and output V_{OUT}.

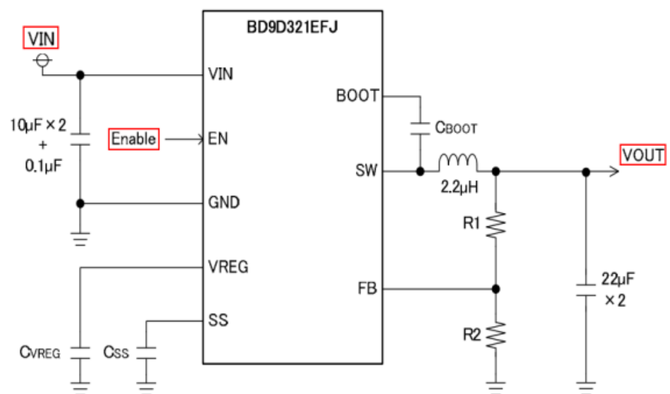


Fig 3: Evaluation Board I/O

- **Operating Procedures**

1. Connect the power supply's GND terminal to GND test point TP2 on the evaluation board.
2. Connect the power supply's V_{CC} terminal to V_{IN} test point TP1 on the evaluation board. This will provide V_{IN} to the IC U1. Please note that V_{CC} should be in the range from 4.5V to 18V.
3. Check that the shunt jumper J1 is in the ON position (connect Pin2 to Pin1, the EN pin of IC U1 is pulled high).
4. Connect the electronic load to TP3 and TP4. Do not turn the load ON (the electronic load is powered OFF).
5. Turn the power supply ON. The output voltage V_{OUT} (+1.8V) can be measured at test point TP3. Now turn the load ON. The load can be increased up to 3A max.

Notes: *DO NOT perform hot plugging on this board, since the inrush current (I_{IN_MAX} >=65A) will exceed the clamping range of SMAJ series diodes (I_{PP}=20A@V_C=20V). These diodes cannot suppress the voltage glitch over the maximum input voltage rating (20V) of the BD9D321EFJ, preventing the IC from being protected against hot plugging. Please refer to Figure 4.*

- **Reference Application Data**
  The following are graphs of the hot plugging test, quiescent current, efficiency, load response, and output voltage ripple response of the BD9D321EFJ-E2EVK-101 evaluation board.

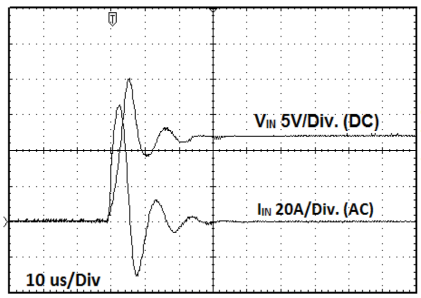


Fig 4: Hot Plug-in Test with Zener Diode SMAJ18A, V_{IN}=12V, V_{OUT}=1.8V, I_{OUT}=3A,

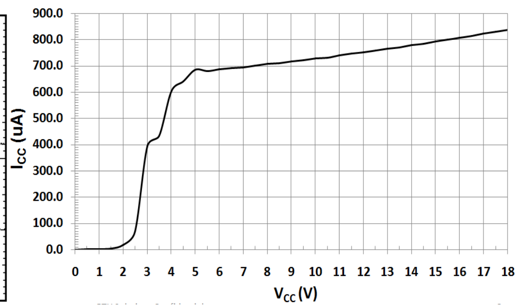


Fig 5: Circuit Current vs. Power Supply Voltage (Temp=25°C)

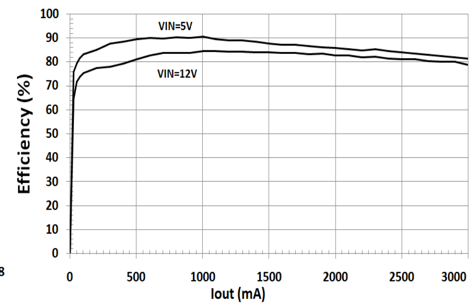


Fig 6: Electric Power Conversion Rate (V_{OUT}=1.8V)

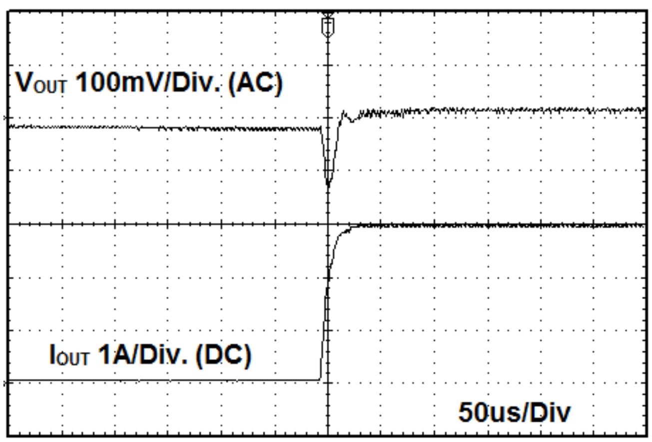


Fig 7: Load Response Characteristics (V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0→3A)

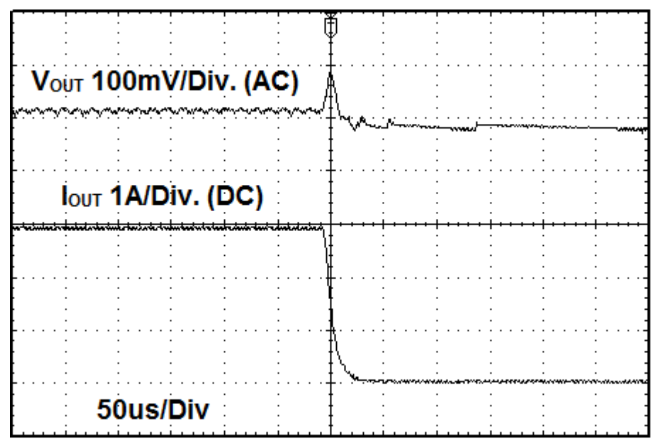


Fig 8: Load Response Characteristics (V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=3A→0A)

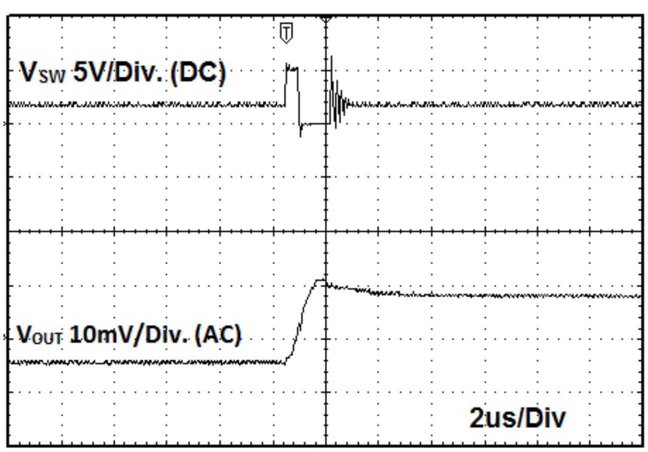


Fig 9: Output Voltage Ripple Response Characteristics (V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0A)

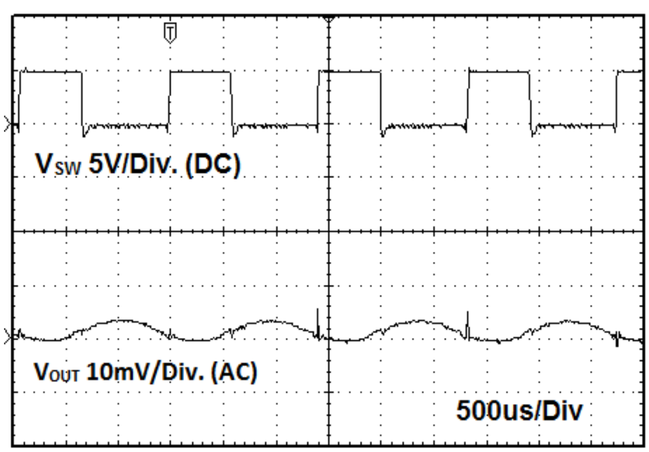


Fig 10: Output Voltage Ripple Response Characteristics (V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=3A)

- **Evaluation Board Layout Guidelines**

In the step-down DC/DC converter, a large pulse current flows through two loops. The first loop is the one into which current flows when the high-side FET is turned ON. The flow starts from the input capacitor C_{IN}, runs through the FET, inductor L and output capacitor C_{OUT}, then back to the ground of C_{IN} via the ground of C_{OUT}. In the second loop current flows when the low-side FET is turned ON. The flow starts from the low-side FET, runs through the inductor L and output capacitor C_{OUT}, then back to the ground of the low-side FET via the ground of C_{OUT}. We recommend routing these two loops as thick and as short as possible to minimize noise and improve efficiency. The input and output capacitors should be connected directly to the ground plane. Please note that the PCB layout has a large influence on the DC/DC converter in terms of heat generation, noise, and efficiency.

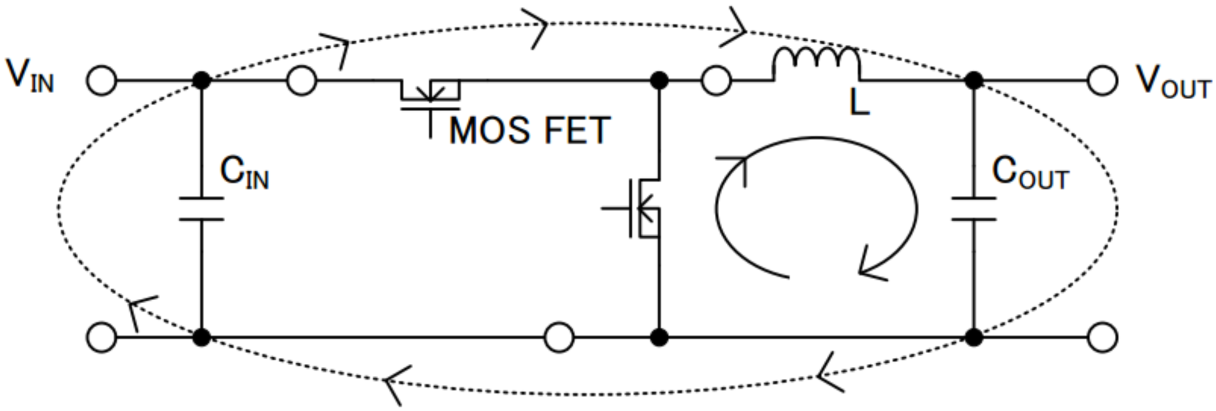
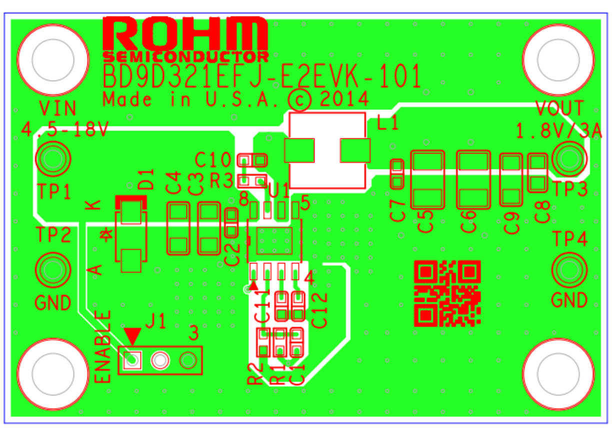
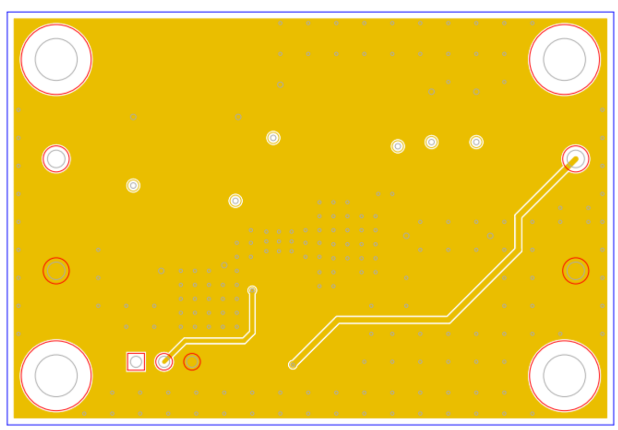


Fig 11: Current Loop of Buck Converter

Accordingly, when designing the PCB layout please consider the following points.

- Connect an input capacitor as close as possible to the IC V_{IN} terminal on the same plane as the IC.
- If there is any unused area on the PCB, provide a copper foil plane for the ground node to assist heat dissipation from the IC and the surrounding components.
- Switching nodes such as SW are susceptible to noise due to AC coupling with other nodes. Route the coil pattern as thick and as short as possible.
- Ensure that lines connected to FB and SS are far from the SW nodes.
- Place the output capacitor away from the input capacitor in order to avoid the effects of harmonic noise from the input.

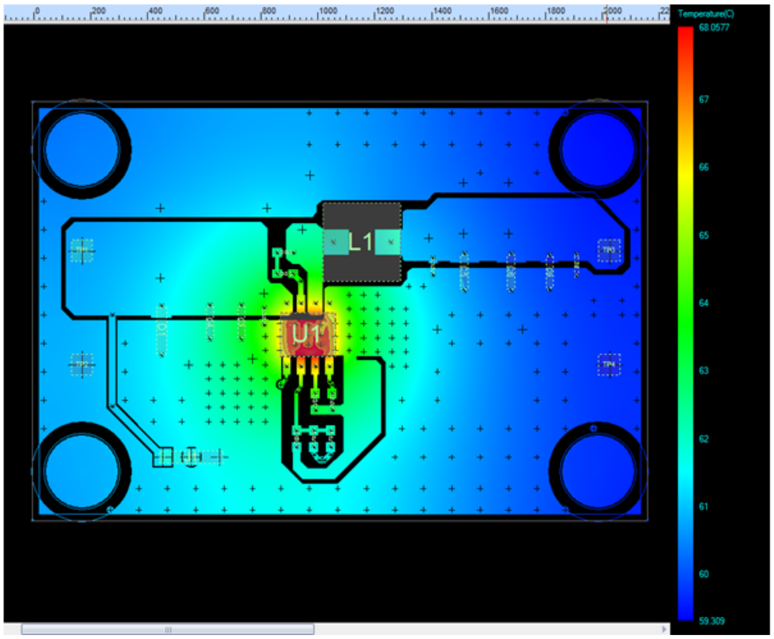




Top Layer

Bottom Layer

Fig 12: Evaluation Board Layout



U1: BD9D321EFJ

- **Max. power dissipation: 1.476 W @VIN=4.5V**
- **Component temperature = 68.06 ^{0}C**

L1: 744311220

- **Max. power dissipation: 0.1026 W**
- **Component temperature = 62.46 ^{0}C**

Fig 13: BD9D321EFJ-E2EVK-101 Thermal Characteristics at Ta=25^{o}C, No air flow, V_{IN}=4.5V, V_{OUT}=1.8V, I_{OUT}=3A

Thermal note: If the board is operated above room temperature (Ta>25^{o}C), an active cooling source (fan) or heat sink (soldered to bottom of PCB) is required.

Additional layout notes:

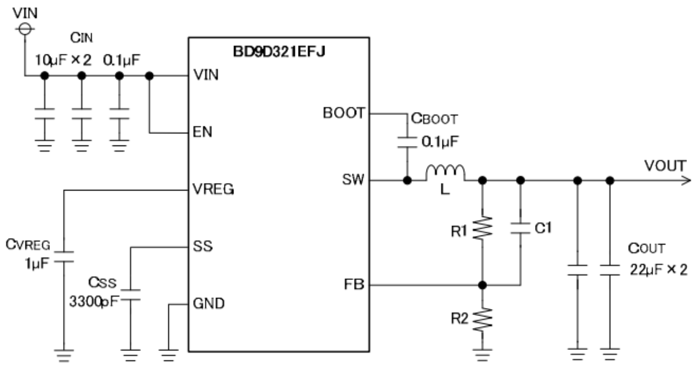
- The thermal pad on the backside of the IC has excellent thermal conduction to the chip, so making the GND plane as broad and wide as possible can help thermal dissipation. And using a large amount of thermal vias to facilitate the spread of heat to the different layers is also effective.
- The input capacitors should be connected to GND as close as possible to the V_{IN} terminal.
- The inductor and output capacitor should be placed as close to the SW pin as possible.
- For applications operating at or near maximum voltage conditions (18V max), additional precautions regarding heat dissipation need to be considered during board layout. The provided evaluation board is a 4-layer board meant for evaluation purposes only. At maximum conditions, the IC's internal thermal shutdown detection circuit will be potentially initiated and the output disabled until the junction temperature drops. Therefore, for final designs operating near these conditions, we recommend using one of the below PCB options for better heat dissipation of the IC.

  1) 4-layer PCB with internal GND planes connected to the IC GND pins
  2) 2-layer PCB with a heat sink attached to the IC package
  3) 2-layer PCB with a copper plane (>1oz) attached to the IC

- **Application Circuit Component Selection**

(1) Output LC Filter Constant

DC/DC converters require an LC filter for smoothing the output voltage in order to supply a continuous current to the load. Selecting an inductor with a large inductance will cause the ripple current ΔI_L that flows into the inductor to be small. However, decreasing the ripple voltage generated in the output is not advantageous in terms of the load transient response. An inductor with a small inductance improves transient response but results in a larger inductor ripple current which increases the ripple voltage at the output, exhibiting a trade-off relationship.
The recommended inductor values are shown in Fig 14.



Application Circuit

V_{OUT} [V]	R1 [kΩ]	R2 [kΩ]	C1 [pF]	L [μH] (Note 7)
1.0	6.8	22	- (Note 6)	1.5
1.05	8.2	22	- (Note 6)	1.5
1.2	12+0.51	22	- (Note 6)	1.5
1.8	30	22	- (Note 6)	2.2
3.3	68+5.1	22	- (Note 6)	2.2
5.0	120+1.8	22	- (Note 6)	3.3
7.0	180	22	- (Note 6)	3.3

Fig 14: Recommended Component values

Note 6: C1 is a feed-forward capacitor. The IC can operate normally even if this capacitor is not connected. Additional phase boost can be achieved by adding a 5pF to 100pF capacitor (C1) in parallel with R1.
Note 7: Recommended inductors

- ALPS GLMC Series
- TDK SPM6530 Series

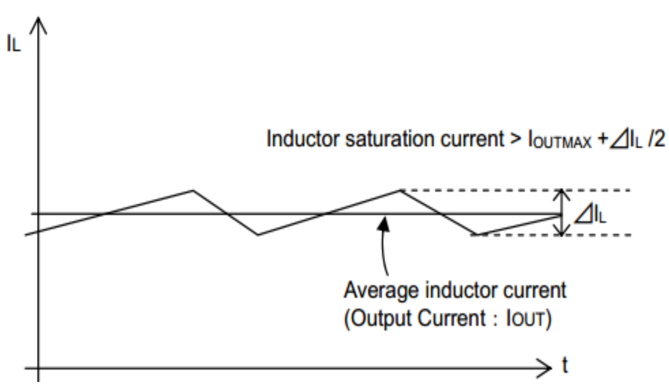


Fig 15. Current Waveform Through Inductor

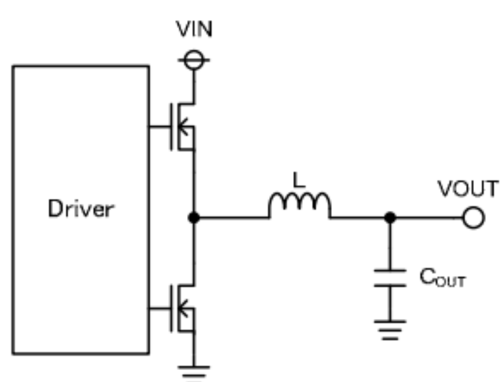


Fig 16. Output LC Filter Circuit

The inductor peak to peak ripple current ΔI_L is calculated using the following equation.

$$\Delta \mathbf{I_L} = \frac{\mathbf{V_{IN}} - \mathbf{V_{OUT}}}{\mathbf{L}} \times \frac{\mathbf{V_{OUT}}}{\mathbf{V_{IN}}} \times \frac{\mathbf{1}}{\mathbf{F_{OSC}}} \quad (\mathbf{A})$$

For example, with V_{IN}= 12 V, V_{OUT}= 1.8 V, L = 2.2µH and switching frequency F_{OSC} = 700 kHz, the calculated peak current ΔI_L is 1.0A.
The inductor saturation current must be larger than the sum of the maximum output current ($I_{OUT\ MAX}$) and 1/2 of the inductor ripple current (ΔI_L / 2).

The output capacitor C_{OUT} affects the output ripple voltage characteristics. Therefore, C_{OUT} must satisfy the following equation for ripple voltage.

$$\Delta \mathbf{V_{RPL}} = \Delta \mathbf{I_L} \times (\mathbf{R_{ESR}} + \frac{\mathbf{1}}{\mathbf{8} \times \mathbf{C_{OUT}} \times \mathbf{F_{OSC}}}) \quad (\mathbf{V})$$

Where R_{ESR} is the Equivalent Series Resistance (ESR) of the output capacitor.

- The capacitor rating must allow for a sufficient margin with respect to the output voltage.
  The output ripple voltage can be decreased by using a smaller ESR.
  A ceramic capacitor between 22µF to 100µF is recommended.

- Please pay attention to the total capacitance value when connecting an additional capacitor C_{LOAD} to the output capacitor C_{OUT}. Then determine C_{LOAD} and soft start time Tss [Refer to (3) Soft Start Setting below] so that the following conditions are satisfied.

$$\mathbf{C_{OUT}} + \mathbf{C_{LOAD}} \leq \frac{(\mathbf{I_{OCP}} - \mathbf{I_{OUT}}) \times \mathbf{T_{SS}}}{\mathbf{V_{OUT}}} \quad (\mathbf{\mu F})$$

Where I_{OCP} is the Over Current Protection Current limit value

(2) Output Voltage Setting
The output voltage value can be set by the feedback resistance ratio.

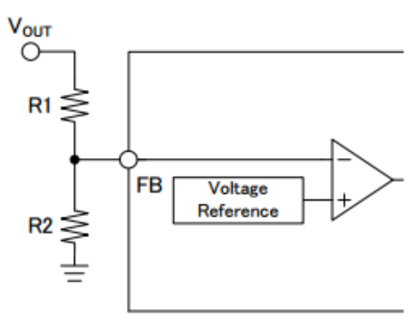


Fig 17: Feedback Resistor Circuit

$$\mathbf{V_{OUT}} = \frac{\mathbf{R_1} + \mathbf{R_2}}{\mathbf{R_2}} \times \mathbf{0.765}\ (\mathbf{V})$$

Please ensure that the following conditions for V_{IN} and V_{OUT} are met to ensure stable operation across all load regions

$$\mathbf{0.07} \leq \frac{\mathbf{V_{OUT}}}{\mathbf{V_{IN}}} \leq \mathbf{0.65}$$

(3) Soft Start Setting

Turning the EN terminal signal High activates the soft start function, which causes the output voltage to gradually rise while the current at startup is restricted, preventing output voltage overshoot and inrush current. The rise time depends on the value of the capacitor connected to the SS terminal.

$$\mathbf{T_d = \frac{C_{SS} \times V_{TH}}{I_{SS}}}$$

$$\mathbf{T_{SS} = \frac{C_{SS} \times V_{FB} \times 1.15}{I_{SS}}}$$

T_d : Soft Start Delay Time
T_{SS} : Soft Start Time
C_{SS} : Capacitor Connected to Soft Start Time Pin
V_{FB} : FB Terminal Voltage (0.765V typ)
V_{TH} : Internal Threshold Voltage (0.7V typ)
I_{SS} : Soft Start Pin Source Current (2.0μA typ)

For example, with C_{SS} = 3300pF,
T_d = (3300pF x 0.7V) / 2.0μA = 1.16msec
T_{SS} = (3300pF x 0.765V x 1.15) / 2.0μA = 1.45msec

- **Evaluation Board BOM**
  Below is a table showing the bill of materials. Part numbers and supplier references are also provided.

No.	Qty.	Ref	Description	Manufacturer	Part Number
1	1	C1	CAP CER 100PF 50V 5% NP0 0603	Murata	GRM1885C1H101JA01D
2	2	C2,C10	CAP CER 0.1UF 50V 10% X7R 0603	Murata	GRM188R71H104KA93D
3	2	C3,C4	CAP CER 10UF 35V 10% X5R 1206	Murata	GRM31CR6YA106KA12L
4	2	C5,C6	CAP CER 22UF 25V 10% X5R 1210	Murata	GRM32ER61E226KE15L
5	1	C11	CAP CER 1UF 25V 10% X7R 0603	Murata	GRM188R71E105KA12D
6	1	C12	CAP CER 3300PF 50V 10% X7R 0603	Murata	GRM188R71H332KA01D
7	1	D1	TVS DIODE 18VWM 29.2VC SMA	Littelfuse Inc	SMAJ18A
8	1	J1	CONN HEADER VERT .100 3POS 15AU	TE Connectivity	87224-3
9	1	L1	INDUCTOR POWER 2.2UH 9A SMD	Wurth	744311220
10	1	R1	RES 30K OHM 1/10W 1% 0603 SMD	Rohm	MCR03ERTF3002
11	1	R2	RES 22K OHM 1/10W 1% 0603 SMD	Rohm	MCR03ERTF2202
12	1	R3	RES 0.0 OHM 1/10W JUMP 0603 SMD	Rohm	MCR03ERTJ000
13	2	TP1,TP3	TEST POINT PC MULTI PURPOSE RED	Keystone Electronics	5010
14	2	TP2,TP4	TEST POINT PC MULTI PURPOSE BLK	Keystone Electronics	5011
15	1	U1	IC REG BUCK SYNC ADJ 3A 8HTSOP	Rohm	BD9D321EFJ-E2
16	1		Shunt jumper for header J1(item #8) CONN SHUNT 2POS GOLD W/HANDLE	TE Connectivity	881545-1

Notes

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ROHM SEMICONDUCTOR

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