Switching regulator series

PCB Layout for BD9D320EFJ and BD9D321EFJ

No.15xxxEAYxx

When designing switching nodes that operate at high speeds and switching power supplies that use a large current, PCB layout design is as important as circuit design. Major problems caused by poor PCB layout design include increase in noise superposed by output and switching signals, deterioration of regulation, and lack of stability. Such problems can be prevented by adopting an appropriate layout.

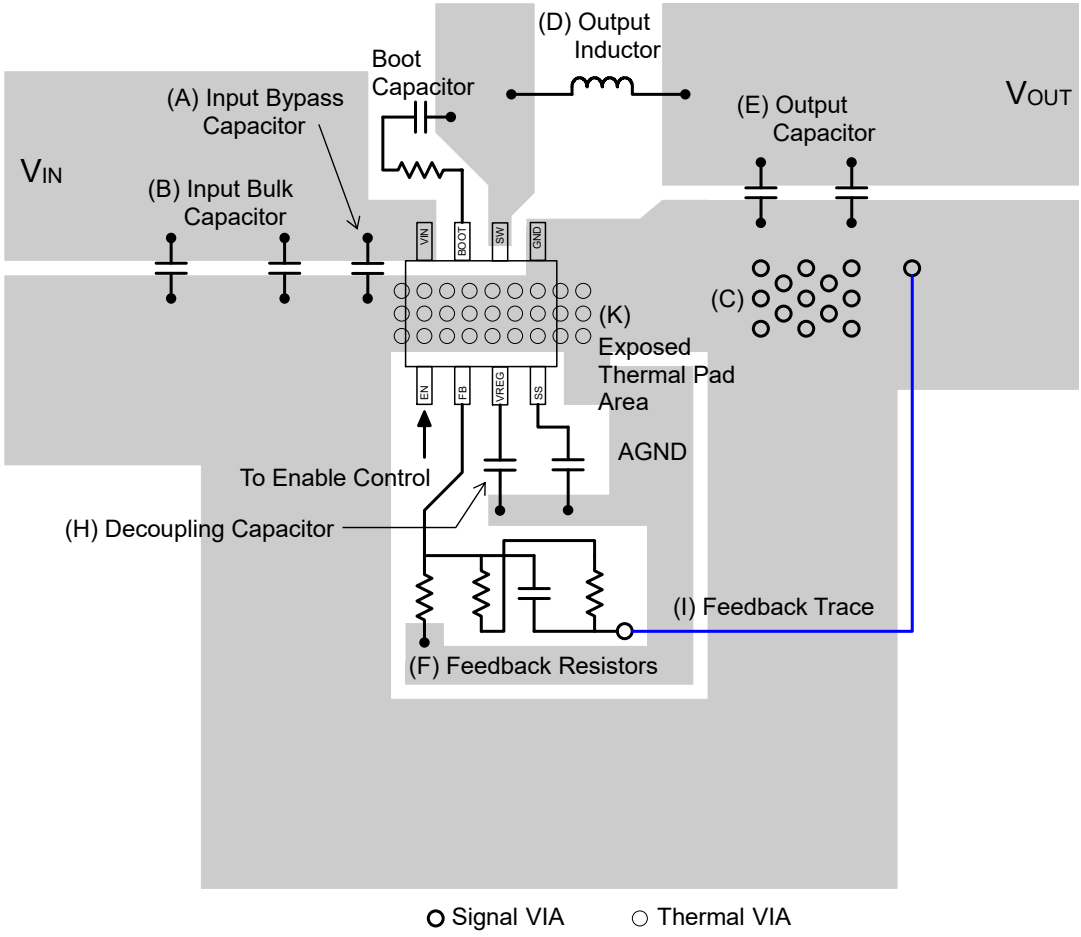

Figure 1. Example of a PCB layout

The V_{IN} pin at which high-frequency voltage switching occurs needs to be bypassed to PGND using a low-ESR ceramic capacitor (A). The bypass capacitor should be brought as close to the V_{IN} pin as possible (even within 1 mm) and positioned on the same surface as the IC. It is preferable to position the input bulk capacitor with the same requirements as that for the bypass capacitor. However, when positioning the bulk capacitor on the back surface owing to insufficient space for placing parts or any other such reason, it is necessary to satisfy the requirements for the bypass capacitor (B). Because high-frequency noise on the order of several hundred megahertz is superposed on the input capacitor ground, it is recommended to position the C_{IN} ground 1 cm to 2 cm away from the C_{OUT} ground to avoid noise propagation to the output. For the connection to the inner layer common ground of the set, multiple VIA holes should be provided for the output capacitor portion with less noise so that the current capacity can be secured (C). If connected at the input capacitor section, high-frequency noise will be propagated to the common ground.

The output inductor should be placed near the SW terminal. The wiring area must not be expanded beyond necessity to prevent EMI increase. In addition, if a ground or other wiring is placed directly under the inductor, decrease in the inductor value, increase in loss (decrease in Q), and propagation of switching noise may arise (D).

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The output capacitor should be connected to PGND (E).
Because the FB pin have high input impedances, they are easily affected by external disturbances. Parts connected to this pin should be placed near the IC pin and connected to AGND (F).
If a large current passes through AGND, a voltage drop may occur, resulting in device malfunction. It must be ensured that a large current does not flow through AGND (G).
To prevent noise mixture in the terminal, the decoupling capacitor for the VREG pin should be positioned as close to the IC as possible, even as close as 1 mm (H).
The voltage feedback loop should be detected at the point on the load side from the output capacitor. If it is detected at the inductor side, the influence of ripple current and voltage drop may cause an error in the output voltage. For the voltage feedback route, it is recommended to avoid wiring directly under and parallel to the inductor to prevent capacitive coupling and to route wires on the back surface or the inner layer sandwiching the ground plane (I). Further, attention must be paid to noise sources of other systems.
It is recommended to lay out the V_{IN}, V_{OUT}, and GND wiring on the same surface as the IC, and the wiring width should be more than the current capacity of the copper wiring (J). If layout on any other layer is required owing to restriction of the board area, multiple VIA holes should be provided to secure the current capacity.
For an IC with an exposed pad (back surface heat radiation pad), it is necessary to solder the pad on the ground. To achieve operation with the maximum load current, the ground region on the upper layer is required to have a sufficient radiation area. If sufficient area cannot be secured on the upper layer, the ground plane of the inner layer or back surface layer must be used with provision of multiple VIA holes near or directly under the IC to improve the radiation performance (K).

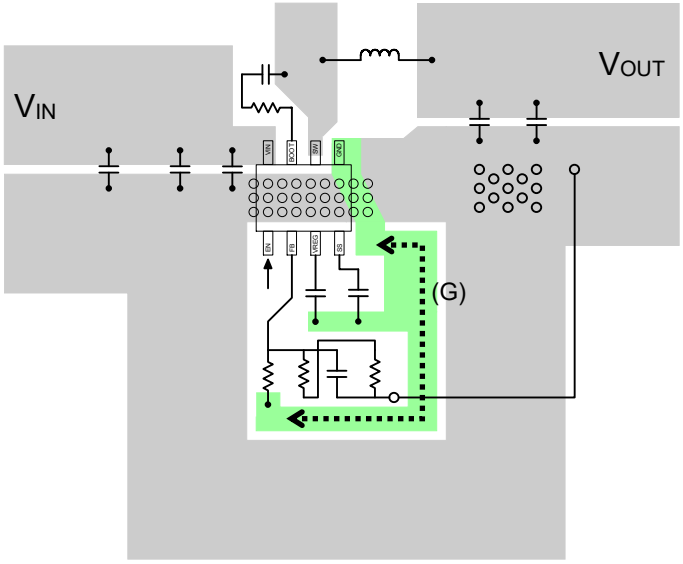

Figure 2. AGND wiring

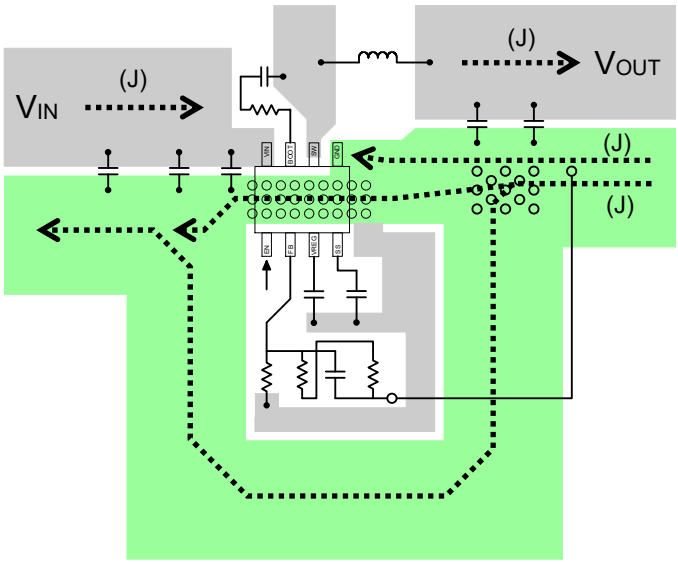

Figure 3. PGND wiring

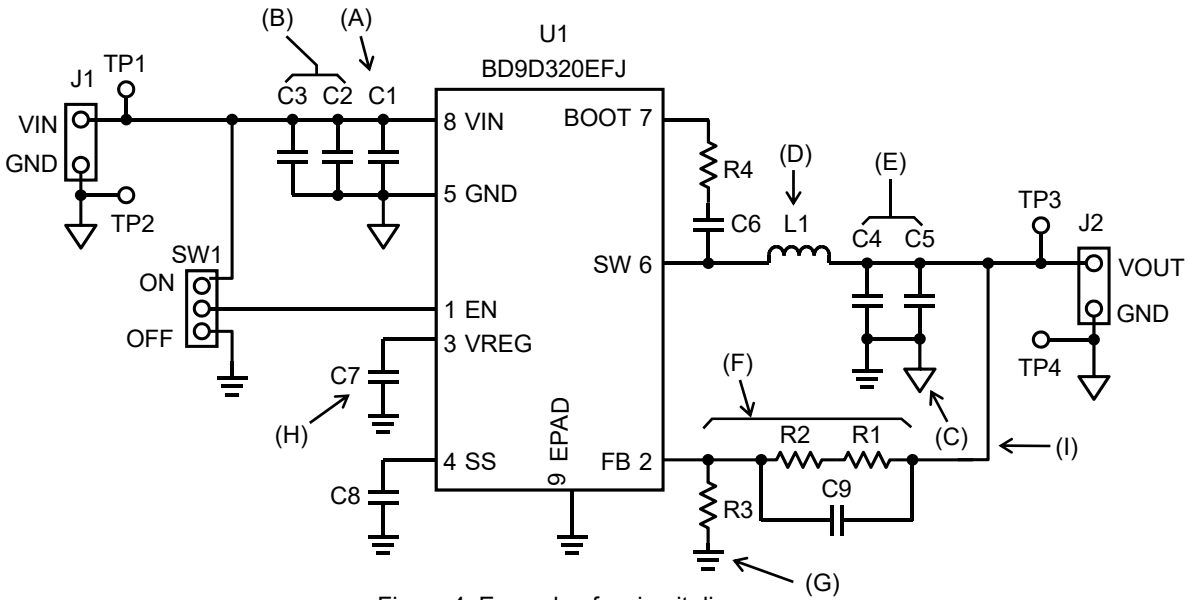

Figure 4. Example of a circuit diagram

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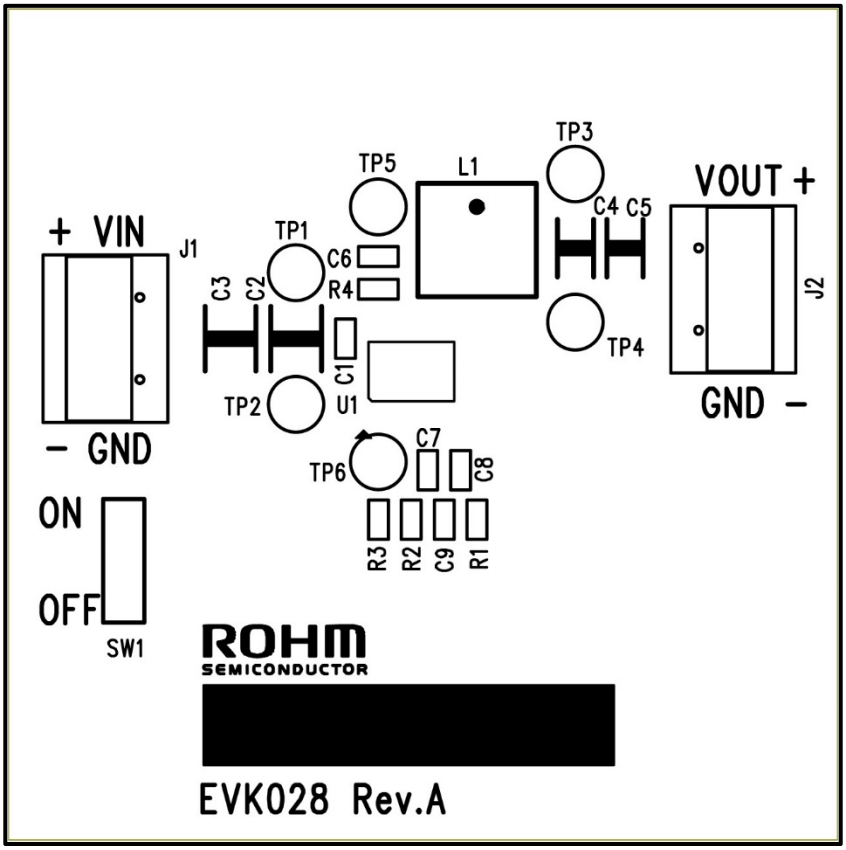

Figure 5. Top silk screen (Top view)

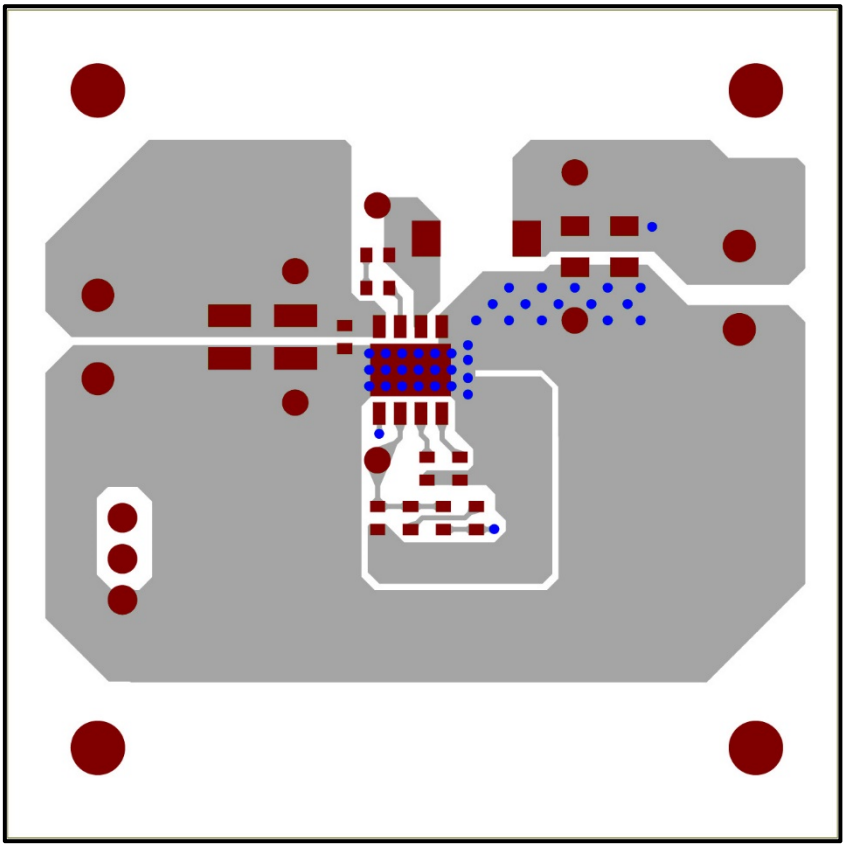

Figure 6. Top surface layout (Top view)

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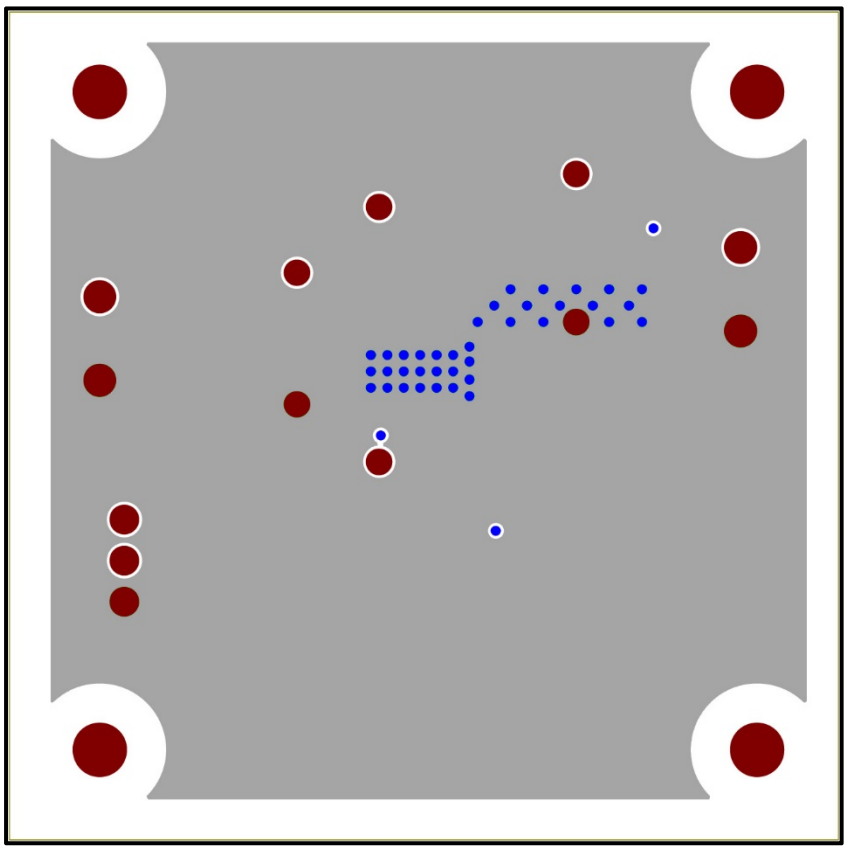

Figure 7. L2 and L3 layout (Top view)

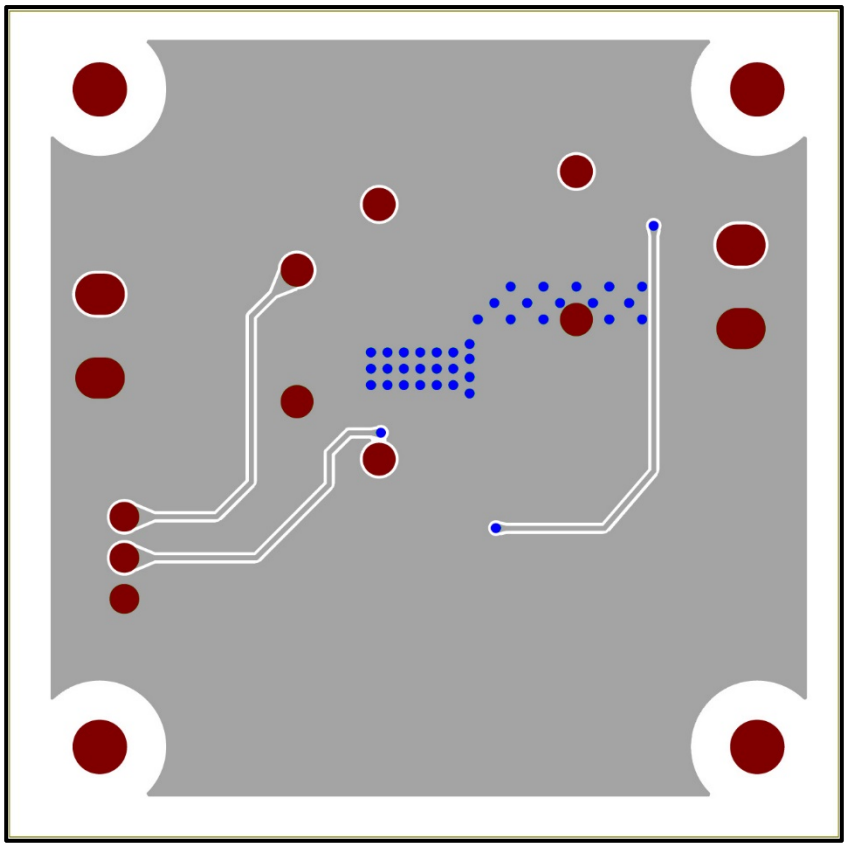

Figure 8. Bottom surface layout (Top view)

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