

## Primary Buck DC/DC Converter

# Single 2.2 MHz Buck DC/DC Converter For Automotive BD9P108MUF-C Evaluation Board

BD9P108MUF-TSB-001 (3.5 to 40V Input, 1.0A)

## Introduction

This user's guide will provide the necessary steps to operate the Evaluation Board of ROHM's BD9P108MUF-C Buck DC/DC converter. This includes the external parts, operating procedures and application data.

## Description

This Evaluation Board was developed for ROHM's single 2.2 MHz buck DC/DC converter BD9P108MUF-C. BD9P108MUF-C is a current mode synchronous buck DC/DC converter with integrated POWER MOSFETs. The BD9P108MUF-C accepts a power supply input range of 3.5 V to 40 V and generates a maximum output current of 1 A. BD9P108MUF-C generates an output voltage range of 0.8 V to 8.5 V using external resistors.

## Application

Automotive Powered Supplies

Consumer Powered Supplies

## Recommended Operating Conditions

Table 1. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units	Conditions
Input Voltage	3.5	-	40	V	Initial startup is 4.0 V or more
Output Voltage (Note1)	0.8	-	8.5	V	
Output Current Range	-	-	1.0	A	OCP_SEL = H : 1.0 A (Max) OCP_SEL = L : 0.5 A (Max)
Switching Frequency	-	2.2	-	MHz	
Maximum Efficiency	-	85.8	-	%	VO = 3.3 V, Io = 0.5 A, Ta = 25 °C
Maximum Efficiency	-	91.4	-	%	VO = 5.0 V, Io = 0.7 A, Ta = 25 °C

(Note1) Although the minimum output voltage is configurable up to 0.8 V, it may be limited by the SW min ON pulse width. For the same reason, although the maximum output voltage is configurable up to 8.5 V, it may be limited by the SW minimum OFF pulse width.

## Evaluation Board



Figure 1. Evaluation Board Top View

## Evaluation Board Schematic

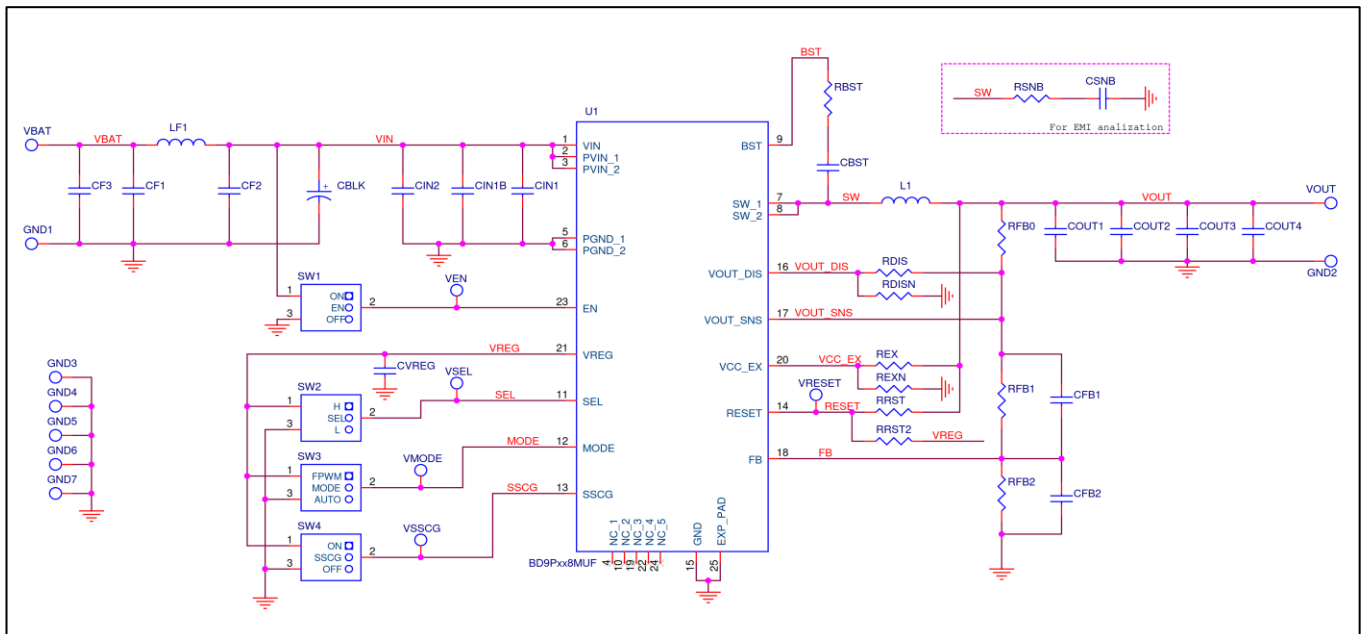


Figure 2. Circuit Diagram

## Operating Procedure

1. Turn off EN and connect the GND terminal of the power supply to the GND terminal of Evaluation Board.
2. Connect VCC pin of power supply to the VBAT pin of the Evaluation Board.
3. Connect the load to the Evaluation Board's VOUT and GND terminals. When using an electronic load, connect with the load turned off.
4. Connect a voltmeter to the Evaluation Board's VOUT and GND terminals.
5. Turn on the Power supply of VBAT. Turn ON the switch of EN terminal.
6. Make sure that the voltmeter is set to measure voltage.
7. Turn on the electronic load.

(Caution) This Evaluation Board does not support hot plug. Do not perform hot plug test.

(Note) If EN=High (EN short to VIN) before Power ON, the turn ON and turn OFF is controlled by VBAT only.

## Operation Mode Settings

Below is a table of BD9P108MUF-C operation modes selectable using OCP\_SEL, MODE and SSCG terminals.

Table 2. Mode Settings

Terminal	Setting	Operation Mode	Function
OCP_SEL	HIGH	OCP threshold selection	OCP threshold is set to 1.250 A (Typ.) Output Current maximum is 1 A.
	LOW		OCP threshold is set to 0.625 A (Typ.) Output Current maximum is 0.5 A.
MODE	HIGH	FPWM	Forced PWM mode
	LOW or OPEN	AUTO	Automatically switched between PWM and LLM mode.
	Apply a clock to this pin	SYNC	Activate synchronization mode
SSCG	ON (HIGH)	Select Spread Spectrum function	Enable Spread Spectrum
	OFF (LOW)		Disable Spread Spectrum

(Note) If setting is High, the terminal is shorted to VREG, and if setting is Low, the terminal is shorted to GND.

## Pin Configuration

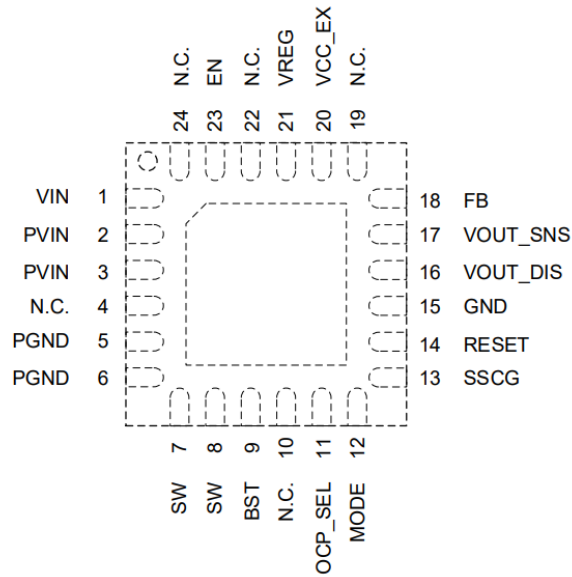


Figure 3. Pin Configuration (Top View)

## Parts List (BD9P108MUF-C)

Table 3. Parts list (3.3 V, 1.0 A)

	Part No	Value	PKG(inch)	PKG(mm)	Manufacturer	Part Name(Series)
π type filter	CF1	4.7μF	1210	3225	Murata	GCM32ER71H475K
	CF3	Open	-	-	-	-
	LF1	2.2μH	2524h18	6360h45	TDK	CLF6045NIT-2R2N-D
	CF2	0.1μF	0402	1005	Murata	GCM155R71H104K
	CBLK	220μF	0404h04	1010h10	Nichicon	UWD1V221MCL1GS
Basic	CIN2	4.7μF	1210	3225	Murata	GCM32ER71H475K
	CIN1	0.1μF	0402	1005	Murata	GCM155R71H104K
	CIN1B	Open	-	-	-	-
	CVREG	1μF	0805	2012	Murata	GCM21BR71C105K
	CBST	0.1μF	0402	1005	Murata	GCM155R71H104K
	RBST	0Ω	0402	1005	ROHM	MCR01 Series
	RSNB	Open	-	-	-	-
	CSNB	Open	-	-	-	-
	RRST	10kΩ	0402	1005	ROHM	MCR01 Series
RRST2 (Note 3)	Open	-	-	-	-	
Application	L1	6.8μH	2524h18	6360h45	TDK	CLF6045NIT-6R8N-D
	COUT1 to 4 (Note 1)	10μF x 3 (Mounted on Board)	1210	3225	Murata	GCM32ER71E106K
		or 22μF x 2	1210	3225	Murata	GCM32ER71A226K
		or 22μF x 3	0805	2012	Murata	GCM21BD70J226M
	RFB0	0Ω	0402	1005	ROHM	MCR01 Series
	RFB1	75kΩ	0402	1005	ROHM	MCR01 Series
	RFB2	24kΩ	0402	1005	ROHM	MCR01 Series
	CFB1 (Note 4)	Open	-	-	-	-
	CFB2 (Note 4)	Open	-	-	-	-
	RDIS	0Ω	0402	1005	ROHM	MCR01 Series
	RDISN	Open	-	-	-	-
REX (Note 2)	0Ω	0402	1005	ROHM	MCR01 Series	
REXN (Note 2)	Open	-	-	-	-	

Table 4. Parts list (5.0 V, 1.0 A)

	Part No	Value	PKG(inch)	PKG(mm)	Manufacturer	Part Name(Series)
π type filter	CF1	4.7μF	1210	3225	Murata	GCM32ER71H475K
	CF3	Open	-	-	-	-
	LF1	2.2μH	2524h18	6360h45	TDK	CLF6045NIT-2R2N-D
	CF2	0.1μF	0402	1005	Murata	GCM155R71H104K
	CBLK	220μF	0404h04	1010h10	Nichicon	UWD1V221MCL1GS
Basic	CIN2	4.7μF	1210	3225	Murata	GCM32ER71H475K
	CIN1	0.1μF	0402	1005	Murata	GCM155R71H104K
	CIN1B	Open	-	-	-	-
	CVREG	1μF	0805	2012	Murata	GCM21BR71C105K
	CBST	0.1μF	0402	1005	Murata	GCM155R71H104K
	RBST	0Ω	0402	1005	ROHM	MCR01 Series
	RSNB	Open	-	-	-	-
	CSNB	Open	-	-	-	-
	RRST	10kΩ	0402	1005	ROHM	MCR01 Series
	RRST2 (Note 3)	Open	-	-	-	-
Application	L1	6.8μH	2524h18	6360h45	TDK	CLF6045NIT-6R8N-D
	COUT1 to 4 (Note 1)	10μF x 3 (Mounted on Board) or 22μF x 2 or 22μF x 3	1210	3225	Murata	GCM32ER71E106K
			1210	3225	Murata	GCM32ER71A226K
			0805	2012	Murata	GCM21BD70J226M
	RFB0	0Ω	0402	1005	ROHM	MCR01 Series
	RFB1	68kΩ	0402	1005	ROHM	MCR01 Series
	RFB2	13kΩ	0402	1005	ROHM	MCR01 Series
	CFB1 (Note 4)	Open	-	-	-	-
	CFB2 (Note 4)	Open	-	-	-	-
	RDIS	0Ω	0402	1005	ROHM	MCR01 Series
	RDISN	Open	-	-	-	-
	REX (Note 2)	0Ω	0402	1005	ROHM	MCR01 Series
	REXN (Note 2)	Open	-	-	-	-

(Note 1)

VOUT	Recommended L Value	Minimum COUT Value (Note1-1,2)
≥ 5.0 V	6.8 μH	COUT_WORST ≥ 16 μF
< 5.0 V	6.8 μH	COUT_WORST ≥ $\frac{81.8}{V_{OUT}}$ μF (*)

\* VOUT is the output voltage [V]

(Note 1-1) When selecting the output capacitor, ensure that the capacitance, COUT\_WORST, of the above equation is maintained at the characteristics of DC Bias, AC Voltage, temperature, and tolerance.

(Note 1-2) If the capacitance falls below this value, oscillation may happen. When using electrolytic capacitor and conductive polymer hybrid aluminum electrolytic capacitor, please place it in addition to the ceramic capacitors with the capacity described above. The changes in the frequency characteristic are greatly affected by the type and the condition (temperature, etc.) of parts that are used, the wire routing and the layout of the PCB. Please confirm stability and responsiveness in actual application.

(Note 2) VCC\_EX is power supply input for internal circuit. VREG voltage is supplied from VCC\_EX when voltage between 3.2V (VTEXH, Max) and 5.65 V (VEXOVL, Min) is connected to this pin. Connecting this pin to VOUT improves efficiency. In case of not use this function, connect this pin to GND.

Output Voltage	REX setting	REXN setting	VCC_EX State
$3.2\text{ V} \leq \text{VOUT} \leq 5.65\text{ V}$	0 $\Omega$	Open	Connected to VOUT
$\text{VOUT} < 3.2\text{ V}$ or $\text{VOUT} > 5.65\text{ V}$	Open	0 $\Omega$	Connected to GND

(Note 3) RESET terminal should be pulled-up to VREG via RRST2 when the output setting is over 6.5 V because RESET pin's absolute maximum rating is 7.0 V. If RESET is not pulled-up to VOUT, it can be pulled-up to VREG via RRST2 by default.

(Note 4) Please use CFB1 and CFB2 PCB patterns to improve the frequency characteristics. Set these values by following the guide in page 31 of datasheet.

(Note 5) If the recommended parts on tables 3 to 7 are not available anymore due to end of production, different parts will be used on the test board because the end of production parts are deprecated.

## Board Layout

Evaluation Board PCB information

Number of Layers	Material	Board Size	Copper Thickness
4	FR-4 High Tg	100mm x 75mm x 1.6mm	2oz(70μm) / 1oz (35μm) / 1oz (35μm) / 2oz(70μm)

The layout is shown below.

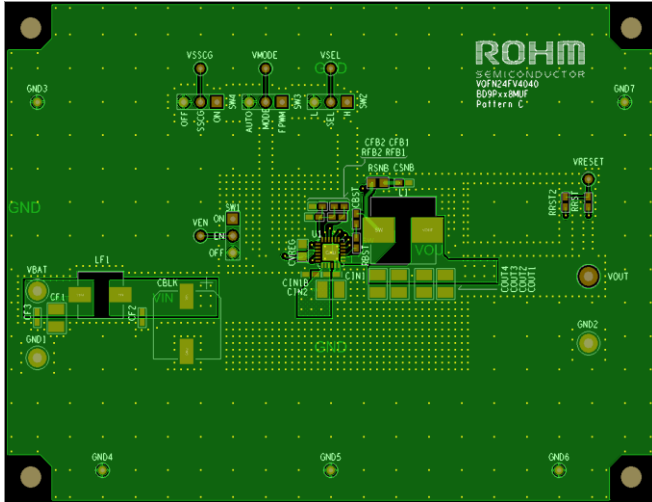


Figure 4. Top Layer Layout  
(Top View)

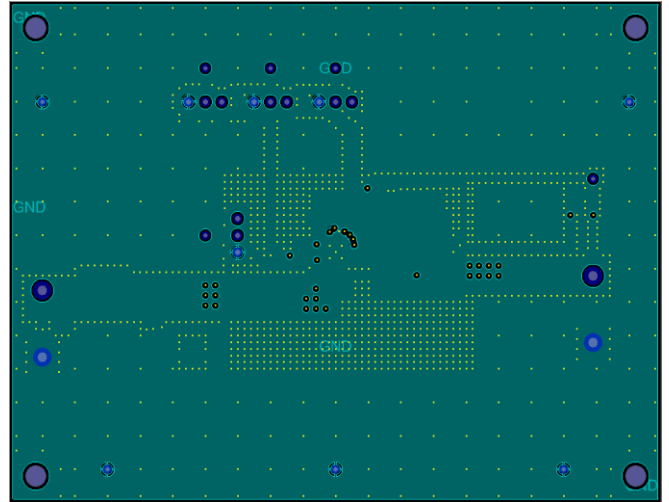


Figure 5. Middle1 Layer Layout  
(Top View)

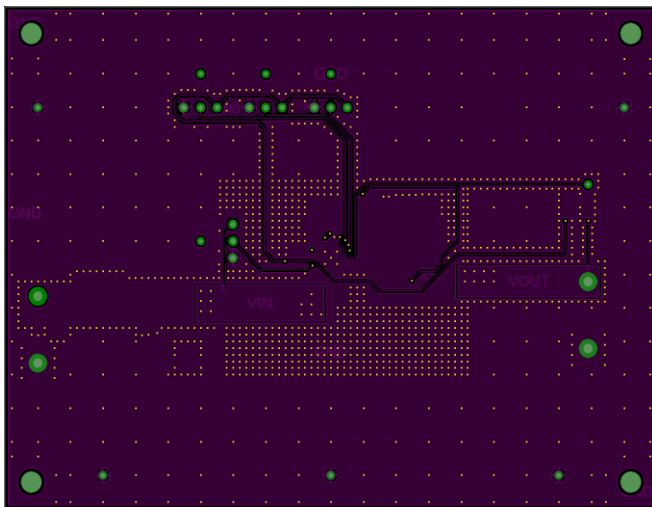


Figure 6. Middle2 Layer Layout  
(Top View)

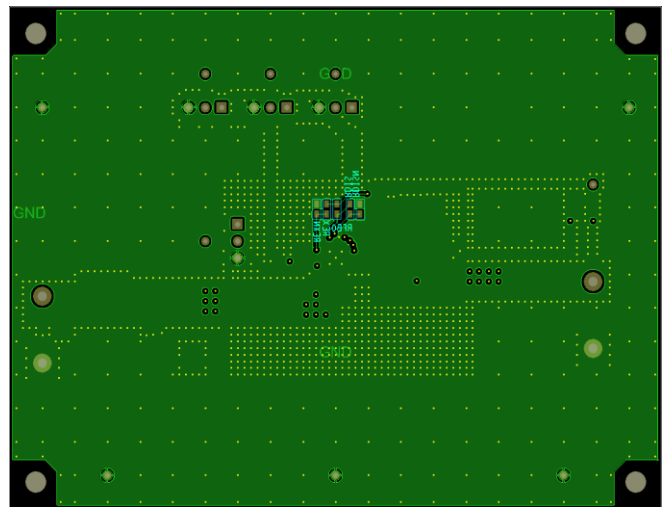


Figure 7. Bottom Layer Layout  
(Top View)

**Revision History**

<b>Date</b>	<b>Revision Number</b>	<b>Description</b>
15. Sep. 2023	001	Initial release



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