

This application note explains the step-up circuit using a bootstrap capacitor. In buck converters, this circuit is used when the highside switch is the N-ch MOSFET.

1. Role of the bootstrap circuit in the buck converter

The configuration of the circuit in proximity to a buck converter depends on the polarity of the high-side switch.

When a P-ch MOSFET is used for the high-side switch, there are advantages over using a N-ch MOSFET, such as the capability of driving the switch with input voltage V_{IN} as the gate voltage, as well as voltage reduction and obtainment of the maximum duty. On the contrary, the use of a P-ch MOSFET requires a larger chip area for passing the same current.

The use of an N-ch MOSFET for the high-side switch requires a gate voltage of V_{IN} + Vth (threshold voltage of the N-ch MOSFET) or higher. A step-up circuit is required because the gate voltage is higher than V_{IN} . This circuit is configured with an internal diode and an external bootstrap capacitor (charge pump type). The total cost, including the cost of the external bootstrap capacitor, can be lowered because the chip area can be reduced compared with the P-ch MOSFET, as mentioned above.

2. Description of the charge pump operation

In the charge-pump-type step-up circuit, the essential parts include a diode and a capacitor (bootstrap capacitor). The diode is often built-in as an element in the IC, and only the bootstrap capacitor is connected externally.

Figure 1 shows an example of an actual circuit.

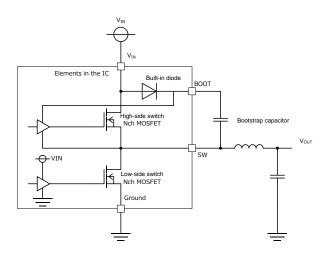


Figure 1. Example of a charge-pump-type step-up circuit

The voltages on the SW and BOOT pins in the example of Figure 1 are described as shown in Figure 2, where Vf is the forward direction voltage of the built-in diode.

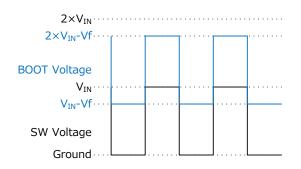


Figure 2. Voltages of SW and BOOT

When the SW voltage is low during the switching operations in Figure 2, the electric charge is stored in the capacitor from V_{IN}, thus resulting in the voltage of V_{IN} - Vf across the capacitor. When the SW voltage is high, the BOOT voltage increases up to $2 \times V_{IN}$ - Vf, and the built-in diode maintains the voltage at $2 \times V_{IN}$ - Vf. Therefore, the BOOT voltage switches between V_{IN} - Vf and $2 \times V_{IN}$ - Vf (Figure 3).

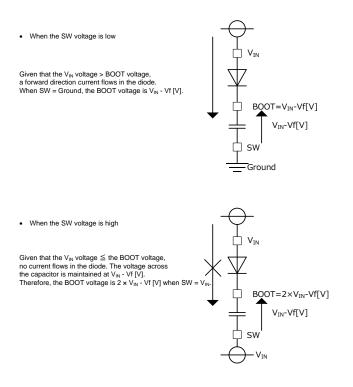
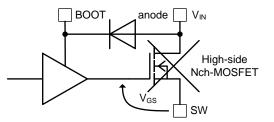


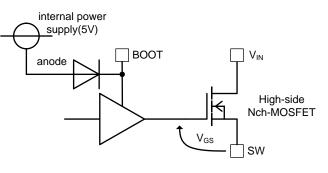
Figure 3. Charge-pump-type step-up circuit diagram

When this BOOT voltage is used as the gate voltage for the high-side N-ch MOSFET, you can obtain a voltage between the gate and the source (V_{GS}) that is sufficient to completely turn ON the MOSFET.

In this example, the anode of the built-in diode is obtained from V_{IN} , and the BOOT voltage can increase up to 2 × V_{IN} - Vf as described in the calculation. It is possible that this BOOT voltage may exceed the breakdown voltage between the gate and source of the high-side N-ch MOSFET. Therefore, in designing products with a high input voltage, an internal power supply of approximately 5 V is connected to the anode so that the BOOT voltage is maintained below the breakdown voltage between the gate and the source (Figure 4).



When the anode of the diode is obtained from V_{IN}, the gate voltage of the high-side N-ch MOSFET is V_{IN} - Vf [V] at maximum. When a high voltage is applied to V_{IN} and when the V_{GS} rating is exceeded, the high-side N-ch MOSFET will be destroyed.



When the anode of the diode is connected to an internal power supply of approximately 5 V, the gate voltage of the high-side N-ch MOSFET is 5 - Vf [V] at maximum. Therefore, the V_{GS} rating of the N-ch MOSFET will not be exceeded, and the high-side N-ch MOSFET can be protected.

Figure 4. Method that considers preventing the V_{GS} rating from

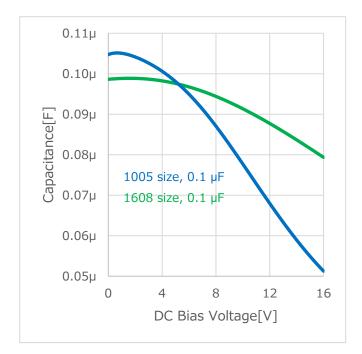
being exceeded

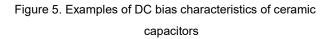
3. Capacitance of the bootstrap capacitor

For the minimum capacitance of the bootstrap capacitors, follow the capacitance described in each data sheet. Use a small ceramic capacitor for the bootstrap capacitors. It is necessary to consider the DC bias characteristics of the ceramic capacitors and to confirm that the actual capacitance corresponds with the capacitance described in the data sheet.

The DC bias characteristics refer to the characteristics of variation in capacitance due to the DC voltage applied across the ceramic capacitor. Generally, the capacitance tends to decrease as the DC voltage increases. Furthermore, the variation in capacitance also depends on the size.

Figure 5 shows the examples of DC bias characteristics with different sizes.





When 16 V is applied to the 1005 size ceramic capacitor, the actual capacitance falls significantly below the nominal value of 0.1 μ F. Furthermore, approximately half of the nominal value remains. Although the minimum capacitance of the bootstrap capacitor varies with each IC, an excessively small capacitance may result in an electric charge that is insufficient for gate driving. The insufficient electric charge may lead to unstable gate driving and impair the operation.

However, we recommend the use of the minimum capacitor that satisfies the minimum capacitance because a larger size will affect the cost. On the contrary, an excessively large capacitance could delay the increase in the voltage across the capacitor and reduce the voltage for gate driving.

The adequate value of the capacitance can be obtained from the following equations. When the high-side N-ch MOSFET is ON, the electric charge stored in the bootstrap capacitor is consumed for the gate driving.

$$Q_{LOSS} = Q_G + I_{BOOT} \times \frac{D}{f}$$
(1)

 Q_{LOSS} : Total electric charge consumed when N – ch MOSFET is ON Q_G : Gate charge and electric charge lost in the internal circuit I_{BOOT} : Current passing from the bootstrap capacitor f: Switching frequency D: Switching duty

Here, the relation of the variation in the voltage between BOOT and SW (ΔV_{BS}), the capacitance of the bootstrap capacitor (C_{BOOT}), and the Q_{LOSS} is expressed as follows.

$$C_{BOOT} \ge \frac{Q_{LOSS}}{\Delta V_{BS}}$$
(2)

Considering that it is desirable to maintain ΔV_{BS} at 0.1 V or below, the equation can be described as follows.

$$C_{\text{BOOT}} \ge \frac{Q_{\text{LOSS}}}{0.1} \tag{3}$$

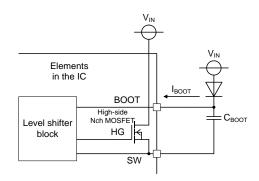


Figure 6. Circuit diagram required for CBOOT determination

As an example, a calculation is performed with Q_G = 10 nC, I_{BOOT} = 10 nA, D = 0.3, and f = 1 MHz. From Equation (1),

 $Q_{LOSS} = 10nC + 10nA \times \frac{0.3}{1MHz} \cong 10nC$

When this value is substituted in Equation (3),

 $C_{BOOT} \geq \frac{10nC}{0.1} = 0.1 \mu F$

Therefore, C_{BOOT} should be 0.1 µF or larger.

However, the capacitances described in the data sheet should be used because they are designed according to the results obtained from these equations.

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