

System Reference series for Automotive application

ROHM Power Supply Design for Telechips TCC805x (Dolphin3M/Dolphin3E/Dolphin+QD) SoC

This document explains the system reference of a power solution for the Telechips TCC805x(Dolphin3M/Dolphin3E/Dolphin+QD) SoC (system-on-chip) power rails using the BD96801Q50-C and BD96801Q51-C. This power solution is supposed an input voltage of 4 V(+/-5%). BD96801Q50-C and BD96801Q51-C have two 4.0A buck converters and two 2.0A buck converters and three 0.3A LDOs. They have four buck converters configured to work as dual 2-phase converters. They have OTP(One time programmable) that are written the output voltage settings, ON/OFF sequences and etc. required for Telechips TCC805x. The ON/OFF sequence required for the Telechips TCC805x is realized with only one line of EN signal from the main system. The OTP is programable in Rohm's production line, so no adjustment is required by customer. This power solution is an example how Telechips TCC805x required rails can be powered with Rohm Power products. Reference design with Rohm power solution and Telechips TCC805x, all needed peripherals, memory, and connections was designed and built to confirm the functionality and performance of the power solution.

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1. Design Parameters

Table 1. shows the power rails, load requirements, and ON/OFF sequence.

Table 1. Design Parameters

Voltage	SoC Current (Note2) (Note3)	Power Source	Rail Name	Sequence (Power ON) (Note1)	Sequence (Power OFF)
3.3V	10mA	External Single LDO1	GPK_RTC_3.3V	-	-
1.8V	10mA	External Single LDO2	GPK_RTC_1.8V	-	-
1.8V	850mA (3M/3E) 818mA (+QD)	BD96801Q50-C Buck1	IO_1.8V	1.408ms	16ms
0.9V	1800mA (3M/3E) 900mA (+QD)	BD96801Q50-C Buck2	CPU_0.9V	0.64ms	25.6ms
0.8V	4900mA (3M/3E) 3300mA (+QD)	BD96801Q50-C Buck3	GB_0.8V	0.256ms	34.816ms
		BD96801Q50-C Buck4			
3.3V	-	BD96801Q50-C LDO5	HVBUCK_EN	0.002ms	45.056ms
1.2V	150mA (3M/3E) 100mA (+QD)	BD96801Q50-C LDO6	MIPI_1.2V	1.408ms	16ms
3.3V/1.8V	10mA	BD96801Q50-C LDO7	SDIO	2.048ms	11.008ms
3.3V	180mA (3M/3E) 150mA (+QD)	BD96801Q51-C Buck1	IO_3.3V	2.048ms	11.008ms
0.6V	620mA (3M/3E) 320mA (+QD)	BD96801Q51-C Buck2	MEMQ_0.6V	4.224ms	1.024ms
0.8V	3800mA (3M/3E) 5400mA (+QD)	BD96801Q51-C Buck3	CORE_0.8V	0.64ms	25.6ms
		BD96801Q51-C Buck4			
3.3V	-	BD96801Q51-C LDO5	EN_A	0.64ms	25.6ms
3.3V	-	BD96801Q51-C LDO6	EN_B	1.28ms	16ms
3.3V	-	BD96801Q51-C LDO7	EN_C	1.664ms	11.008ms
1.0V (3M/3E) 0.8V (+QD)	5500mA (3M/3E) 1800mA (+QD)	External Single Buck1	CPU_1.0V (3M/3E) CPU_0.8V (+QD)	0.64ms	25.6ms
1.8V	-	External Single LDO3	LPDDR4_1.8V	1.28ms	16ms
1.1V	2mA	External Single Buck2	MEM_1.1V	1.664ms	11.008ms
1.1V	-	External Single Buck3	LPDDR4_1.1V	1.664ms	11.008ms

(Note1) Indicates the delay time of each output after the OTP read is completed after applying the EN signal. This is not the startup time of each output after EN=High. For details, please check 3.ON/OFF sequence.

(Note2) (3M/3E) = Dolphin3M/Dolphin3E, (+QD) = Dolphin+QD

(Note3) The SoC currents are reference values. To be precise, please confirm the SoC datasheet. Also, the load currents of the PMIC depend on the other components used, such as DDR.

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