

BD71847MWV Functional Errata

The problem described on errata has been solved with new product **BD71847AMWV**. The **BD71847MWV** will be replaced by the **BD71847AMWV**. **BD71847AMWV** has same foot print and functionality with previous **BD71847MWV**.

The difference is only that the initial value of the REV register (address 0x00) has been changed from **0xA0** to **0xA1** for identification.

1. Functional Errata History

Date	Errata Number	Title	Silicon Revision	
			BD71847MWV (REV[0x00]=0xA0)	BD71847AMWV (REV[0x00]=0xA1)
26.Mar.2019	BD71847_001	PMIC Hung in OTP Load State	Yes	No

A “Yes” entry indicates the erratum applies to a particular revision level, and “No” entry means it does not apply.

2. PMIC Hung in OTP Load State

2.1. Summary

When PMIC is in shutdown state **EMG** and VSYS voltage is below 2.7V, a 100 μs - 390 μs surge on VSYS causes PMIC to transition to and remains in OTP loading state **READY** until power is removed.

One possible workaround is to disable the reloading of OTP settings on resets. Since this is likely to be undesirable for many use cases, new silicon stepping is being planned. The fix is a simple, low-risk metal layer change.

New silicon samples: 15 April 2019

New qualified samples: End of May 2019.

New PN: BD71847AMWV

2.2. Conditions That Leads to Failure

Figure 1 shows the power state transition diagram annotated with arrows showing how the problem could develop and manifest itself.

The test sequence below corresponds to the matching labeled arrows in the diagram.

1. Input supply VSYS is lowered below VSYS_UVLO level (2.7V) => PMIC enters **EMG** state in which all power rails are turned off.
 - VSYS_UVLO is 2.7V (sweeping down) – 3.0V (sweeping up)
2. VSYS is raised above VSYS_UVLO (3.0v) for a ‘short’ time to simulate noise spike => PMIC enters **READY** state in which OTP settings are loaded.

- Here, short means 100 μs – 390 μs. Anything shorter is filtered out by the debounce circuit. Longer duration doesn't cause problem. The reason is OTP loading takes approximately 390 μs.
- 3. If the noise spike lasts less than 390 μs, VSYS drops back to below VSYS_UVLO (2.7V) before OTP loading is completed. PMIC remains in READY state until power is removed, or, more precisely, until VSYS is below 1.35V. At that point, PMIC goes to **OFF** state – the same starting point as first time power-on.

With one exception, the above behavior holds regardless of how PMIC enters EMG state. Therefore, in addition to VSYS being less than VSYS_UVLO, other events that may lead to failure is thermal shutdown and power fault detected on a power rail. If the conditions in Steps 2 and 3 hold, these events result in PMIC hang as well.

Exception: this problem doesn't occur when PMIC enters EMG via OFF state (as in first time power-on)

Reason: OTP loading actually takes place in OFF state in this case. The deadlock condition described in 2.3 does not arise because neither the detection logic nor the state machine is operational in OFF state.

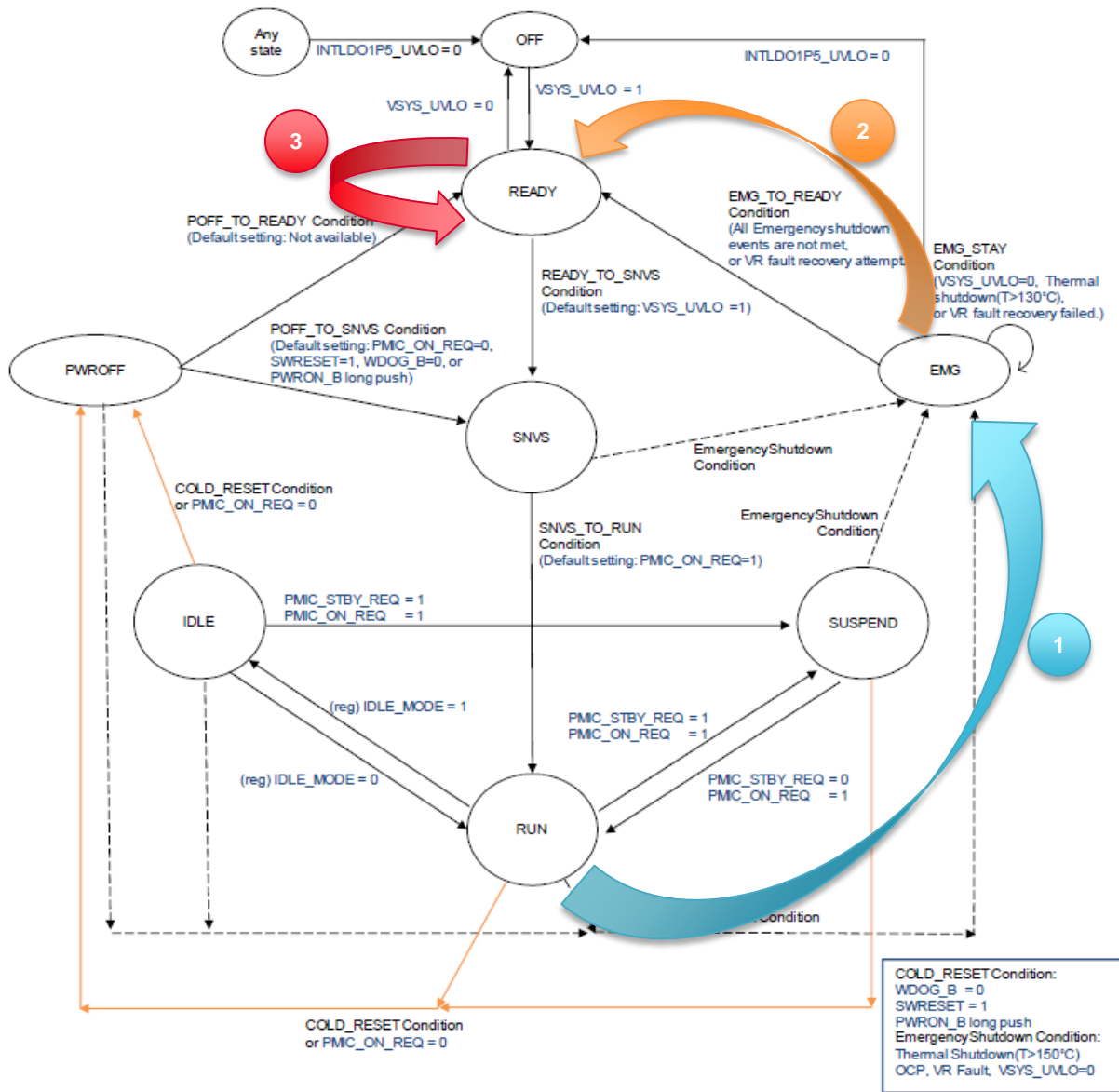


Figure 1: Power State Diagram

2.3. Root Cause – Design Details

PMIC is stuck in **READY** state because of a deadlock situation between the logic that detects state of VSYS (being below or above VSYS_UVLO) and the power state transition state machine that takes detection result as one of its input.

Internally a pulse is generated upon detection of VSYS_UVLO event. During OTP download while in **READY** state, such pulse is ignored. Since the event is not registered, the power state machine receives no trigger after OTP loading is completed to transition to another state. Hence PMIC remains in **READY**.

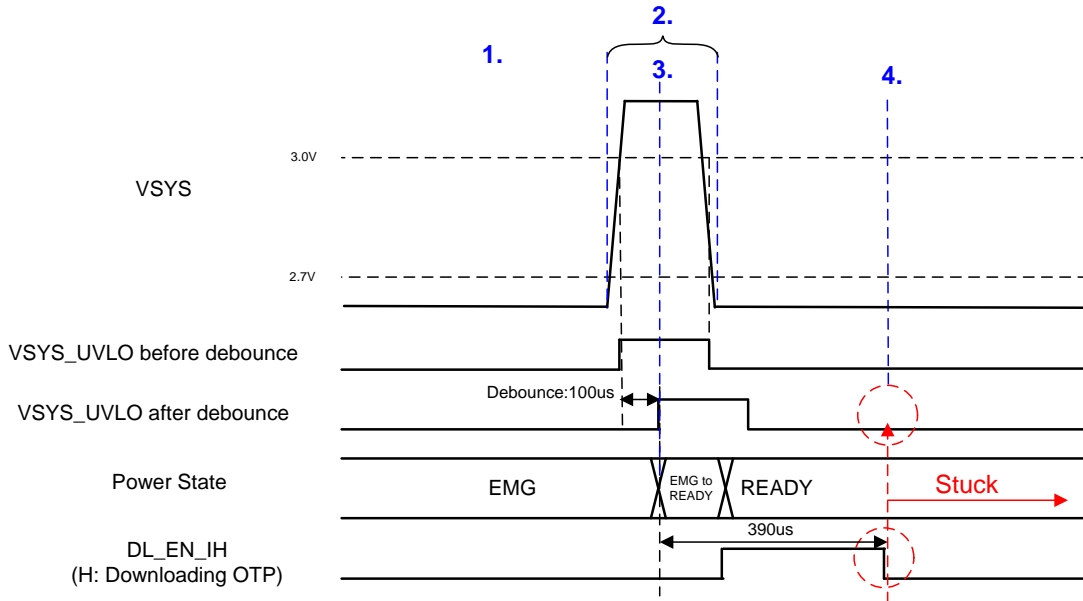


Figure 2: Power State Transition Diagram

2.4. Workaround

One possible work around is to disable the reloading of OTP while in **READY** state. This would eliminate the cause of deadlock described in 2.3 by reducing the OTP loading time – the time window deadlock may arise – to zero.

The drawback is the PMIC can't be re-initialized to a clean, known state after cold reset.

To disable OTP loading while in **READY**, OTP must be changed. Specifically, D5 (RELOAD_REG) in PWRCTRL0 register at address 0x03 is to be changed to '0'.

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
PWRCTRL0	R/W	DEBUG_STATE[1:0]		RELOAD_REG	-	-	-	WDOGB_SEL[1:0]		0xA2	0x03

Bit	Name	Function	Initial
D[7:6]	DEBUG_STATE[1:0]	Select Cold reset, Warm reset or No reset action when PWRON_B long push is detected. 00 = No reset action 01 = No reset action 10 = Cold reset 11 = Warm reset	10
D[5]	RELOAD_REG	Select OTP configurable registers initialization when the power state goes through READY state. 0 = No initialization 1 = Reload OTP registers and set to initial value	1
D[1:0]	WDOGB_SEL[1:0]	Select Cold reset, Warm reset or No reset action when WDOG_B is asserted to 0. 00 = No reset action 01 = No reset action 10 = Cold reset 11 = Warm reset	10

2.5. Hardware Fix – New Silicon Stepping

A silicon revision will fix the issue; no work around would be needed.

Availability.

New silicon samples: 15 April 2019

New qualified samples: End of May 2019.

New PN: BD71847AMWV

3. Revision History

Date	Revision Number	Description
26.Mar.2019	001	First Release

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