

Voltage Detector (Reset IC) Series

Method for Expanding Hysteresis Width

This application note explains a method to modify the hysteresis voltage of an open drain or open collector Reset IC using an external circuit.

Method for expanding hysteresis width

In models with the open drain output configuration, the hysteresis width can be expanded by connecting the pull-up resistance R_L to VDD and connecting the resistance R_{VDD} between VDD and VIN. This method is not applicable to models with the CMOS output.

(This method is not recommended for the BU48xx and BU42xx series with open drain output since a large voltage drop is caused by R_{VDD} due to an inrush current during the output switching.)

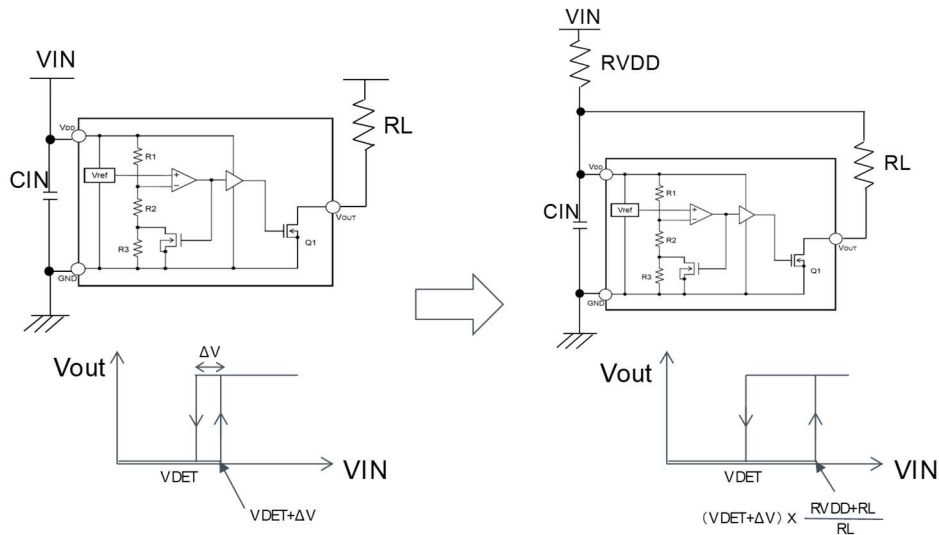


Figure 1. Method for expanding hysteresis width of open drain output Reset IC

Calculation of hysteresis width

A circuit configuration as shown in the right side of Figure 1 can be used to expand the hysteresis voltage. When VDD is normal, transistor Q1 is OFF, the output impedance is high, and the reset output V_{OUT} is “H” for the open drain output. Since the current consumption by the IC is sufficiently small and no current flows through R_L , no voltage drop is caused by R_{VDD} , resulting in $V_{IN} = V_{DD}$. Thus, when the power supply voltage V_{IN} is reduced, the detection voltage is the normal V_{DET} .

If the power supply voltage V_{IN} is V_{DET} or lower, V_{OUT} is at the “L” level. Assume that the ON-resistance of Q1 is negligible relative to R_L and the “L” level \approx ground = 0 V.

The voltage applied on VDD is the voltage divided by the resistances R_{VDD} and R_L as follows: $V_{DD} = V_{IN} \times R_L / (R_{VDD} + R_L) \dots(1)$

When the hysteresis voltage ΔV_{DET} described in the data sheet is 5% (typ) of V_{DET} , the reset release voltage based on VDD is described as follows: $V_{DD} = V_{DET} + \Delta V_{DET} = 1.05 \times V_{DET} \dots(2)$

Substituting the right side of (2) for VDD in (1) results in $1.05 \times V_{DET} = V_{IN} \times R_L / (R_{VDD} + R_L)$

The release voltage viewed from VIN is $V_{IN} = 1.05 \times V_{DET} \times (RVDD + RL) / RL \dots(3)$.

Therefore, the release voltage can be expanded by an amount of $(RVDD + RL) / RL$ from the normal value.

The hysteresis voltage after the modification ΔV_{new} is described as follows:

$$\Delta V_{new} = 1.05 \times V_{DET} \times (RVDD + RL) / RL - V_{DET} \dots(4)$$

Variation range of reset release voltage

Release voltage (typ) : $V_{IN} = 1.05 \times V_{DET} \times (RVDD + RL) / RL \dots(3)$

VDET variation: $\pm 1\%$ at 25°C

VDET temperature coefficient: ± 360 ppm/ $^\circ\text{C}$ (Max)

When the ambient temperature is between T_a (Min) [$^\circ\text{C}$] and T_a (Max) [$^\circ\text{C}$]

Variation range of VDET is

$$V_{DET} (\text{Max}) = V_{DET} \times 1.01 + V_{DET} \times 1.01 \times |T_a (\text{Max}) - 25| \times (360 / 1,000,000)$$

$$V_{DET} (\text{Min}) = V_{DET} \times 0.99 - V_{DET} \times 0.99 \times |T_a (\text{Min}) - 25| \times (360 / 1,000,000)$$

Taking into account the variation ranges of ΔV_{DET} at all operating temperatures, 3% (Min) and 8% (Max), the variation range of the release voltage is derived as follows from (3)

$$V_{IN} (\text{Max}) = 1.08 \times \{V_{DET} \times 1.01 + V_{DET} \times 1.01 \times |T_a (\text{Max}) - 25| \times (360 / 1,000,000)\} \times (RVDD + RL) / RL$$

$$V_{IN} (\text{Min}) = 1.03 \times \{V_{DET} \times 0.99 - V_{DET} \times 0.99 \times |T_a (\text{Min}) - 25| \times (360 / 1,000,000)\} \times (RVDD + RL) / RL$$

This is the result obtained.

Setting for constants of hysteresis width expansion circuit

Set C_{IN} to a value of $0.1 \mu\text{F}$ or larger.

The recommended range for resistance is $RVDD \leq 15\text{k}\Omega$

The recommended range for the total output pull-up resistance $RL' = RVDD + RL$ is $10\text{k}\Omega \leq RL' \leq 1\text{M}\Omega$

(BD48xx/BD48Exx/BD48Kxx/BD48Lxx/BD52xx)

$50\text{k}\Omega \leq RL' \leq 1\text{M}\Omega$

(BD52Exx/BD52xx-2C/BD45xx/BD45Exx/BD45Kxx/BD45xxL)

Since a higher value of $RVDD$ may cause an oscillation, keep $RVDD$ as low as possible.

However, a resistance of $15\text{k}\Omega$ or higher may be used depending on the V_{DD} waveform of the set.

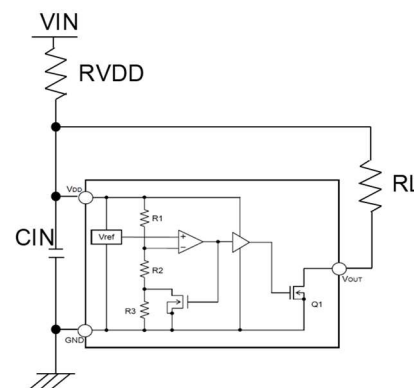


Figure 2. Hysteresis expansion circuit

After setting the constants, confirm the margin as follows.

Keep the value of C_{IN} fixed and set $RVDD$ and RL to values twice those of their target values.

If no issue is found in the evaluation within the set temperature range, the reset IC can be considered as usable with the target values.

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