Voltage Detector (Reset IC) Series

# Method for Expanding Hysteresis Width

This application note explains a method to modify the hysteresis voltage of an open drain or open collector Reset IC using an external circuit.

## Method for expanding hysteresis width

In models with the open drain output configuration, the hysteresis width can be expanded by connecting the pull-up resistance RL to VDD and connecting the resistance RVDD between VDD and VIN. This method is not applicable to models with the CMOS output.

(This method is not recommended for the BU48xx and BU42xx series with open drain output since a large voltage drop is caused by RVDD due to an inrush current during the output switching.)

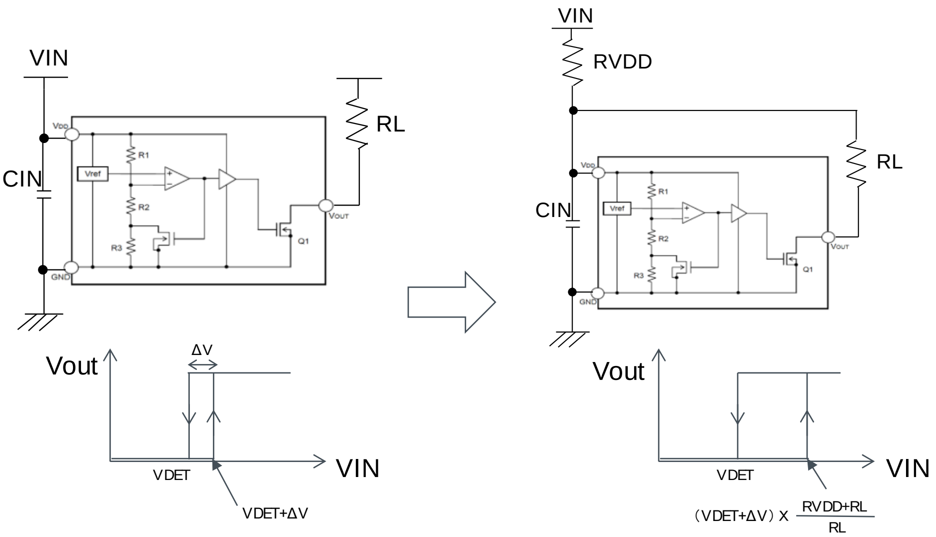


Figure 1. Method for expanding hysteresis width of open drain output Reset IC

## Calculation of hysteresis width

A circuit configuration as shown in the right side of Figure 1 can be used to expand the hysteresis voltage. When VDD is normal, transistor Q1 is OFF, the output impedance is high, and the reset output $V_{OUT}$ is “H” for the open drain output. Since the current consumption by the IC is sufficiently small and no current flows through RL, no voltage drop is caused by RVDD, resulting in VIN = VDD. Thus, when the power supply voltage VIN is reduced, the detection voltage is the normal VDET.

If the power supply voltage VIN is VDET or lower, $V_{OUT}$ is at the “L” level. Assume that the ON-resistance of Q1 is negligible relative to RL and the “L” level ≈ ground = 0 V.

The voltage applied on VDD is the voltage divided by the resistances RVDD and RL as follows: VDD = VIN × RL/(RVDD + RL) ...(1)

When the hysteresis voltage ΔVDET described in the data sheet is 5% (typ) of VDET, the reset release voltage based on VDD is described as follows: VDD = VDET + ΔVDET = 1.05 × VDET ...(2)

Substituting the right side of (2) for VDD in (1) results in 1.05 × VDET = VIN × RL/(RVDD + RL)

The release voltage viewed from VIN is VIN = 1.05 × VDET × (RVDD + RL)/RVDD ...(3).

Therefore, the release voltage can be expanded by an amount of (RVDD + RL)/RL from the normal value.

The hysteresis voltage after the modification $\Delta V_{new}$ is described as follows:

$\Delta V_{new}$ = 1.05 × VDET × (RVDD+RL)/RVDD – VDET ...(4)

## Variation range of reset release voltage

Release voltage (typ) :VIN = 1.05 × VDET × (RVDD + RL)/RVDD ...(3)

VDET variation: ±1% at 25°C

VDET temperature coefficient: ±360 ppm/°C (Max)

When the ambient temperature is between Ta (Min) [°C] and Ta (Max) [°C]

Variation range of VDET is

VDET (Max) = VDET × 1.01 + VDET × 1.01 × |Ta (Max) - 25| × (360/1,000,000)

VDET (Min) = VDET × 0.99 - VDET × 0.99 × |Ta (Min) - 25| × (360/1,000,000)

Taking into account the variation ranges of ΔVDET at all operating temperatures, 3% (Min) and 8% (Max), the variation range of the release voltage is derived as follows from (3)

VIN (Max) = 1.08 × {VDET × 1.01 + VDET × 1.01 × |Ta (Max) - 25| × (360/1,000,000)} × (RVDD + RL)/RVDD

VIN (Min) = 1.03 × {VDET × 0.99 - VDET × 0.99 × |Ta (Min) - 25| × (360/1,000,000)} × (RVDD + RL)/RVDD

This is the result obtained.

## Setting for constants of hysteresis width expansion circuit

Set CIN to a value of 0.1 µF or larger.

The recommended range for resistance is RVDD ≤ 15kΩ

The recommended range for the total output pull-up resistance RL' = RVDD + RL is

10kΩ ≤ RL' ≤ 1MΩ

(BD48xx/BD48Exx/BD48Kxx/BD48Lxx/BD52xx)

50kΩ ≤ RL' ≤ 1MΩ

(BD52Exx/BD52xx-2C/BD45xx/BD45Exx/BD45Kxx/BD45xxL)

Since a higher value of RVDD may cause an oscillation, keep RVDD as low as possible.

However, a resistance of 15kΩ or higher may be used depending on the VDD waveform of the set.

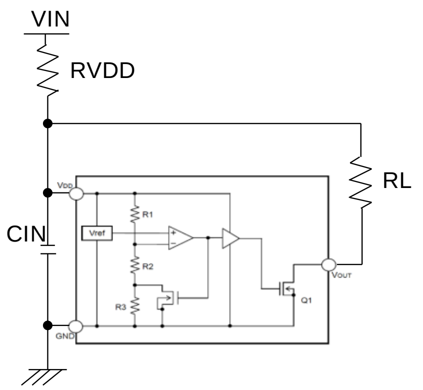


Figure 2. Hysteresis expansion circuit

After setting the constants, confirm the margin as follows.

Keep the value of CIN fixed and set RVDD and RL to values twice those of their target values.

If no issue is found in the evaluation within the set temperature range, the reset IC can be considered as usable with the target values.

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