Voltage Detector (Reset IC) Series

Resistance Division and Inrush Current

If the detection voltage of the voltage to be monitored (VIN) is higher than the detection voltage of the reset IC (VDET), VIN may be divided by the resistance and supplied to the reset IC as VDD. This application note summarizes the precautions when utilizing this resistance division method.

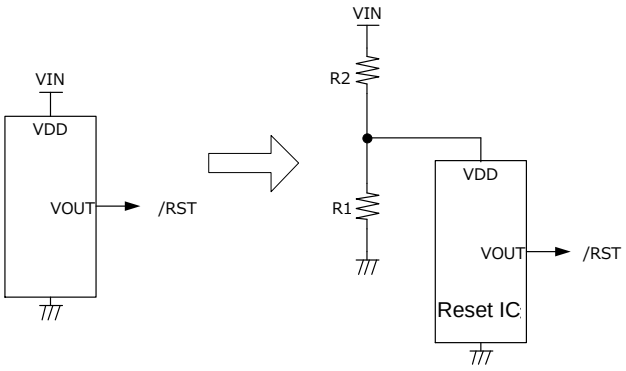


Figure 1. Example of resistance division for reset IC

Location of inrush current occurrence and power supply voltage

In a CMOS inverter, generally, PMOS and NMOS are simultaneously ON near the threshold for the output H/L switching.

In a reset IC, an inrush current occurs in the inverter on the output front stage (inside the blue dotted circle) near the release voltage.

The inrush current flows from VIN to R2 and the voltage on the power supply terminal of the reset IC (VDD) drops.

As a result, even when VIN has reached the release voltage, VDD may still be below the release voltage and VOUT may not be switched to H.

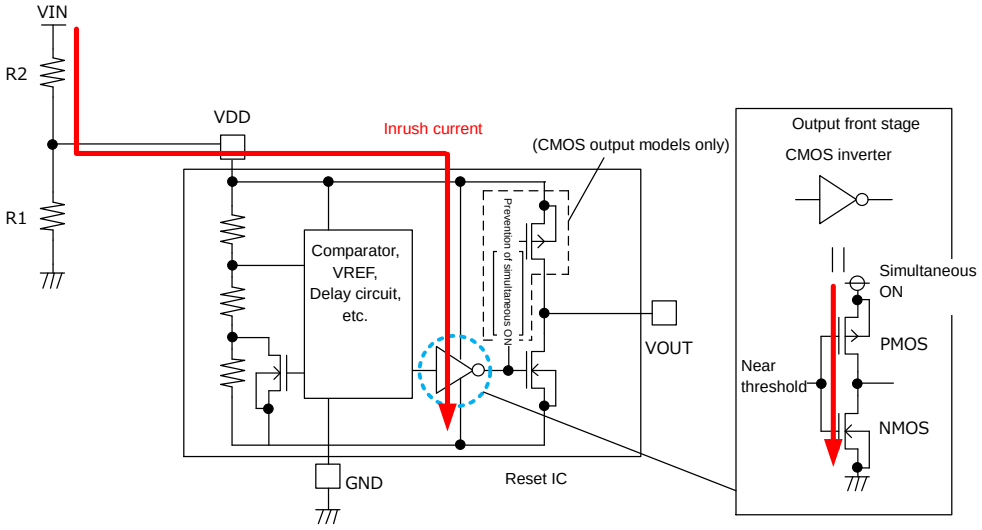


Figure 2. Location of inrush current occurrence in reset IC

Voltage drop and unstable operation caused by inrush current (1)

When the inrush current is large, an oscillation of the VDD voltage occurs near the release voltage following the sequence below.

(1) When the voltage approaches the release voltage, the amount of inrush current increases.

(2) R2 causes a voltage drop in proportion to the amount of inrush current.

(3) The VDD voltage drops along with (2).

(4) Since the VDD voltage drops, the amount of inrush current decreases.

(5) Since the amount of inrush current decreases, the VDD voltage increases.

(6) Returns to (1).

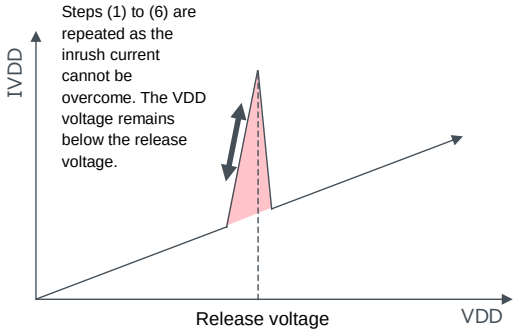
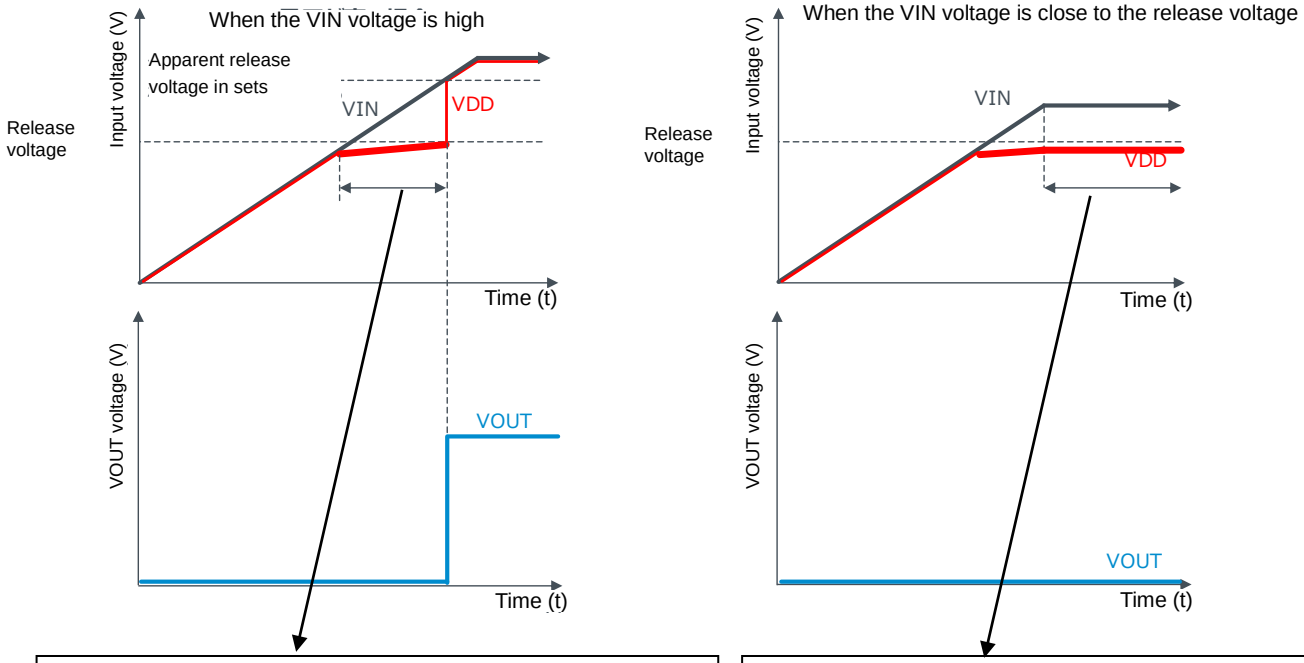


Figure 3. Inrush current near release voltage

Voltage drop and unstable operation caused by inrush current (2)



In this section, it appears that VDD stops increasing near the release voltage. However, VDD is still increasing slightly with VIN while oscillating slightly.
When VDD exceeds the release voltage, the inrush current disappears. Therefore, it appears that the state has suddenly changed from a VDD clamped state to VOUT = H and VDD ≈ VIN.
It also appears that the release voltage for VIN is higher than the setting.

When the VIN voltage remains at a value that keeps the VDD voltage in this section, the VDD voltage cannot exceed the release voltage and VOUT = L is maintained.
It appears as if no reset release is performed even when the input voltage exceeds the release voltage for VIN.

Figure 4. Effect of inrush current on rise waveform of power supply

Countermeasure using input capacitor

When the capacitor CIN is located between the VDD terminal and ground, the electric charge that is necessary to increase the voltage over the release voltage is compensated and the comparator can reach a state above the release voltage.

After that, the voltage drop of VDD disappears as the inrush current disappears, resulting in VDD ≈ VIN.

Therefore, as the value of CIN increases, it becomes more effective.

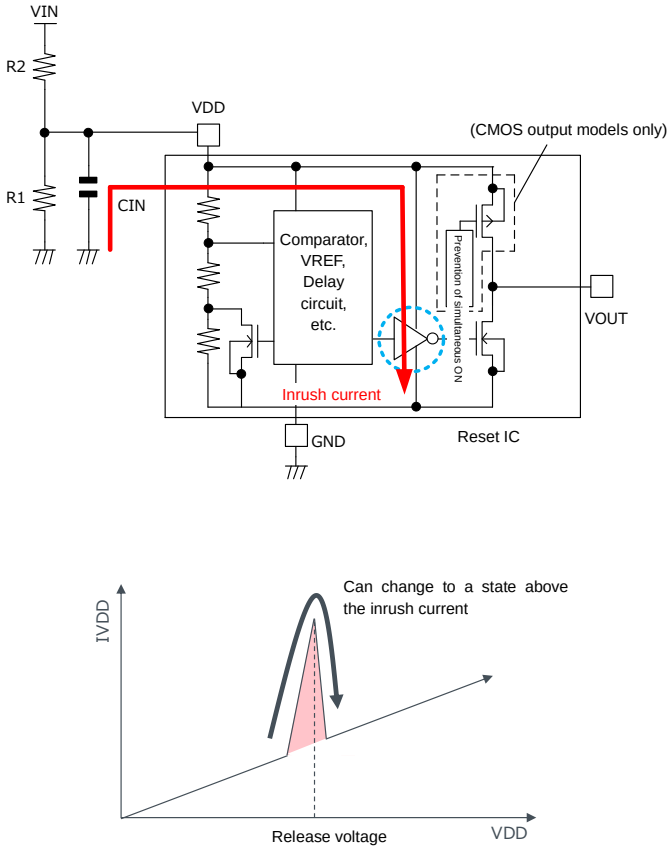


Figure 5. Reduction of inrush current effect by CIN capacitor

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