Automotive 45 V, 500 mA Fixed Output Nano Cap™ LDO Regulators with WDT and Voltage Supervisor (Reset)

BD9xxF5-C Series

General Description

The BD9xxF5-C series are linear regulators using the Nano Cap™ topology(Note 1) designed as low current consumption components for power supplies in various automotive applications requiring a direct connection to the battery. It integrates a reset block (RESET) that monitors the input voltage of the microcomputer and a watchdog timer block (WDT) that monitors the clock signal of the microcomputer.

The RESET delay time and WDT monitor time can be adjusted through an external capacitor.

These products are designed for an absolute maximum input voltage of 45 V and to operate at up to 500 mA of current load with a low current consumption of 32 µA (Typ). Output voltage regulation is guaranteed to be highly accurate at ±2 %.

An output capacitor of 470 nF (Typ) or more can be used for this product series and it has excellent transient characteristics even with small output capacitance.

It has an output shutdown function. A logical HIGH at the EN pin turns on the product output and a logical LOW disable the output.

The products feature an integrated Over Current Protection to protect the device from damage caused by a short circuit or an overload. These products also integrate Thermal Shutdown Protection to avoid damage by overheating and Under Voltage Lock Out to avoid false operation at low input voltage.

Furthermore, low ESR ceramic capacitors are sufficient for phase compensation.

Additionally, this IC functions as a ComfySIL™(Note 2) compatible product, to support functional analysis related to functional safety.

(Note 1) Nano Cap™ is a combination of technologies which allow stable operation even if output capacitance is connected with the range of nF units.

(Note 2) ComfySIL™ is awarded to products that conform to the ComfySIL™ concept for functional safety in the industrial equipment and automotive markets.

Key Specifications

- Wide Temperature Range (Tj): -40 °C to +150 °C
- Wide Operating Input Range: 3 V to 42 V
- Output Voltage: 3.3 V / 5.0 V
- Low Current Consumption: 32 µA (Typ)
- Output Current Capability: 500 mA
- High Output Voltage Accuracy: ±2.0 %
- RESET Detection Voltage Accuracy: ±2.0 %

Features

- Nano Cap™ Topology(Note 1)
- QuiCur™ Topology(Note 3)
- AEC-Q100 Qualified(Note 4)
- Functional safety supportive automotive products
- Integrated Power ON and Under-Voltage Detection Reset
- Integrated Watchdog Timer
- Adjustable Reset Delay Time and Watchdog Monitor Time by External Capacitor
- Over Current Protection (OCP)
- Thermal Shutdown Protection (TSD)
- Under Voltage Lock Out (UVLO)

(Note 3) QuiCur™ is a combination of technologies that provides high-speed load response.

(Note 4) Grade 1

Applications

- Automotive (Power Train, Body ECU)
- Car Infotainment system
- Consumer applications, Industrial applications, etc.

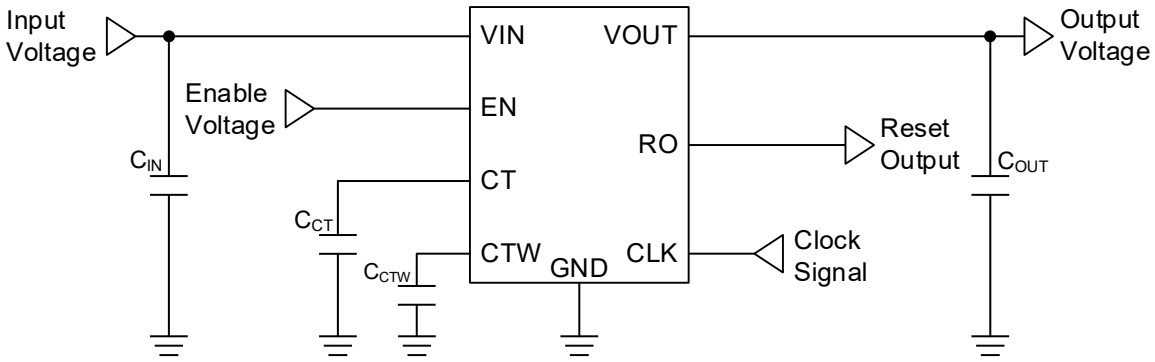
Package

Package	W (Typ) x D (Typ) x H (Max)
■ HTSOP-J8	4.9 mm x 6.0 mm x 1.0 mm

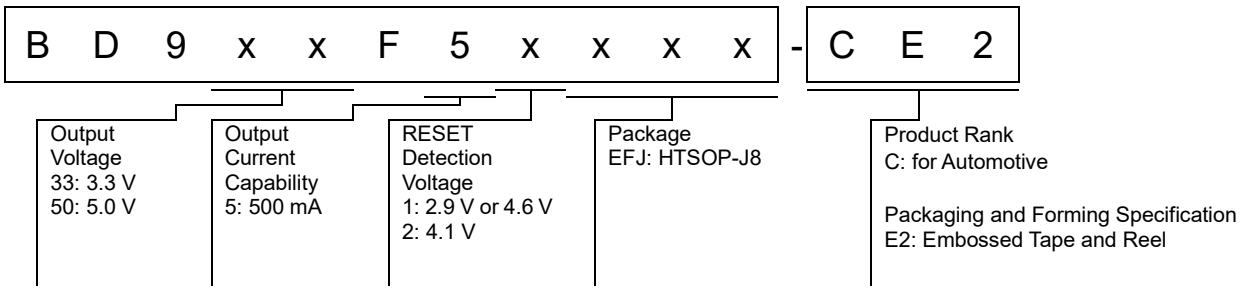
Typical Application Circuits

External Components
Capacitors: 0.1 µF ≤ C_{IN} (Min), 0.23 µF ≤ C_{OUT} (Min)*(Note 1)*, 0.001 µF ≤ C_{CT} ≤ 47 µF, 0.00047 µF ≤ C_{CTW} ≤ 10 µF

(Note 1) Ceramic capacitors are recommended for the output capacitor. Electrolytic capacitors and tantalum capacitors can also be used. But when using electrolytic capacitors or tantalum capacitors with large ESR (> 400 mΩ), a ceramic capacitor of at least 0.23 µF must be connected in parallel near the VOUT pin.



Ordering Information

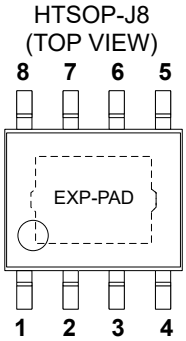


Lineup

Output Voltage	Output Current Capability	RESET Detection Voltage	WDT Function	Package	Ordering
3.3 V	500 mA	2.9 V	available	HTSOP-J8	BD933F51EFJ-CE2
5.0 V		4.1 V	available	HTSOP-J8	BD950F52EFJ-CE2
		4.6 V	available	HTSOP-J8	BD950F51EFJ-CE2

Contents

Pin Configurations



Pin Descriptions

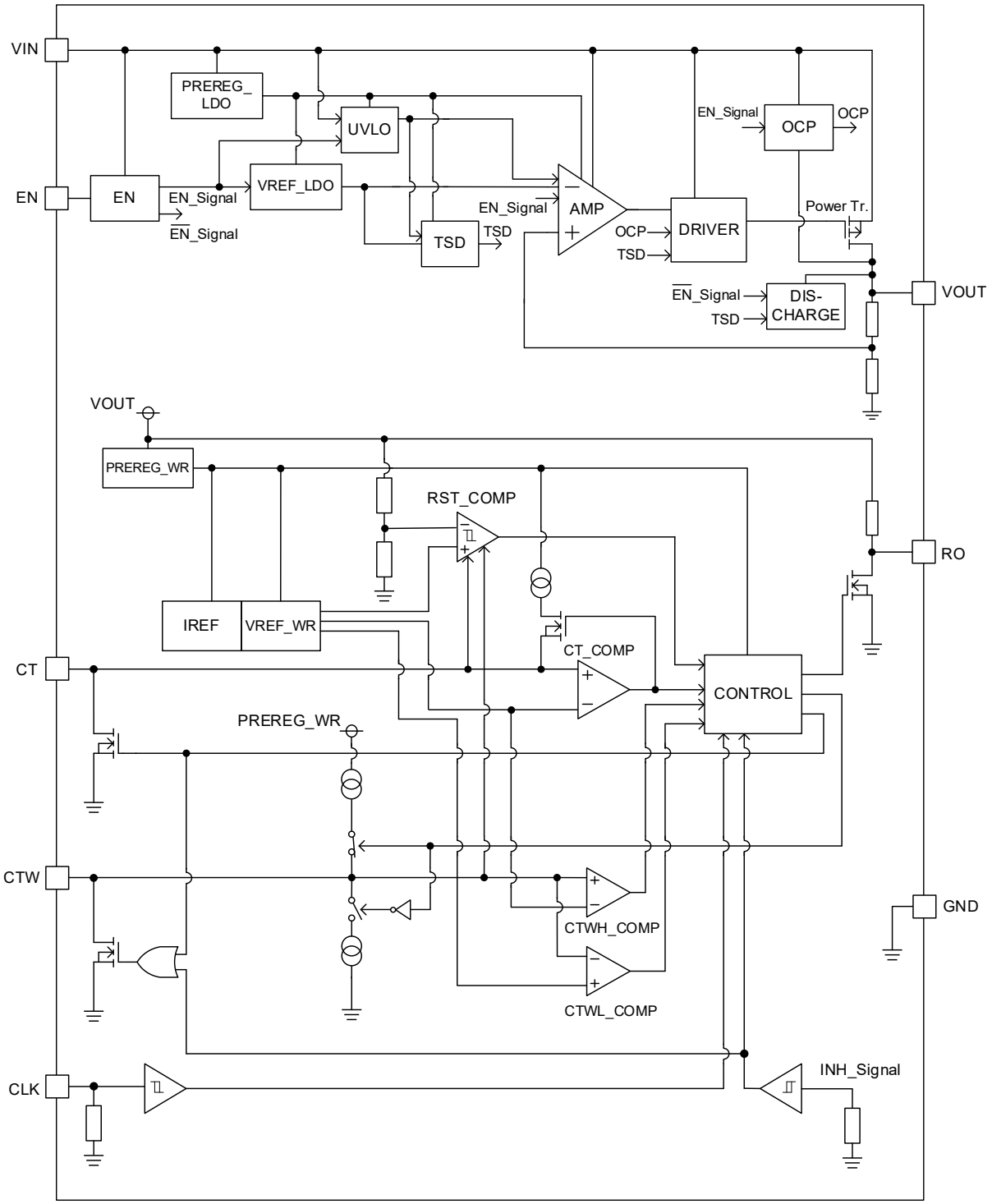
(HTSOP-J8) BD933F51EFJ-C, BD950F51EFJ-C, BD950F52EFJ-C

Pin No.	Pin Name	Function	Descriptions
1	VIN	Input Supply Voltage Pin	Pin for application of Input Voltage Supply. Set a capacitor with a capacitance of 0.1 µF (Min) or higher between the VIN pin and the GND pin. The selection method is described in **Selection of External Components**. If the inductance of power supply line is high, adjust input capacitor value.
2	EN	Control Output ON / OFF Pin	A logical HIGH (V_{EN} ≥ 1.5 V) at the EN pin enables the device and a logical LOW (V_{EN} ≤ 0.6 V) at the EN pin disables the device. Although the output is turned off when the EN pin is open, it is recommended to connect it to the GND pin via a low impedance path to prevent incorrect operation.
3	CT	Reset Delay Time Setting Pin	This pin sets the RESET Delay Time. It is necessary to connect a capacitor ranging from 0.001 µF (Min) to 47 µF (Max) in value between the CT pin and the GND pin. If setting the RESET delay time is not necessary, the CT pin can be used open. For detailed information, refer to the **Application Circuit Examples**.
4	CTW	WDT Monitor Time Setting Pin	This pin sets the WDT Monitor Time. It is necessary to connect a capacitor ranging from 0.00047 µF (Min) to 10 µF (Max) in value between the CTW pin and the GND pin. If the WDT is not used and only the LDO and RESET functions are used, short the CTW pin to the GND pin. For detailed information, refer to the **Application Circuit Examples**.
5	CLK	Clock Signal Input Pin	This pin is an input for CLK signal*(Note 1)* from Microcomputer. Pull-down resistors are implemented within the IC. If this pin is open, the input state is kept LOW.
6	GND	Ground Pin	This pin should be connected to the lowest potential.
7	RO	RESET Output Pin	This is the output for RESET block. It is pulled up internally to the VOUT pin via a 30 kΩ(Typ) resistance. It is also possible to connect additional pull-up resistors of at least 3 kΩ (Min) externally.
8	VOUT	Output Voltage Pin	Outputs the set voltage. Set a capacitor with at least 0.23 µF (Min) this pin and the GND pin. The selection method is described in **Selection of External Components**.
-	EXP-PAD	Heat Dissipation	It is recommended to connect EXP-PAD on the back side to an external ground pattern in the PCB in order to improve heat dissipation.

(Note 1) CLK Input High/Low Level Voltage should be supplied to the CLK pin as described in the Electrical Characteristics.
It is not allowed to keep the value at the midpoint voltage potential which to it may accidentally switch between High and Low.

Block Diagram

BD933F51EFJ-C, BD950F51EFJ-C, BD950F52EFJ-C



Description of Blocks

Block Name	Function	Description of Blocks
EN	Enable Input	A logical HIGH (V_{EN} ≥ 1.5 V) at the EN pin enables the device and a logical LOW (V_{EN} ≤ 0.6 V) at the EN pin disables the device.
PREREG_LDO	Internal Power Supply	Power supply for internal circuit of LDO block.
TSD	Thermal Shutdown Protection	When the maximum power dissipation or when the junction temperature rises and the chip temperature (Tj) exceeds the set thermal protection temperature (Typ: 175 °C), the TSD protection circuit detects this and forces the gate of output MOSFET to turn off in order to protect the product from overheating. When the junction temperature decreases a set temperature below this protection temperature, the thermal Shutdown protection is released and the output turns on automatically.
VREF_LDO	Reference Voltage	Generates the reference voltage used in the internal circuit of the LDO block.
AMP	Error Amplifier	The fixed output voltage product compares a sampled voltage obtained by dividing the output voltage via a resistor network with the reference voltage and controls the output power transistor via the DRIVER.
DRIVER	Output MOSFET Driver	Drives the output MOSFET.
OCP	Over Current Protection	When the output current increases above the maximum rated output current, it is limited by Over Current Protection (Typ: 1000 mA) to protect the device from damage caused by an over current. While this block is operational, the output voltage may decrease because the output current is limited. When the abnormal state is removed and the output current value returns to normal, the output voltage also returns to its normal state.
DISCHARGE	Output Discharge	The output pin is discharged by through an internal resistance when EN = LOW input or TSD is detected.
UVLO	Under Voltage Lock Out	The Under Voltage Lock Out protection detects when V_{IN} voltage goes below 2.4 V (Typ) and forces AMP to turn off to avoid any false operation at low input voltage.
PREREG_WR	Internal Power Supply	Power Supply for Internal circuit for WDT and RESET block.
IREF	Reference Current	Generates for the Reference Current for the Internal Circuit of the WDT and RESET block.
VREF_WR	Reference Voltage	Generates for the Reference Voltage for the WDT and RESET block.
RST_COMP	Comparator	Compares the VOUT voltage and the Reference Voltage and outputs a signal to the CONTROL block.
CT_COMP	Comparator	Compares the CT voltage and the Reference Voltage and outputs a signal to the CONTROL block.
CTWH_COMP	Comparator	Compares the CTW voltage and the Reference Voltage and outputs the CTW Upper-side Threshold signal to the CONTROL block.
CTWL_COMP	Comparator	Compares the CTW voltage and the Reference Voltage and outputs the CTW Lower-side Threshold signal to the CONTROL block.
CONTROL	Control function	Controls Reset and Watchdog operation depending on each state of VOUT voltage, CT voltage, CTW voltage, and CLK signal.

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage*(Note 1)*	V_{IN}	-0.3 to +45.0	V
EN Pin Voltage	V_{EN}	-0.3 to +45.0	V
VOUT Pin Voltage	V_{OUT}	-0.3 to +20.0 (≤ V_{IN} + 0.3)	V
CT Pin Voltage	V_{CT}	-0.3 to +20.0 (≤ V_{OUT} + 0.3)	V
CTW Pin Voltage	V_{CTW}	-0.3 to +7.0 (≤ V_{OUT} + 0.3)	V
CLK Pin Voltage	V_{CLK}	-0.3 to +7.0 (≤ V_{OUT} + 0.3)	V
RO Pin Voltage	V_{RO}	-0.3 to +20.0	V
Junction Temperature Range	Tj	-40 to +150	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C
ESD Withstand Voltage (HBM)*(Note 2)*	V_{ESD_HBM}	±2000	V
ESD Withstand Voltage (CDM)*(Note 3)*	V_{ESD_CDM}	±750	V

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, to protect the IC from being operated outside the absolute maximum ratings.

Caution 2: If the maximum junction temperature rating is exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance and power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

(Note 1) Do not exceed Tjmax.
The start-up orders of power supply (V_{IN}) and the V_{EN} do not matter if the voltage is within the operation power supply voltage range.

(Note 2) ESD susceptibility Human Body Model “HBM”; based on AEC-Q100-002 (1.5 kΩ, 100 pF).

(Note 3) ESD susceptibility Charged Device Model “CDM”; base on AEC-Q100-011.

Thermal Resistances(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
HTSOP-J8				
Junction to Ambient	θ_{JA}	132.6	28.3	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	14	5	°C/W

(Note 1) Based on JESD51-2A (Still-Air), using a BD950F51EFJ-C.
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 5) This thermal via connects with the copper pattern of 1,2,4 layers. Placement follows the land pattern.

Operating Conditions (-40 °C ≤ Tj ≤ +150 °C)

Parameter	Symbol	Min	Max	Unit
Input Voltage *(Note 1) (Note 2)*	V_{IN}	4.6	42.0	V
		V_{OUT} (Max) + ΔV_D (Max)	42.0	V
Start-Up Voltage	$V_{IN\ Start\text{-}Up}$	3.0	-	V
Enable Input Voltage	V_{EN}	0	42.0	V
Output Current	I_{OUT}	0	500	mA
Input Capacitor *(Note 3) (Note 4)*	C_{IN}	0.1	-	µF
Output Capacitor *(Note 4)*	C_{OUT}	0.23	470	µF
Output Capacitor Equivalent Series Resistance *(Note 5)*	ESR (C_{OUT})	-	400	mΩ
CT Capacitor	C_{CT}	0.001	47	µF
CTW Capacitor	C_{CTW}	0.00047	10	µF
RO External Pull-up Resistor to VOUT *(Note 6)*	$R_{RO,ext}$	3	-	kΩ
Operating Ambient Temperature	Ta	-40	+125	°C

(Note 1) Consider that the output voltage would be dropped (Dropout voltage ΔV_D) by the output current.
(Note 2) Apply 4.6 V or V_{OUT} (Max) + ΔV_D (Max), whichever is higher.
(Note 3) If the inductance of power supply line is high, please adjust input capacitor value to lower the input impedance.
A lower input impedance can cause the IC to operate in its ideal characteristics.
It also has the effect of preventing voltage drop at the input line.
(Note 4) Set capacitor value which do not fall below the minimum value. This value also has to consider the temperature characteristics and DC device characteristics of the capacitor.
(Note 5) It is recommended to use ceramic capacitors that have low ESR characteristics for output phase compensation.
In case of using electrolytic capacitor or tantalum capacitor with large ESR (> 400 mΩ), note that ceramic capacitor of at least 0.23 µF must be connected in parallel near the VOUT pin.
(Note 6) There is a 30 kΩ (typ) pull-up resistor between RO and VOUT inside the IC. Therefore, it can be used without an external pull-up resistor.

Electrical Characteristics

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND *(Note 1)*
Typical values are defined at Tj = 25 °C, V_{IN} = 13.5 V

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Shutdown Current	I_{SHUT}	-	1.0	5.0	µA	V_{EN} = 0 V, Tj ≤ 125 °C
Circuit Current (WDT OFF)	I_{CC1}	-	32	60	µA	I_{OUT} = 0 mA, Tj ≤ 125 °C
	I_{CC2}	-	32	65	µA	I_{OUT} = 0 mA, Tj ≤ 150 °C
Circuit Current (WDT ON)	I_{CC3}	-	35	65	µA	I_{OUT} = 0 mA, Tj ≤ 125 °C C_{CT} = 0.001 µF, C_{CTW} = 0.00047 µF f_{CLK} = 1 kHz
	I_{CC4}	-	35	70	µA	I_{OUT} = 0 mA, Tj ≤ 150 °C C_{CT} = 0.001 µF, C_{CTW} = 0.00047 µF f_{CLK} = 1 kHz
Output Voltage *(Note 2)*	V_{OUT}	3.234	3.300	3.366	V	4.6 V ≤ V_{IN} ≤ 42 V, 0 mA ≤ I_{OUT} ≤ 500 mA
Output Voltage *(Note 3)*	V_{OUT}	4.900	5.000	5.100	V	5.85 V ≤ V_{IN} ≤ 42 V, 0 mA ≤ I_{OUT} ≤ 300 mA, or 6.35 V ≤ V_{IN} ≤ 42 V, 0 mA ≤ I_{OUT} ≤ 500 mA
Dropout Voltage	ΔV_{D1}	-	400	900	mV	V_{IN} = 3.135 V, I_{OUT} = 300 mA
	ΔV_{D2}	-	700	1500	mV	V_{IN} = 3.135 V, I_{OUT} = 500 mA
	ΔV_{D3}	-	380	750	mV	V_{IN} = 4.75 V, I_{OUT} = 300 mA
	ΔV_{D4}	-	650	1250	mV	V_{IN} = 4.75 V, I_{OUT} = 500 mA
Ripple Rejection *(Note 4)*	R.R.	-	65	-	dB	f = 1 kHz, V_{Ripple} = 1 Vrms I_{OUT} = 10 mA
Line Regulation	Reg.I	-	0.1	0.3	%	V_{OUT} + 1.5 V ≤ V_{IN} ≤ 42 V
Load Regulation	Reg.L	-	0.1	0.5	%	0 mA ≤ I_{OUT} ≤ 500 mA

(Note 1) Short the CTW pin to GND pin to disable the WDT function.
(Note 2) Applicable for product with BD933F51EFJ-C.
(Note 3) Applicable for product with BD950F51EFJ-C, BD950F52EFJ-C.
(Note 4) Not all devices are measured for shipment.

Electrical Characteristics – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND*(Note 1)*
Typical values are defined at Tj = 25 °C, V_{IN} = 13.5 V

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
UVLO Fall Threshold	V_{UVLOF}	1.8	2.4	2.8	V	V_{IN} falling
UVLO Rise Threshold	V_{UVLOR}	2.0	2.6	3.0	V	V_{IN} rising
UVLO Hysteresis Voltage	$V_{UVLOHYS}$	-	0.2	-	V	-
Over Current Protection	I_{OCP}	501	1000	1300	mA	V_{OUT} = 0 V
Thermal Shutdown Temperature	T_{TSD}	151	175	-	°C	-
Thermal Shutdown Hysteresis Temperature	T_{TSDHYS}	-	15	-	°C	-
Enable ON Threshold Voltage	V_{ENTH}	0.70	1.10	1.50	V	V_{EN} rising
Enable OFF Threshold Voltage	V_{ENTL}	0.60	0.90	1.30	V	V_{EN} falling
Enable Hysteresis Voltage	V_{ENHYS}	-	0.18	-	V	-
Enable Bias Current	I_{EN}	-	4	8	µA	V_{EN} = 5 V
VOUT Discharge Resistance	R_{DSC}	2.6	6.5	11.0	kΩ	V_{EN} = 0 V, V_{OUT} = 5 V

(Note 1) Short the CTW pin to GND pin to disable the WDT function.

Electrical Characteristics – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = V_{OUT} = 5.0 V, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, C_{CT} = 0.01 µF, C_{CTW} = 0.0047 µF

Typical values are defined at Tj = 25 °C, V_{IN} = V_{OUT} = 5.0 V

Parameter		Symbol	Limits			Unit	Conditions
			Min	Typ	Max		
RO Pin Leakage Current		I_{LEAK}	-	-	1	µA	V_{OUT} = V_{RO} = 5.0 V *(Note 1)*
RO Pin Current Capability 1		I_{OL1}	0.4	-	-	mA	V_{OUT} = 1.0 V, V_{RO} = 0.5 V
RO Pin Current Capability 2		I_{OL2}	2.0	-	-	mA	V_{OUT} = 2.0 V, V_{RO} = 0.5 V
RO Low Voltage		V_{ROL}	-	-	0.4	V	V_{OUT} ≥ 1 V, $R_{RO,ext}$ ≥ 3 kΩ
RESET Detection Voltage	2.9 V *(Note 2)*	V_{DET}	V_{DET} (Typ) x (-2 %)	2.900	V_{DET} (Typ) x (+2 %)	V	-
	4.1 V *(Note 3)*	V_{DET}	V_{DET} (Typ) x (-2 %)	4.100	V_{DET} (Typ) x (+2 %)	V	-
	4.6 V *(Note 4)*	V_{DET}	V_{DET} (Typ) x (-2 %)	4.600	V_{DET} (Typ) x (+2 %)	V	-
RESET Detection Hysteresis Voltage	2.9 V *(Note 2)*	V_{RHY}	V_{RHY} (Typ) x (-45 %)	104	V_{RHY} (Typ) x (+45 %)	mV	-
	4.1 V *(Note 3)*	V_{RHY}	V_{RHY} (Typ) x (-45 %)	148	V_{RHY} (Typ) x (+45 %)	mV	-
	4.6 V *(Note 4)*	V_{RHY}	V_{RHY} (Typ) x (-45 %)	166	V_{RHY} (Typ) x (+45 %)	mV	-
RO Internal Pull-up Resistor to VOUT		$R_{RO,int}$	18	30	46	kΩ	-

(Note 1) V_{RO} is the voltage applied to the RO pin.
(Note 2) Applicable for product with BD933F51EFJ-C.
(Note 3) Applicable for product with BD950F52EFJ-C.
(Note 4) Applicable for product with BD950F51EFJ-C.

Electrical Characteristics – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = V_{OUT} = 5.0 V, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, C_{CT} = 0.01 µF, C_{CTW} = 0.0047 µF

Typical values are defined at Tj = 25 °C, V_{IN} = V_{OUT} = 5.0 V

Parameter	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
CT Threshold	V_{CTTH}	-	0.9	-	V	-
CT Charge Current	I_{CT_C}	-	1.3	-	µA	V_{CT} = 0.5 V
CTW Upper-side Threshold	V_{CTWH}	-	0.9	-	V	-
CTW Lower-side Threshold	V_{CTWL}	-	0.3	-	V	-
CTW Charge Current	I_{CTW_C}	-	0.3	-	µA	V_{CTW} = 0.2 V
CTW Discharge Current	I_{CTW_D}	-	0.9	-	µA	V_{CTW} = 1.0 V
Delay Time L→H	t_D	5.5	6.9	8.3	ms	C_{CT} = 0.01 µF *(Note 1)*
WDT Monitor Time	t_{WH}	7.5	9.4	11.5	ms	C_{CTW} = 0.0047 µF *(Note 1)*
WDT Reset Time	t_{WL}	2.5	3.2	3.9	ms	C_{CTW} = 0.0047 µF *(Note 1)*
CLK Input Current	I_{CLK}	-	0.3	2.0	µA	V_{CLK} = 5.0 V
CLK Input Pulse Width	t_{PCLK}	0.5	-	-	µs	-
CLK Input High Level Voltage	V_{HCLK}	V_{OUT} x 0.8	-	V_{OUT}	V	-
CLK Input Low Level Voltage	V_{LCLK}	0	-	V_{OUT} x 0.2	V	-

(Note 1) t_D, t_{WH}, and t_{WL} can be adjustable by changing the CT and CTW pins capacitance value.

t_D [s] = 0.69 x C_{CT} [F] x 10^6

t_{WH} [s] = 2 x C_{CTW} [F] x 10^6

t_{WL} [s] = 0.67 x C_{CTW} [F] x 10^6

C_{CT} and C_{CTW} can be used even if they are below the minimum operating conditions, but the t_D, t_{WH}, and t_{WL} settings will increase depending on the delay time inside the circuit. In addition, the deviation of the external components which are C_{CTW} and C_{CT}, (e.g.) absolute value of capacitance, DC bias, and temperature characteristic, is not considered in these formulas.

Typical Performance Curves 5 V Output

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND

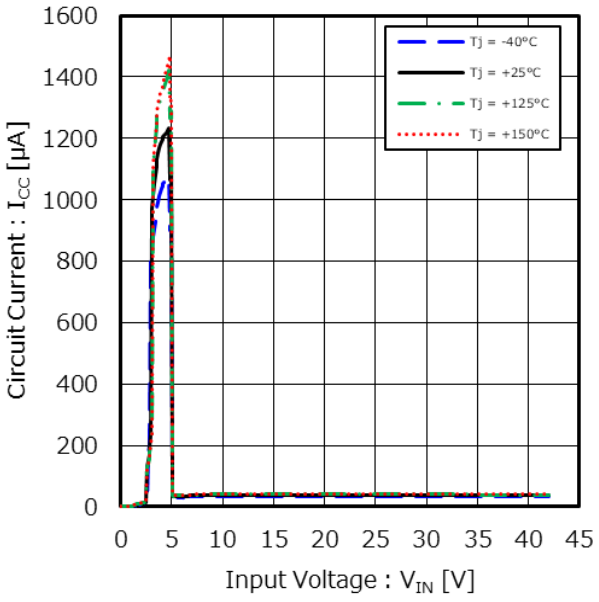


Figure 1. Circuit Current vs Input Voltage
(5 V output)

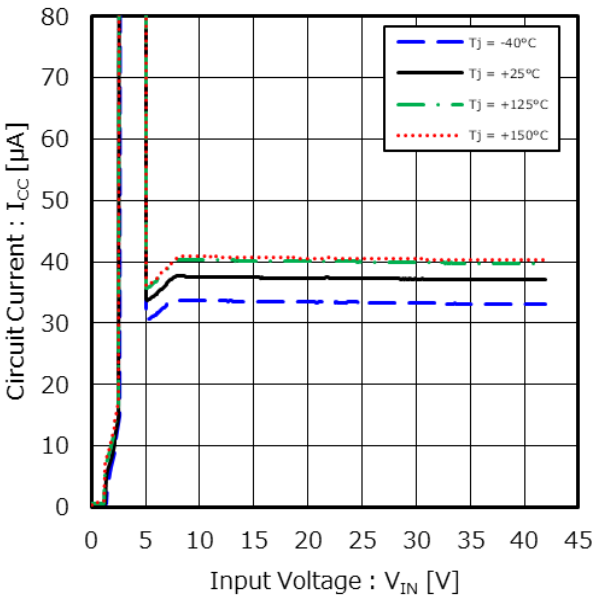


Figure 2. Circuit Current vs Input Voltage
Enlarged view of Figure 1 at narrow Circuit Current range
(5 V output)

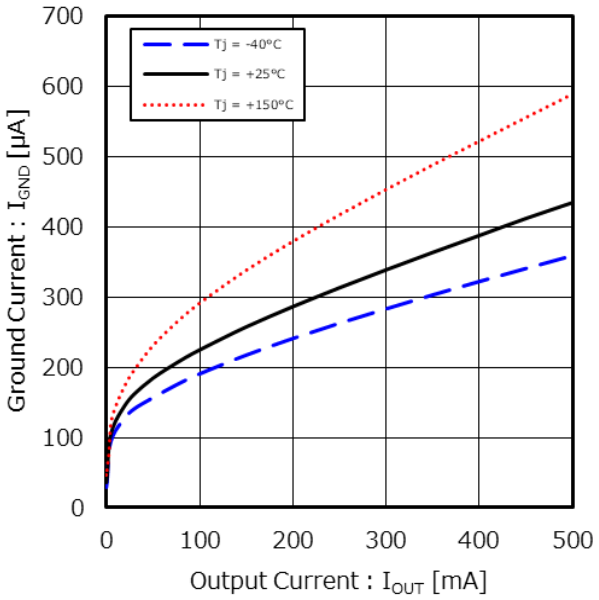


Figure 3. Ground Current vs Output Current
(5 V output)

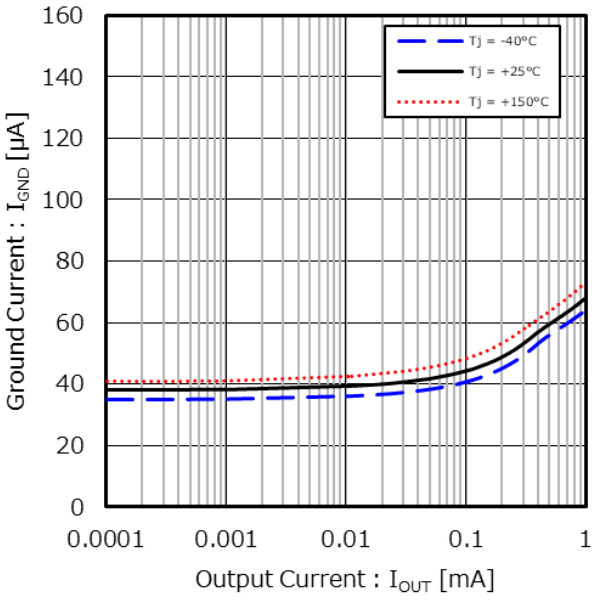


Figure 4. Ground Current vs Output Current
Enlarged view of Figure 3 at low Output Current
(5 V output)

Typical Performance Curves 5 V Output – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND

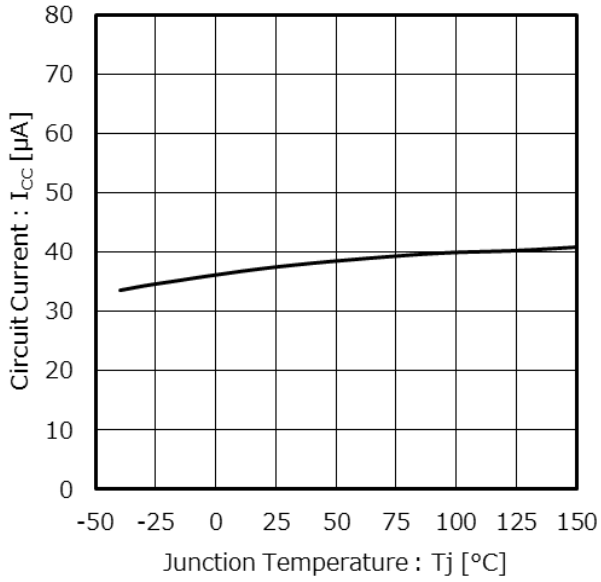


Figure 5. Circuit Current vs Junction Temperature (5 V output)

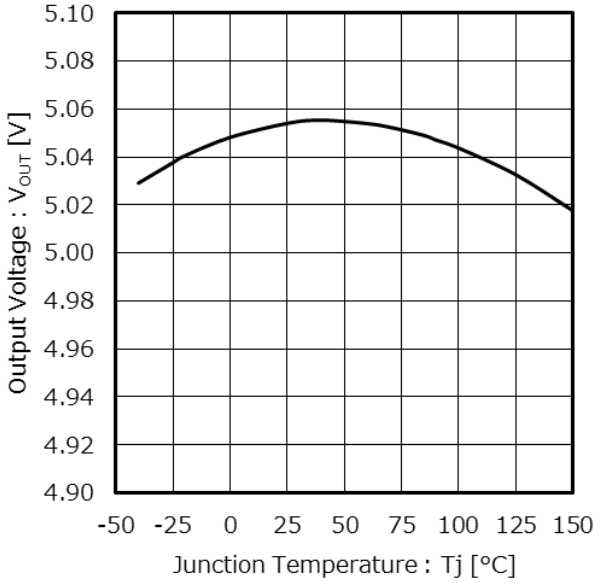


Figure 6. Output Voltage vs Junction Temperature (5 V output)

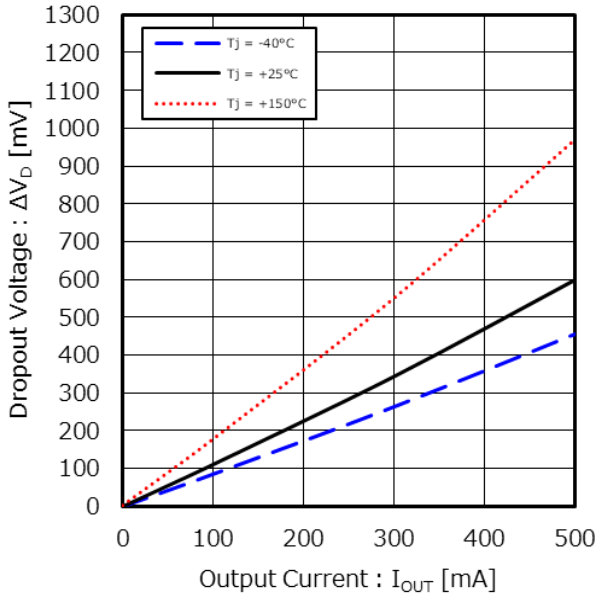


Figure 7. Dropout Voltage vs Output Current (5 V output, V_{IN} = 4.75 V)

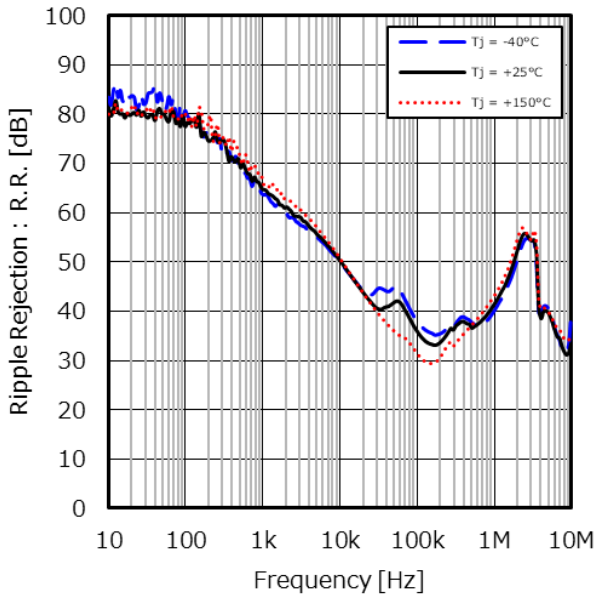


Figure 8. Ripple Rejection vs Frequency (5 V output, V_{Ripple} = 1 Vrms, I_{OUT} = 10 mA)

Typical Performance Curves 5 V Output – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND

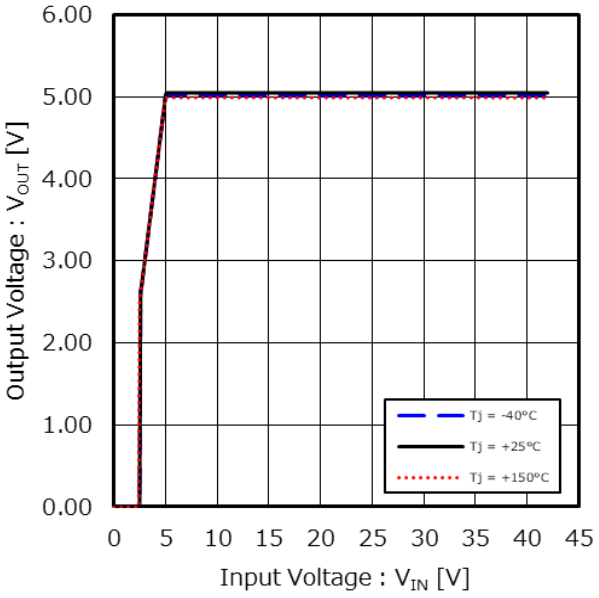


Figure 9. Output Voltage vs Input Voltage
(5 V output)

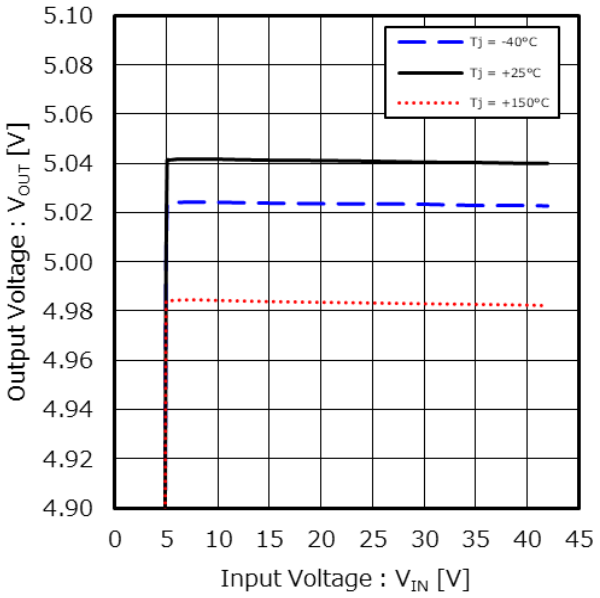


Figure 10. Output Voltage vs Input Voltage
Enlarged view of Figure 9 at narrow Output Voltage range
(5 V output, Line Regulation)

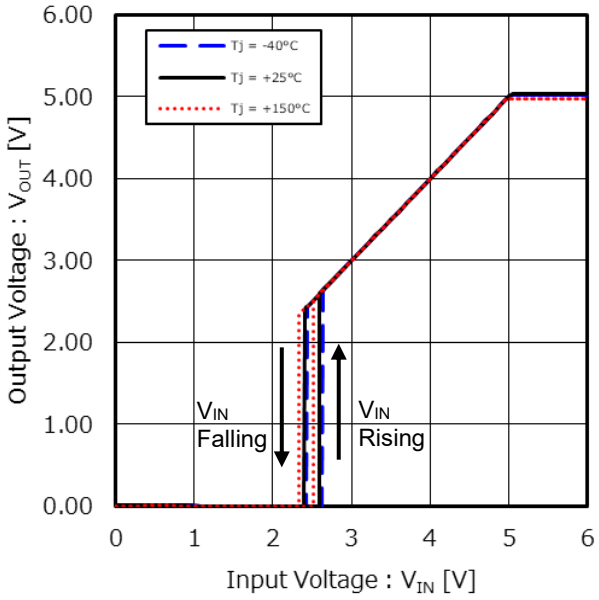


Figure 11. Output Voltage vs Input Voltage
Enlarged view of Figure 9 at low Input Voltage
(5 V output, UVLO)

Typical Performance Curves 5 V Output – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND

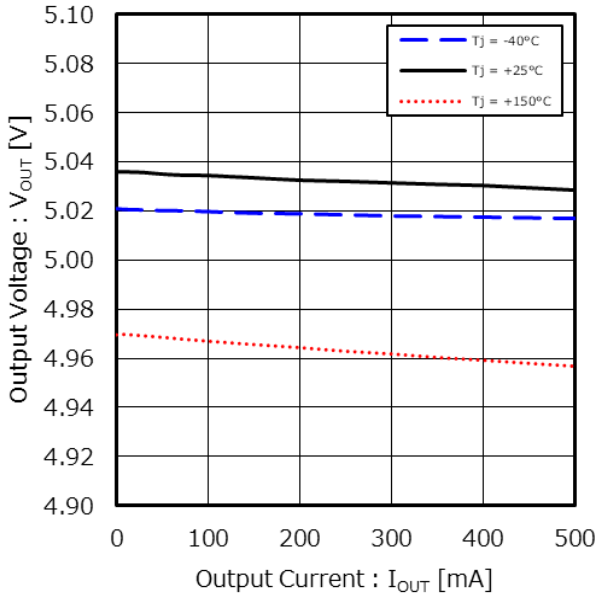


Figure 12. Output Voltage vs Output Current
(5 V output, Load Regulation)

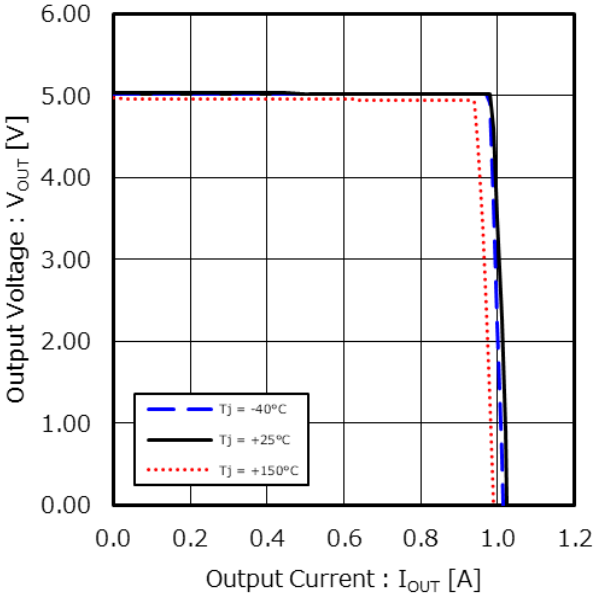


Figure 13. Output Voltage vs Output Current
(5 V output, Over Current Protection)

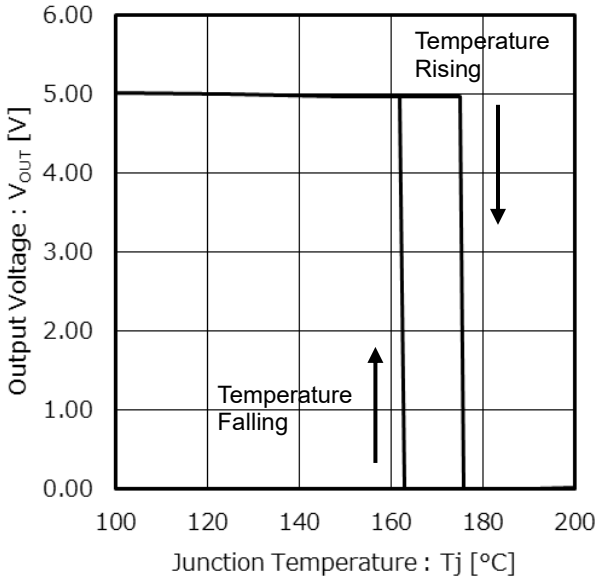


Figure 14. Output Voltage vs Junction Temperature
(5 V output, Thermal Shutdown)

Typical Performance Curves 5 V Output – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND

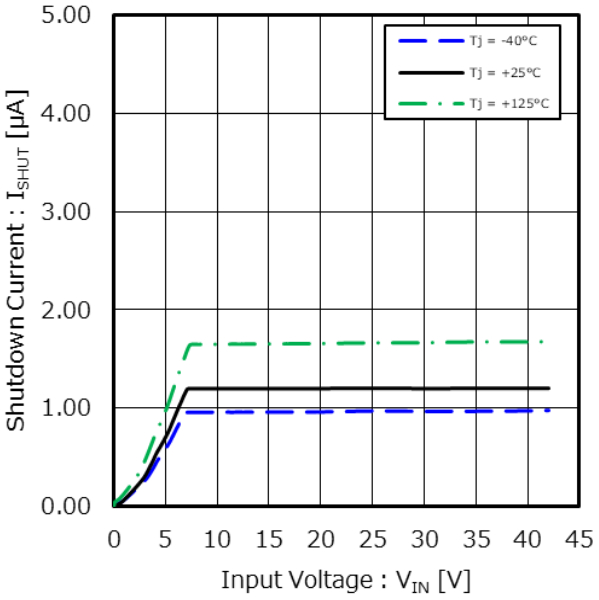


Figure 15. Shutdown Current vs Input Voltage (V_{EN} = 0 V)

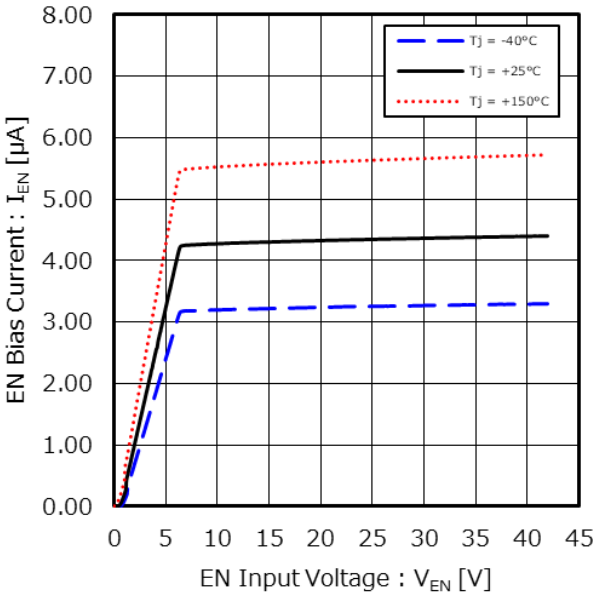


Figure 16. EN Bias Current vs EN Input Voltage

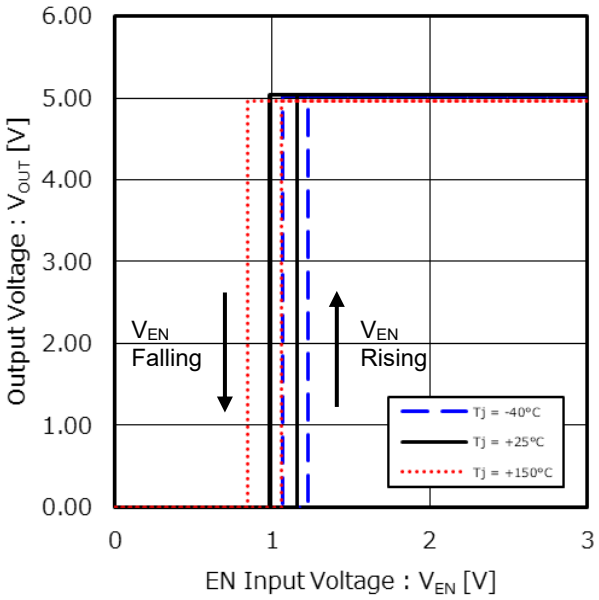


Figure 17. Output Voltage vs EN Input Voltage (5 V output)

Typical Performance Curves 5 V Output – continued

Unless otherwise specified, Tj = 25 °C, V_{IN} = 13.5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND

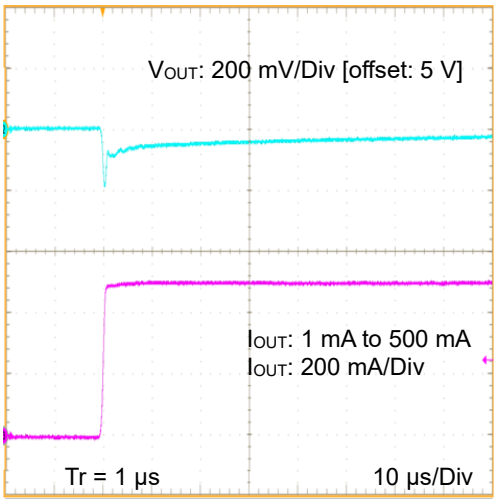


Figure 18. Load Transient 1 mA to 500 mA (5 V output, Tr = 1 µs)

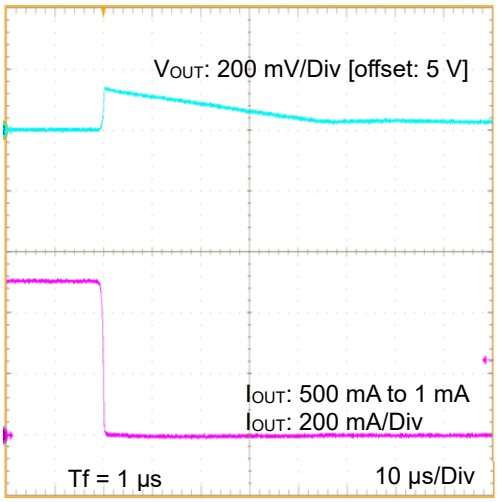


Figure 19. Load Transient 500 mA to 1 mA (5 V output, Tf = 1 µs)

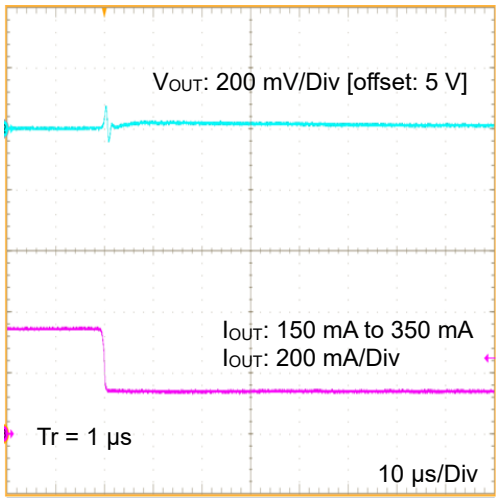


Figure 20. Load Transient 150 mA to 350 mA (5 V output, Tr = 1 µs)

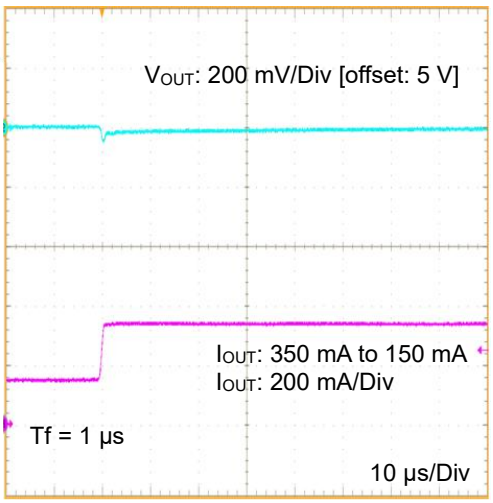


Figure 21. Load Transient 350 mA to 150 mA (5 V output, Tf = 1 µs)

Typical Performance Curves 5 V Output – continued

Unless otherwise specified, Tj = 25 °C, V_{IN} = 13.5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND

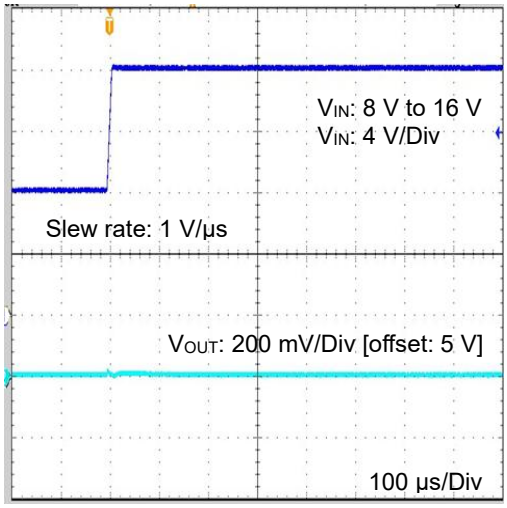


Figure 22. Line Transient 8 V to 16 V
(5 V output, I_{OUT} = 0 mA)

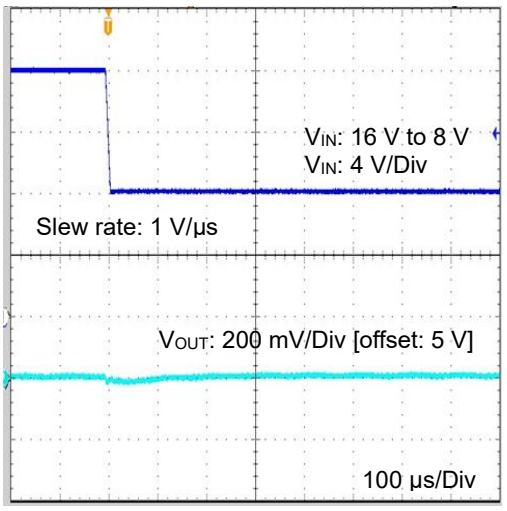


Figure 23. Line Transient 16 V to 8 V
(5 V output, I_{OUT} = 0 mA)

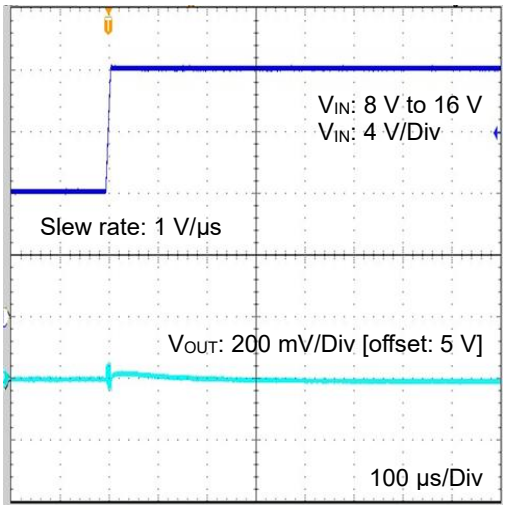


Figure 24. Line Transient 8 V to 16 V
(5 V output, I_{OUT} = 500 mA)

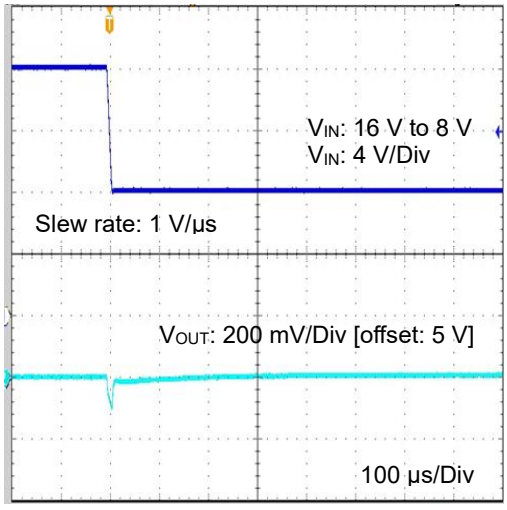


Figure 25. Line Transient 16 V to 8 V
(5 V output, I_{OUT} = 500 mA)

Typical Performance Curves 5 V Output – continued

Unless otherwise specified, Tj = 25 °C, V_{IN} = 13.5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND

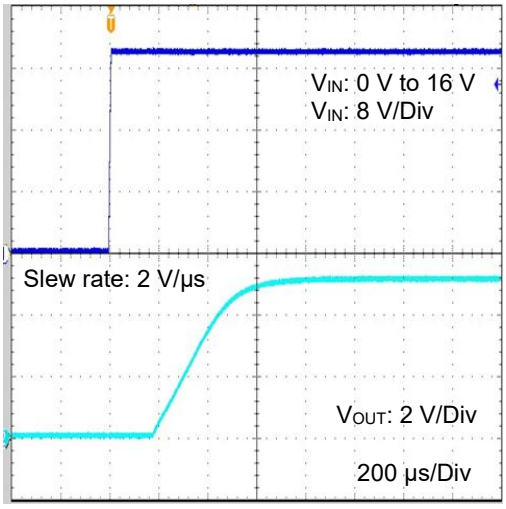


Figure 26. VIN Startup Waveform
V_{IN}: 0 V to 16 V
(5 V output, I_{OUT} = 0 mA)

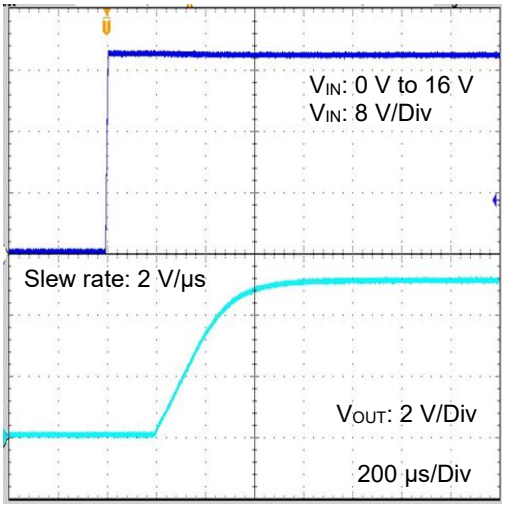


Figure 27. VIN Startup Waveform
V_{IN}: 0 V to 16 V
(5 V output, I_{OUT} = 500 mA)

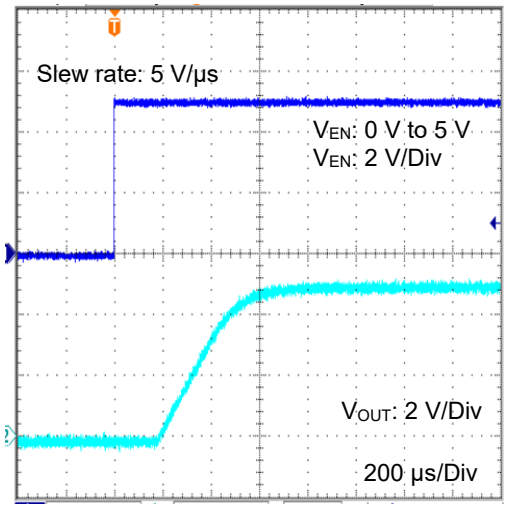


Figure 28. EN Startup Waveform
(5 V output, I_{OUT} = 1 mA)

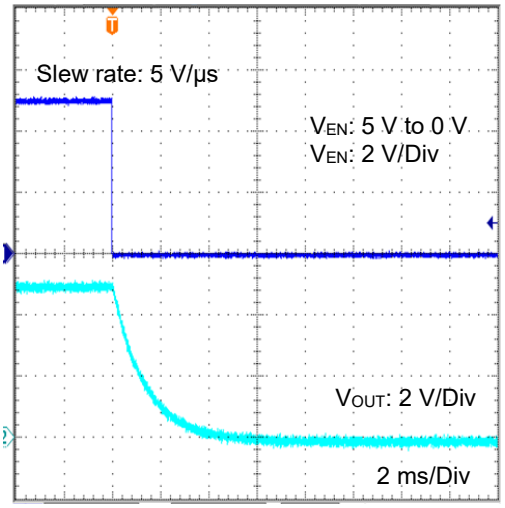


Figure 29. EN Shutdown Waveform
(5 V output, I_{OUT} = 1 mA)

Typical Performance Curves 3.3 V Output

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND

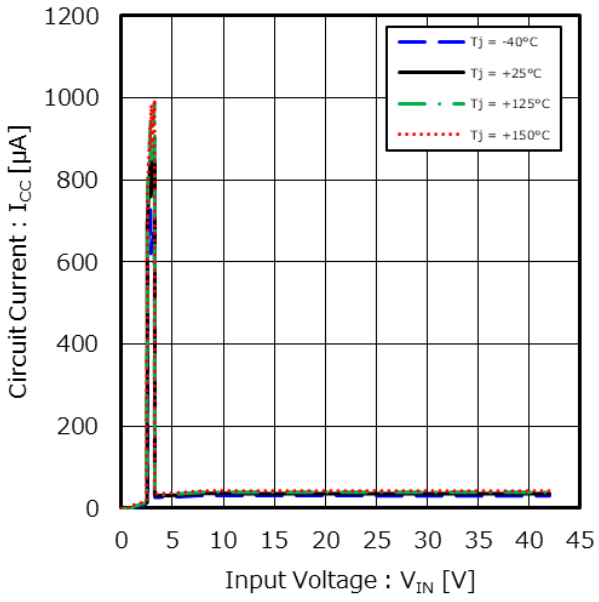


Figure 30. Circuit Current vs Input Voltage
(3.3 V output)

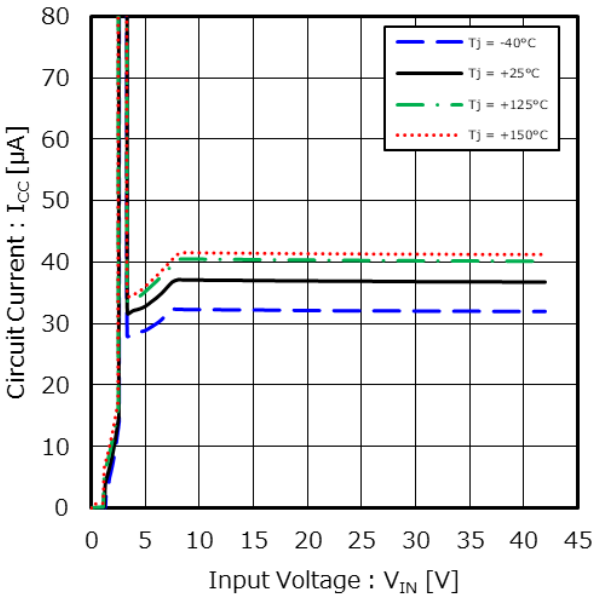


Figure 31. Circuit Current vs Input Voltage
Enlarged view of Figure 30 at narrow Circuit Current range
(3.3 V output)

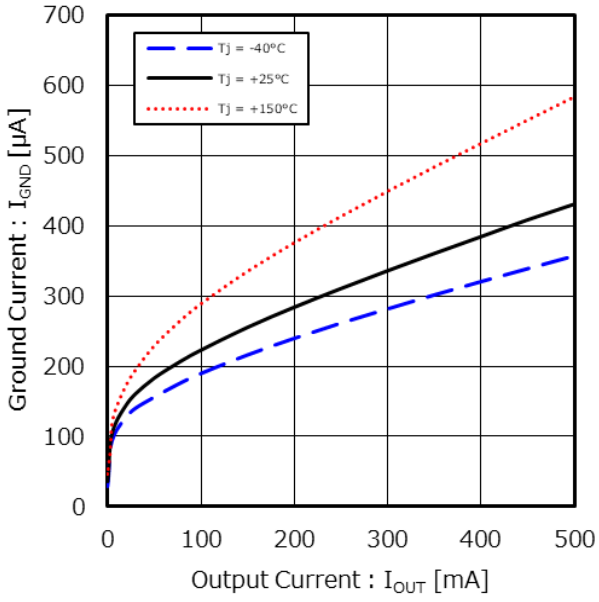


Figure 32. Ground Current vs Output Current
(3.3 V output)

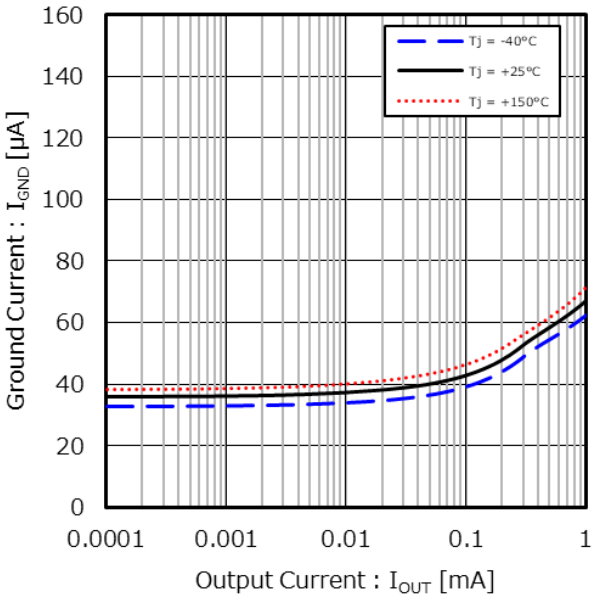


Figure 33. Ground Current vs Output Current
Enlarged view of Figure 32 at low Output Current
(3.3 V output)

Typical Performance Curves 3.3 V Output – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND

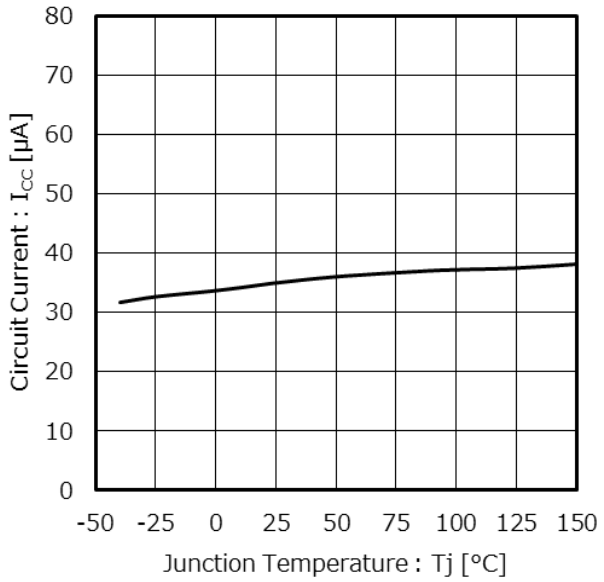


Figure 34. Circuit Current vs Junction Temperature (3.3 V output)

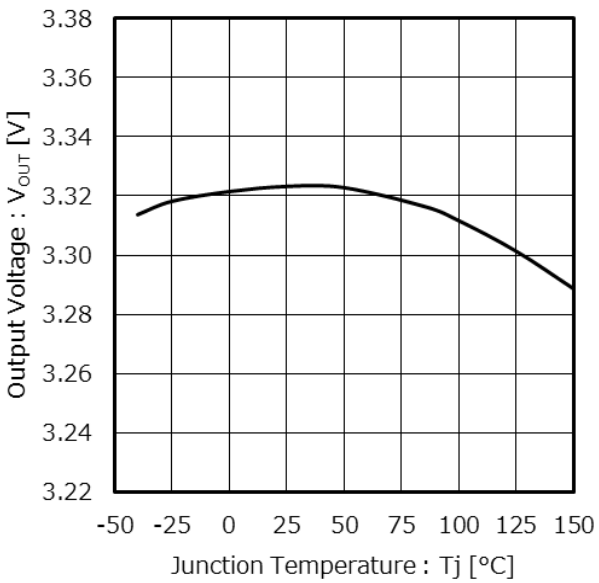


Figure 35. Output Voltage vs Junction Temperature (3.3 V output)

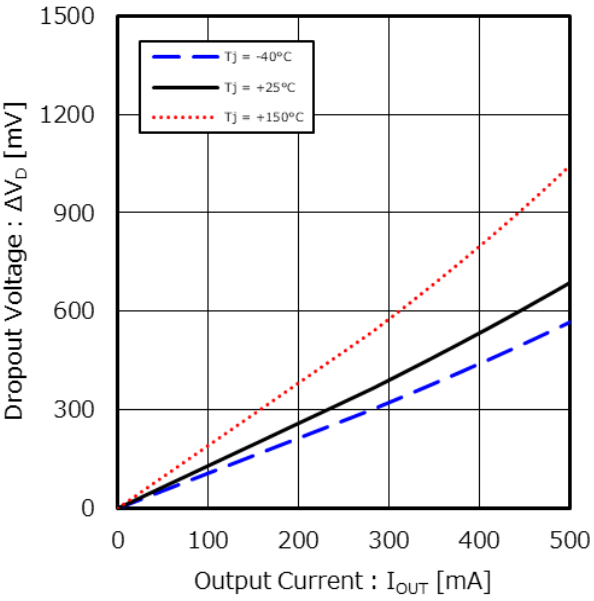


Figure 36. Dropout Voltage vs Output Current (3.3 V output, V_{IN} = 3.135 V)

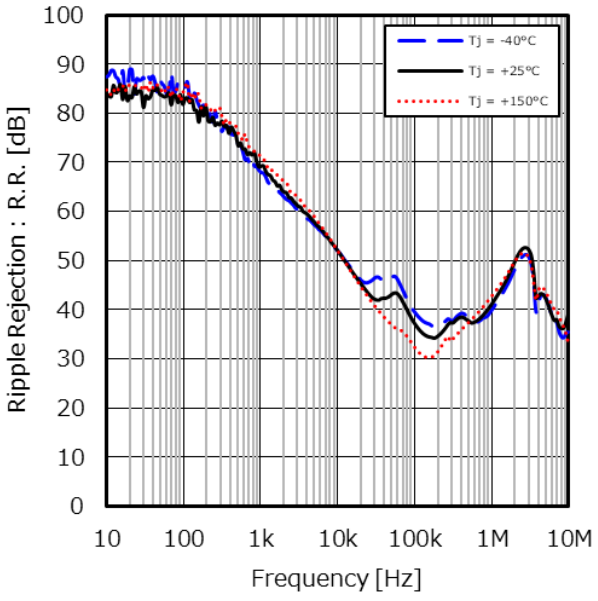


Figure 37. Ripple Rejection vs Frequency (3.3 V output, V_{Ripple} = 1 Vrms, I_{OUT} = 10 mA)

Typical Performance Curves 3.3 V Output – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = 13.5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND

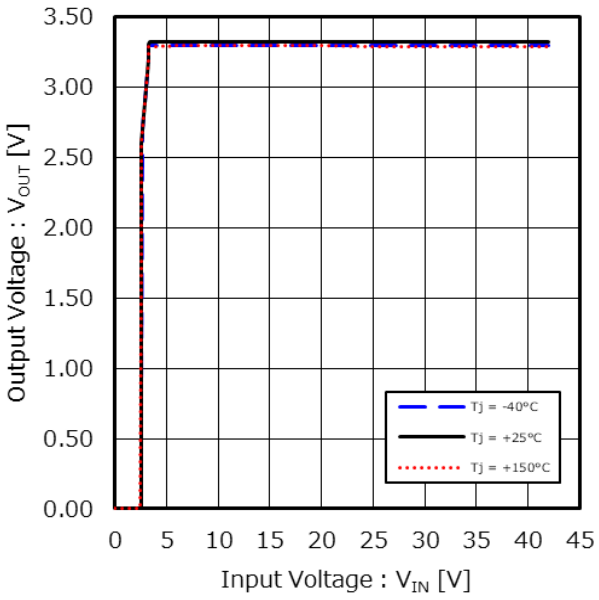


Figure 38. Output Voltage vs Input Voltage
(3.3 V output)

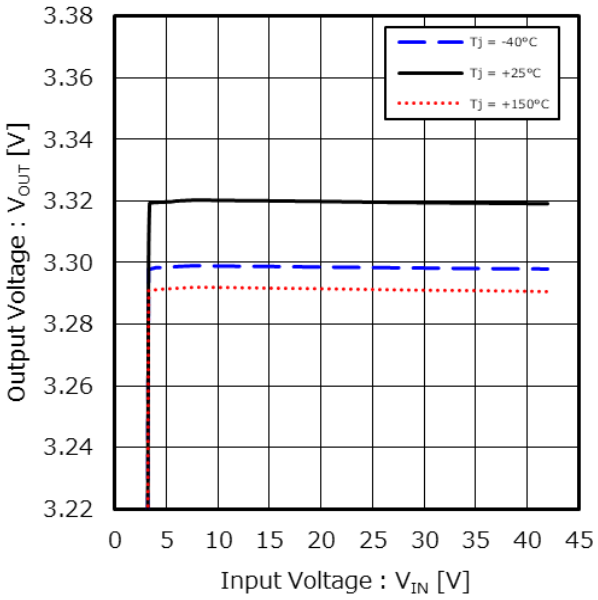


Figure 39. Output Voltage vs Input Voltage
Enlarged view of Figure 38 at narrow Output Voltage range
(3.3 V output, Line Regulation)

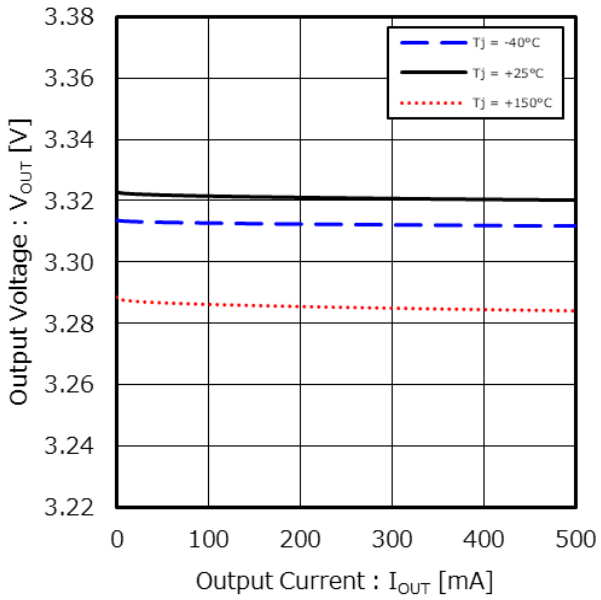


Figure 40. Output Voltage vs Output Current
(3.3 V output, Load Regulation)

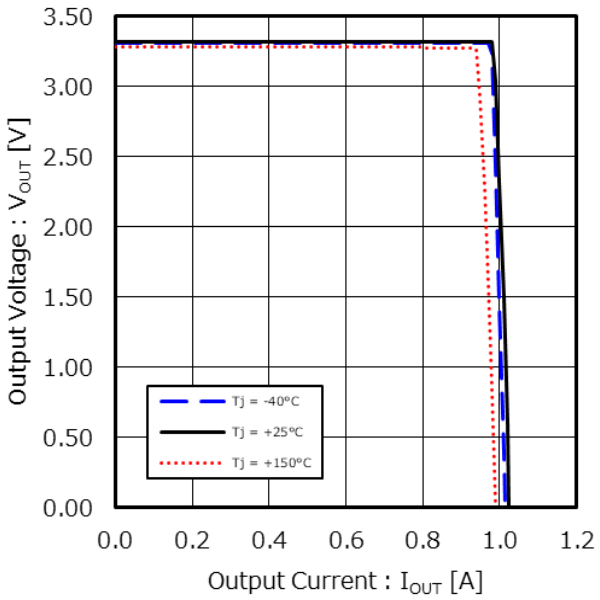


Figure 41. Output Voltage vs Output Current
(3.3 V output, Over Current Protection)

Typical Performance Curves 3.3 V Output – continued

Unless otherwise specified, Tj = 25 °C, V_{IN} = 13.5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND

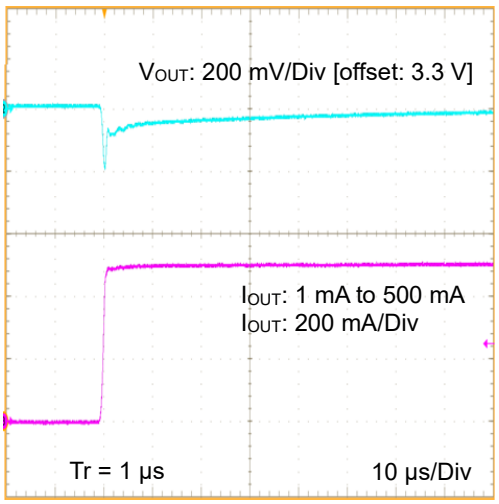


Figure 42. Load Transient 1 mA to 500 mA (3.3 V output, Tr = 1 µs)

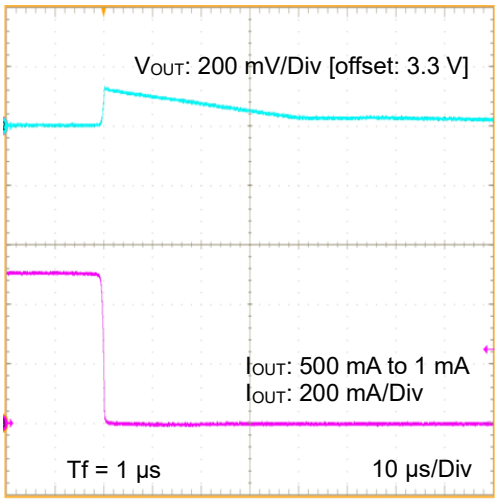


Figure 43. Load Transient 500 mA to 1 mA (3.3 V output, Tf = 1 µs)

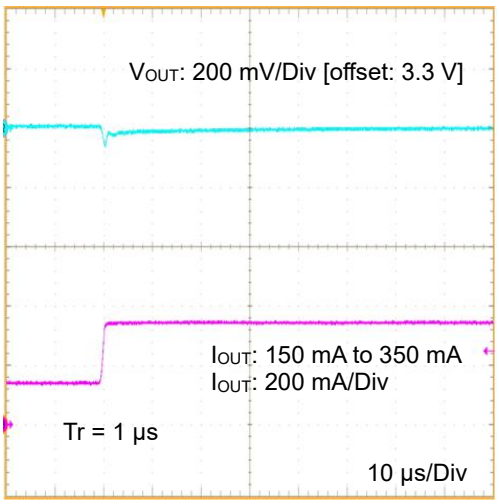


Figure 44. Load Transient 150 mA to 350 mA (3.3 V output, Tr = 1 µs)

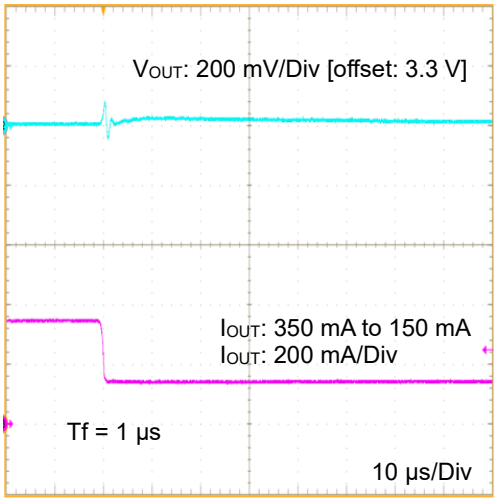


Figure 45. Load Transient 350 mA to 150 mA (3.3 V output, Tf = 1 µs)

Typical Performance Curves 3.3 V Output – continued

Unless otherwise specified, Tj = 25 °C, V_{IN} = 13.5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND

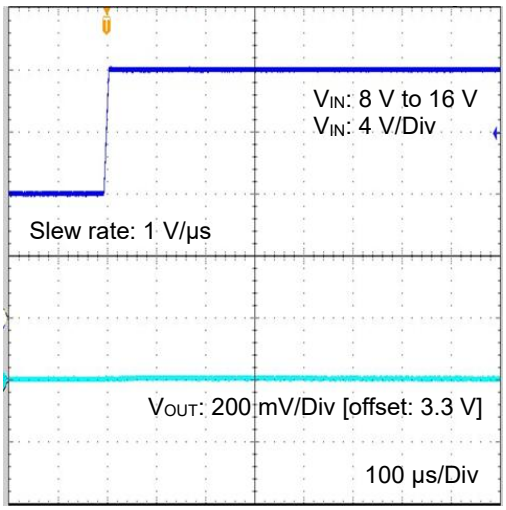


Figure 46. Line Transient 8 V to 16 V
(3.3 V output, I_{OUT} = 0 mA)

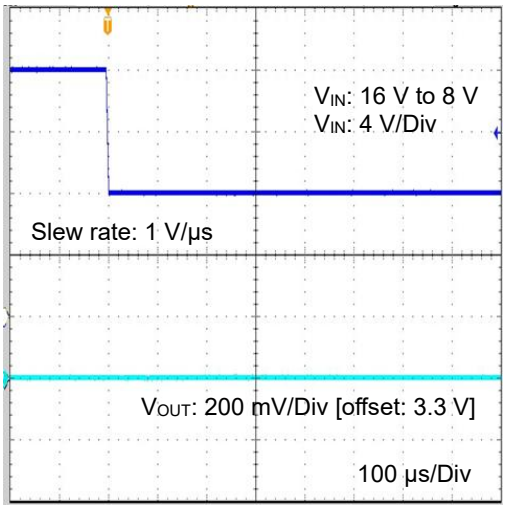


Figure 47. Line Transient 16 V to 8 V
(3.3 V output, I_{OUT} = 0 mA)

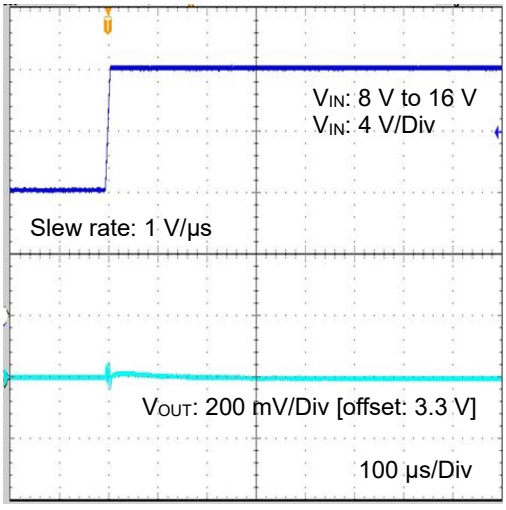


Figure 48. Line Transient 8 V to 16 V
(3.3 V output, I_{OUT} = 500 mA)

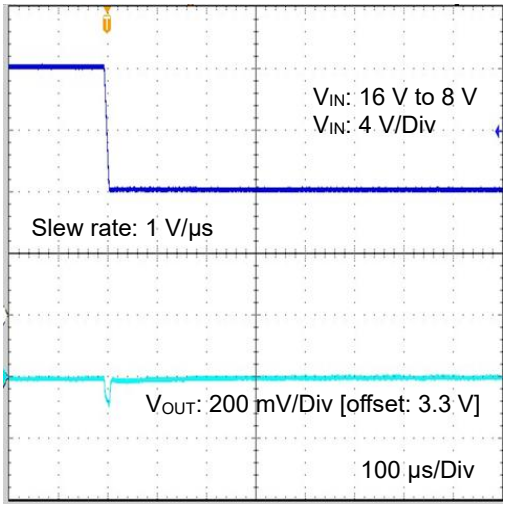


Figure 49. Line Transient 16 V to 8 V
(3.3 V output, I_{OUT} = 500 mA)

Typical Performance Curves 3.3 V Output – continued

Unless otherwise specified, Tj = 25 °C, V_{IN} = 13.5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, CTW = GND

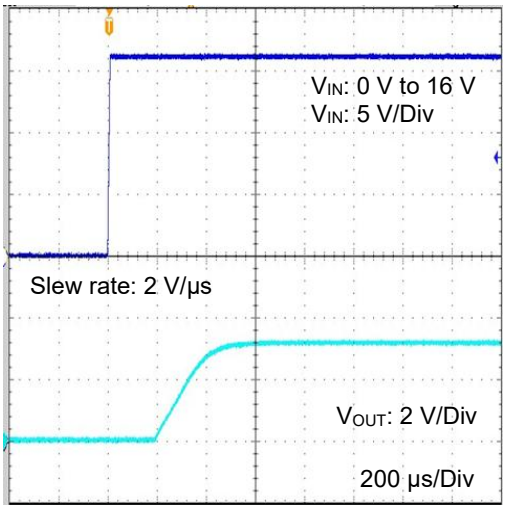


Figure 50. VIN Startup Waveform
V_{IN}: 0 V to 16 V
(3.3 V output, I_{OUT} = 0 mA)

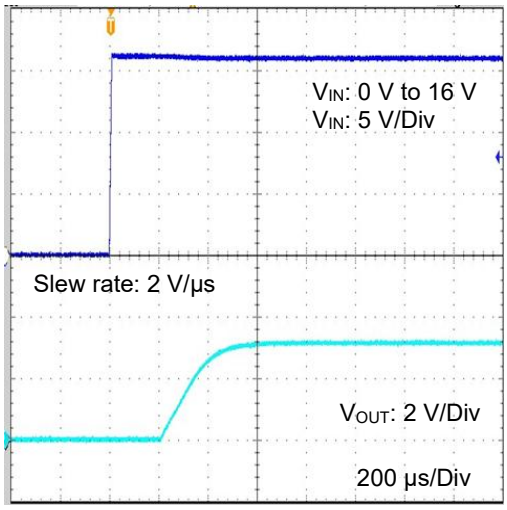


Figure 51. VIN Startup Waveform
V_{IN}: 0 V to 16 V
(3.3 V output, I_{OUT} = 500 mA)

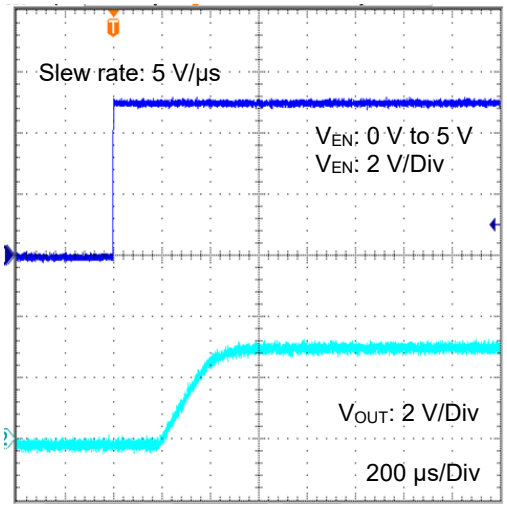


Figure 52. EN Startup Waveform
(3.3 V output, I_{OUT} = 1 mA)

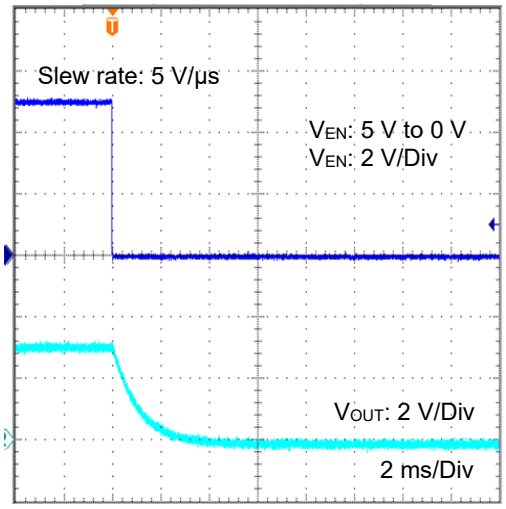


Figure 53. EN Shutdown Waveform
(3.3 V output, I_{OUT} = 1 mA)

Typical Performance Curves WDT, RESET

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = V_{OUT} = 5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, C_{CT} = 0.01 µF, C_{CTW} = 0.0047 µF

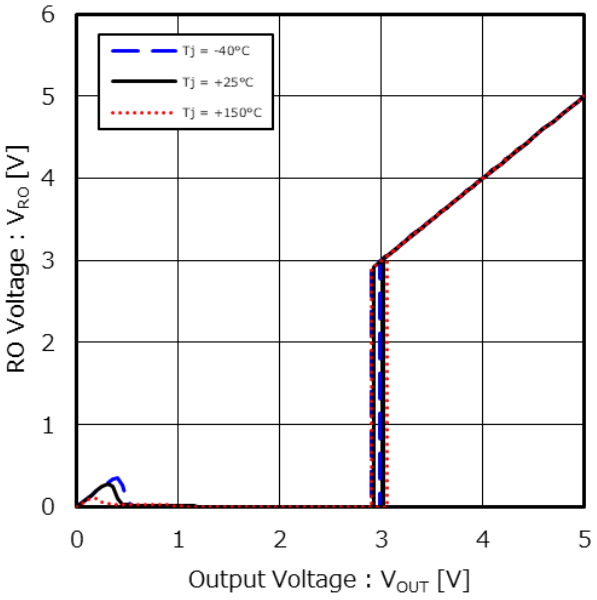


Figure 54. RO Voltage vs Output Voltage
(Reset Detection Voltage, V_{DET} = 2.9 V)

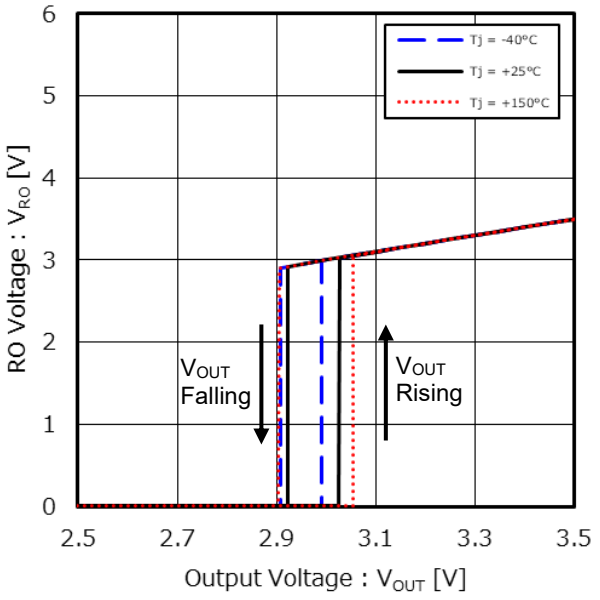


Figure 55. RO Voltage vs Output Voltage
(Reset Detection Voltage, V_{DET} = 2.9 V, Zoom version)

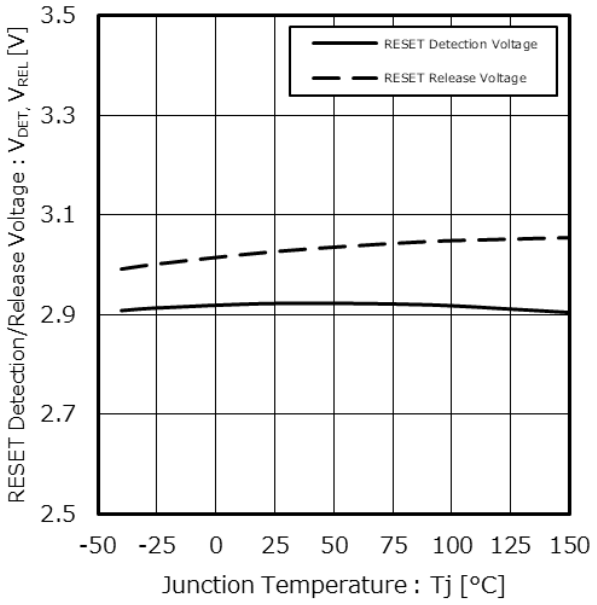


Figure 56. RESET Detection/Release Voltage vs Junction Temperature
(V_{DET} = 2.9 V)

Typical Performance Curves WDT, RESET – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = V_{OUT} = 5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, C_{CT} = 0.01 µF, C_{CTW} = 0.0047 µF

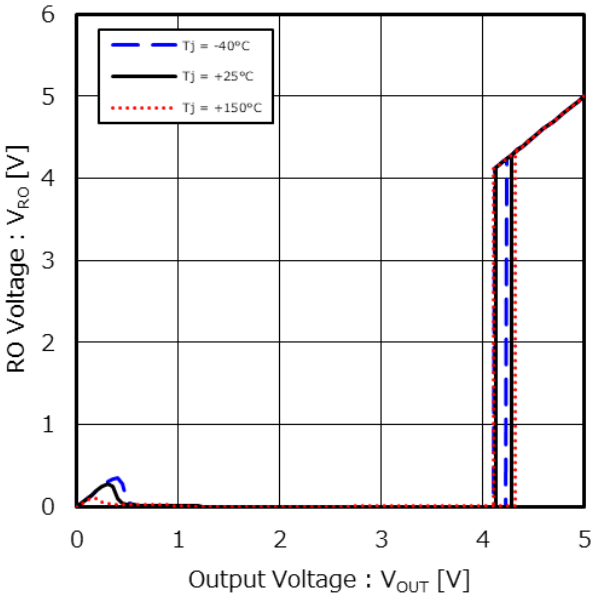


Figure 57. RO Voltage vs Output Voltage
(Reset Detection Voltage, V_{DET} = 4.1 V)

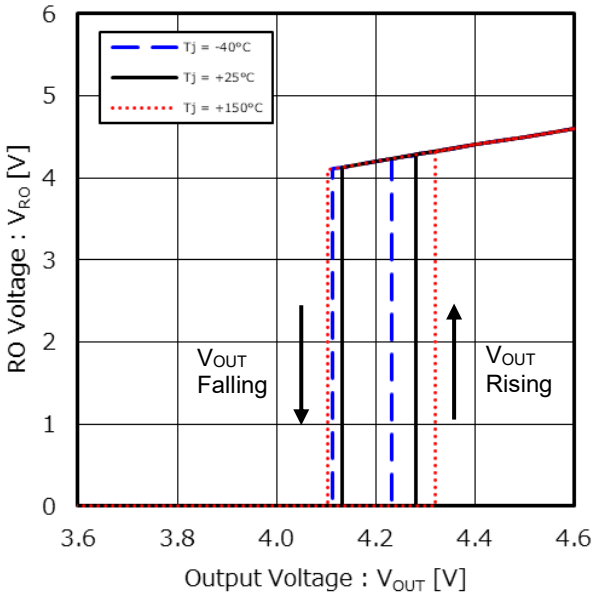


Figure 58. RO Voltage vs Output Voltage
(Reset Detection Voltage, V_{DET} = 4.1 V, Zoom version)

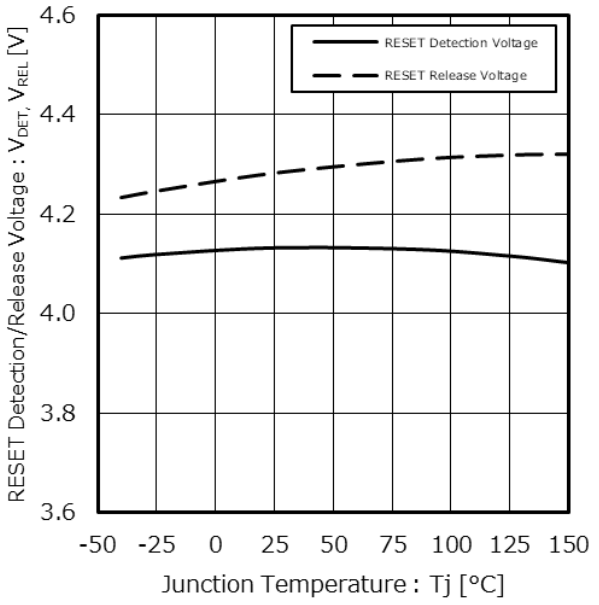


Figure 59. RESET Detection/Release Voltage vs Junction Temperature
(V_{DET} = 4.1 V)

Typical Performance Curves WDT, RESET – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = V_{OUT} = 5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, C_{CT} = 0.01 µF, C_{CTW} = 0.0047 µF

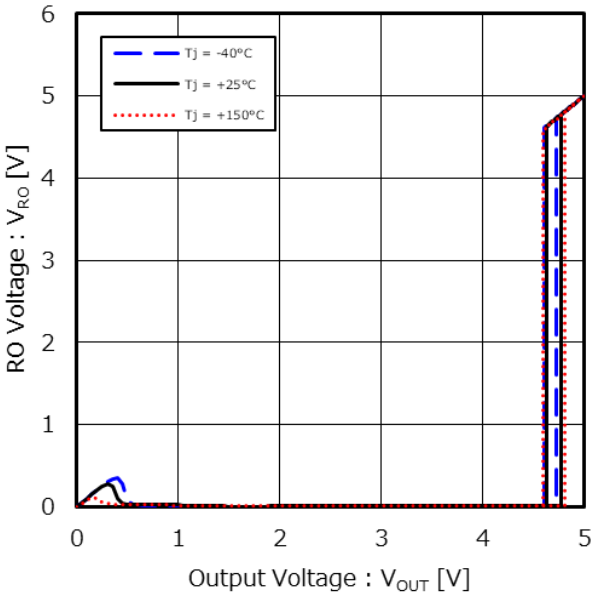


Figure 60. RO Voltage vs Output Voltage
(Reset Detection Voltage, V_{DET} = 4.6 V)

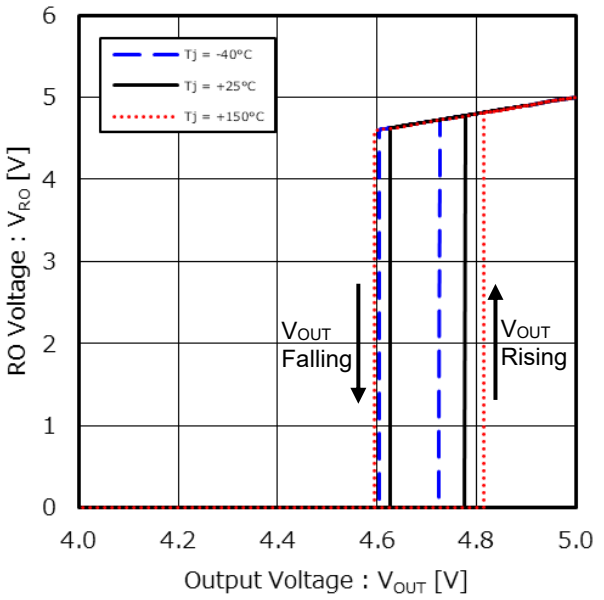


Figure 61. RO Voltage vs Output Voltage
(Reset Detection Voltage, V_{DET} = 4.6 V, Zoom version)

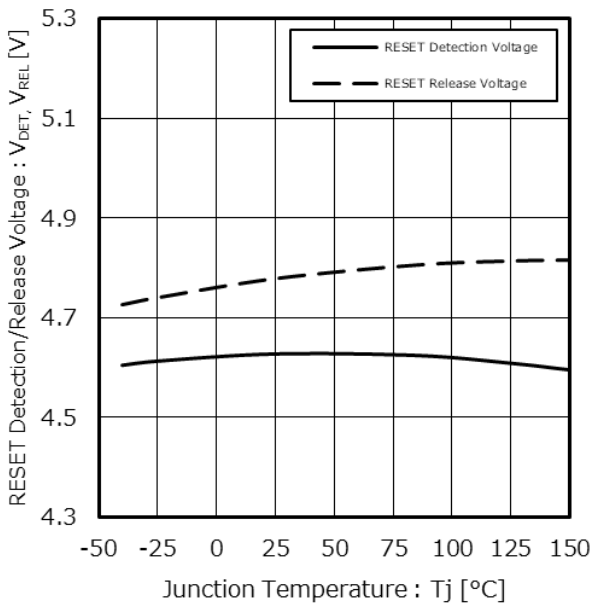


Figure 62. RESET Detection/Release Voltage vs Junction Temperature
(V_{DET} = 4.6 V)

Typical Performance Curves WDT, RESET – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = V_{OUT} = 5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, C_{CT} = 0.01 µF, C_{CTW} = 0.0047 µF

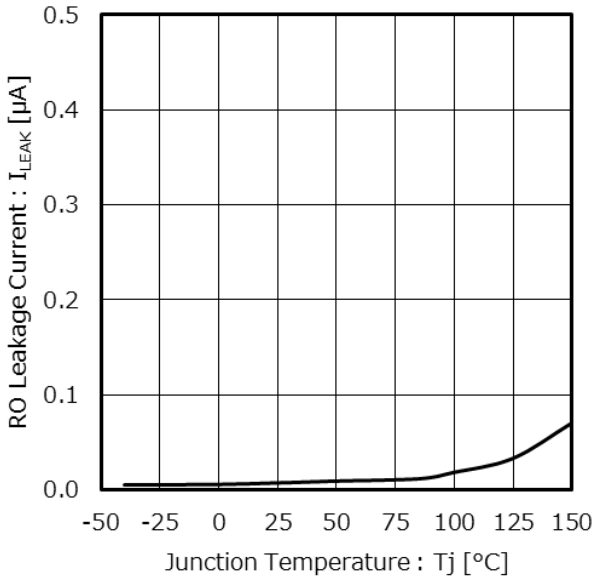


Figure 63. RO Leakage Current vs Junction Temperature (V_{RO} = 5 V)

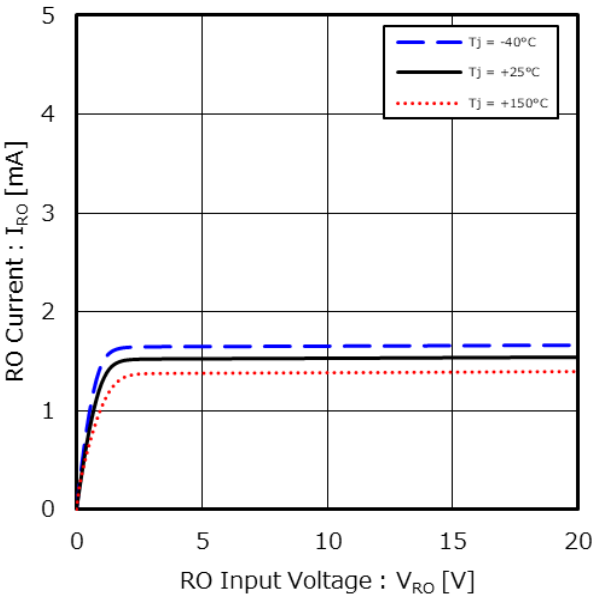


Figure 64. RO Current vs RO Input Voltage (V_{IN} = 1.0 V, Exclude the current flowing through the internal pull-up resistor between RO and VOUT.)

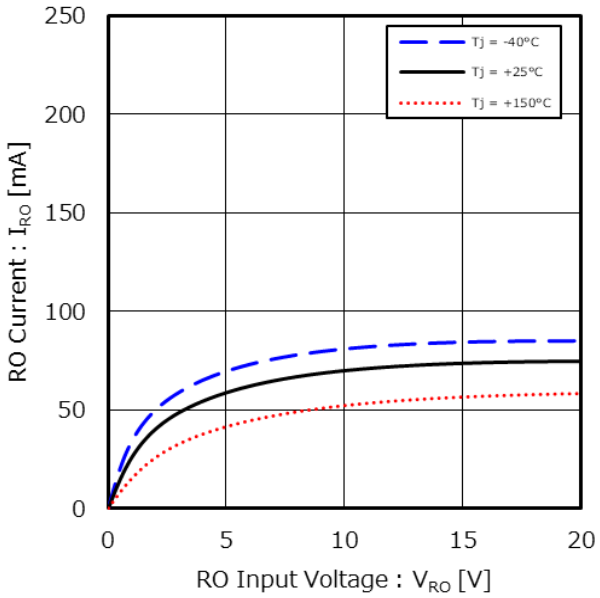


Figure 65. RO Current vs RO Input Voltage (V_{IN} = 2.0 V, Exclude the current flowing through the internal pull-up resistor between RO and VOUT.)

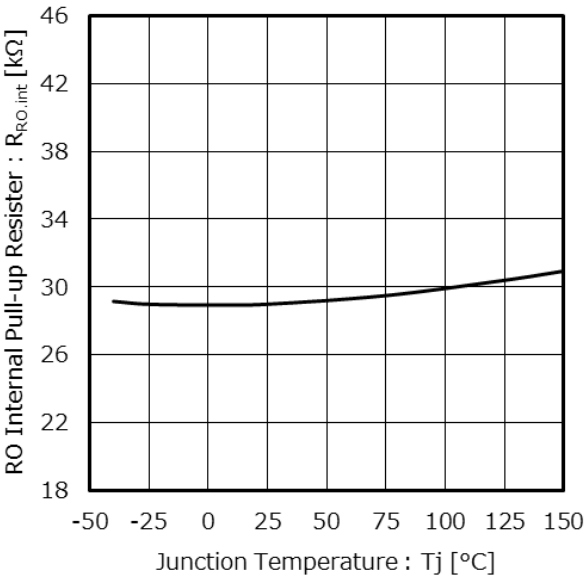


Figure 66. RO Internal Pull-up Resistor vs Junction Temperature (V_{IN} = 0 V, V_{RO} = 0.5 V)

Typical Performance Curves WDT, RESET – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = V_{OUT} = 5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, C_{CT} = 0.01 µF, C_{CTW} = 0.0047 µF

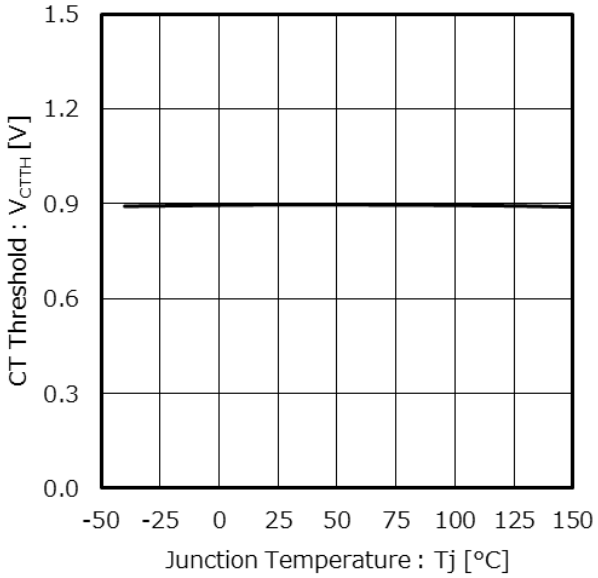


Figure 67. CT Threshold vs Junction Temperature

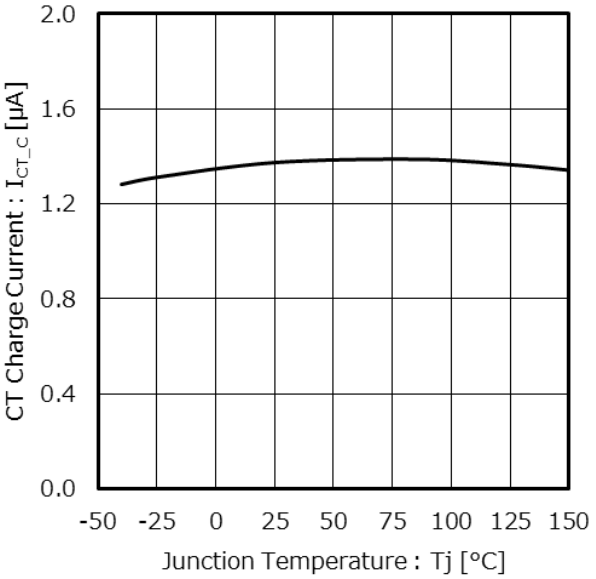


Figure 68. CT Charge Current vs Junction Temperature (V_{CT} = 0.5 V)

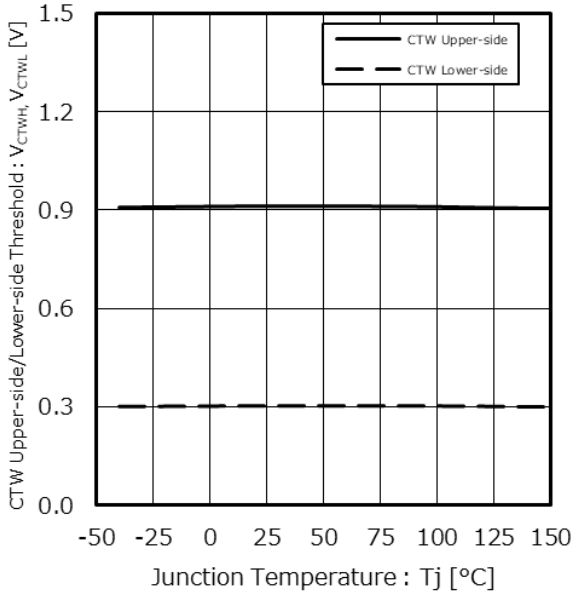


Figure 69. CTW Upper-side/Lower-side Threshold vs Junction Temperature

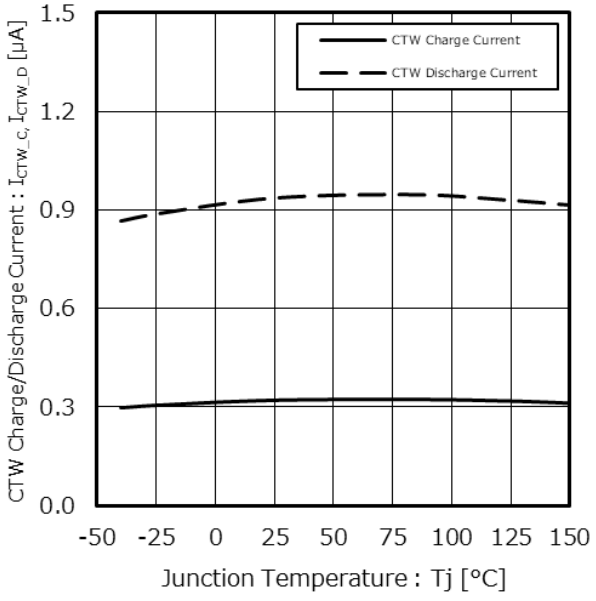


Figure 70. CTW Charge/Discharge Current vs Junction Temperature (CTW Charge Current V_{CTW} = 0.2 V, CTW Discharge Current V_{CTW} = 1.0 V)

Typical Performance Curves WDT, RESET – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = V_{OUT} = 5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, C_{CT} = 0.01 µF, C_{CTW} = 0.0047 µF

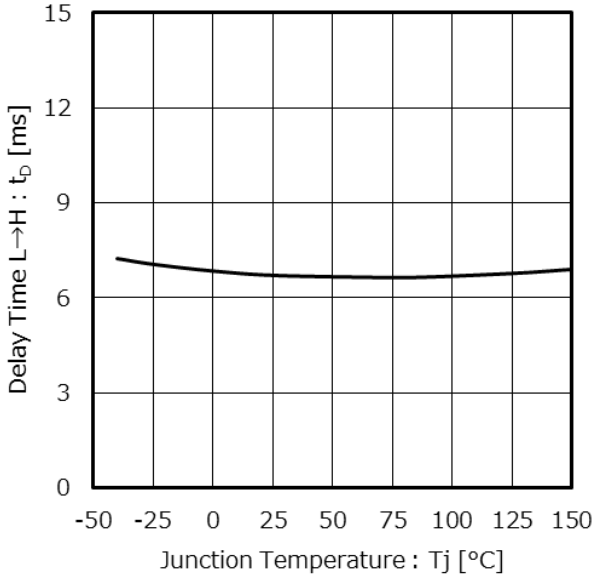


Figure 71. Delay Time L→H vs Junction Temperature

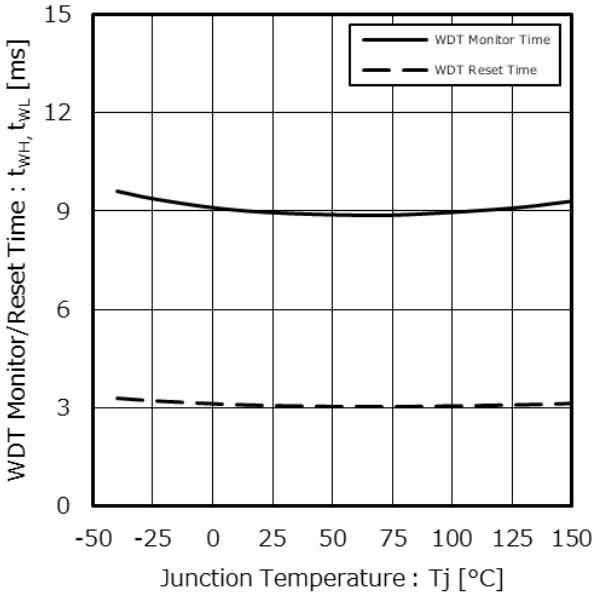


Figure 72. WDT Monitor/Reset Time vs Junction Temperature

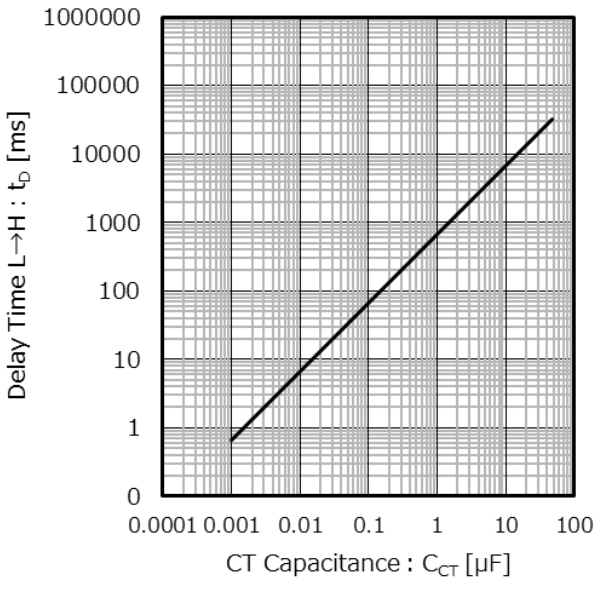


Figure 73. Delay Time L→H vs CT Capacitance
(Tj = 25 °C)

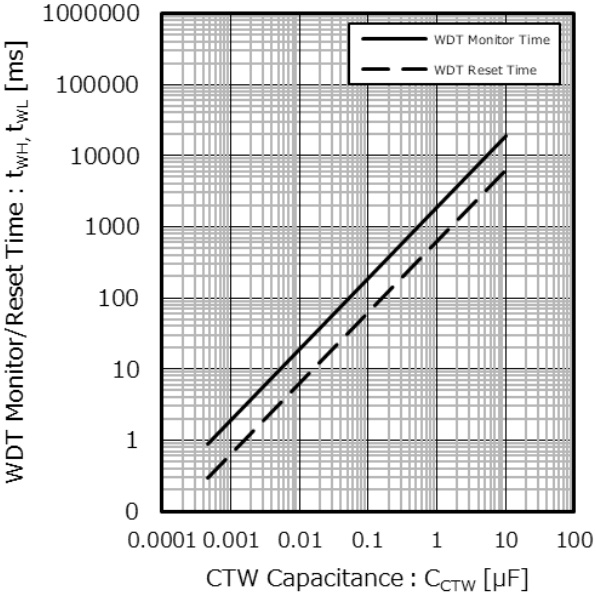


Figure 74. WDT Monitor/Reset Time vs CTW Capacitance
(Tj = 25 °C)

Typical Performance Curves WDT, RESET – continued

Unless otherwise specified, Tj = -40 °C to +150 °C, V_{IN} = V_{OUT} = 5 V, C_{IN} = 1 µF, I_{OUT} = 0 mA, C_{OUT} = 0.47 µF, V_{EN} = 5.0 V, C_{CT} = 0.01 µF, C_{CTW} = 0.0047 µF

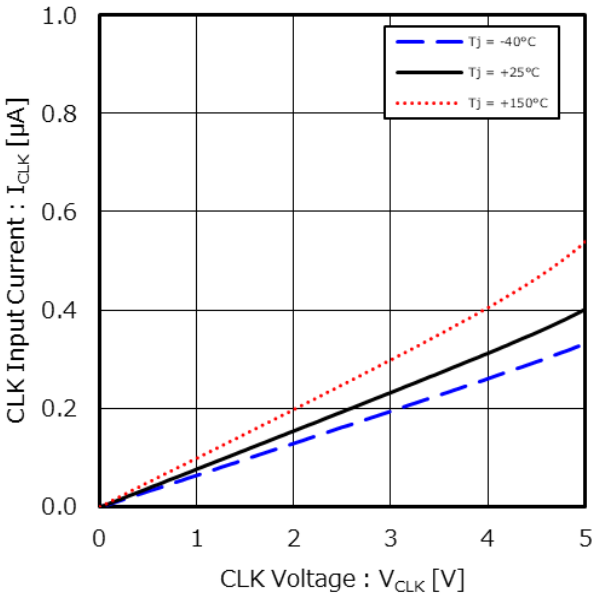


Figure 75. CLK Input Current vs CLK Voltage

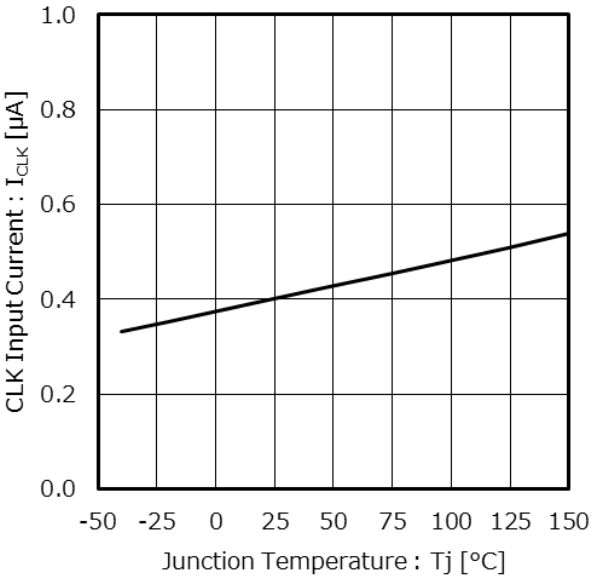
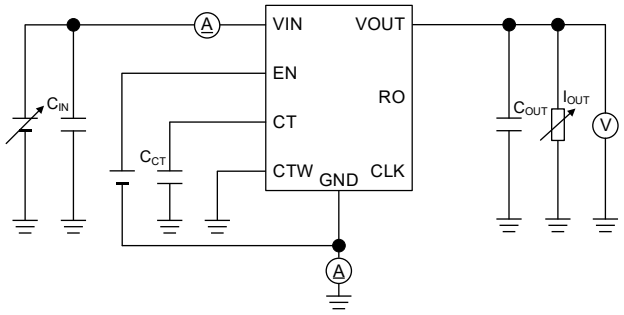
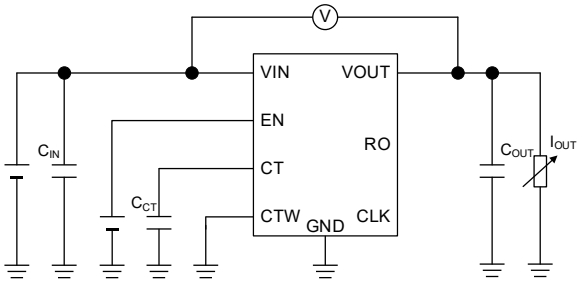


Figure 76. CLK Input Current vs Junction Temperature (V_{CLK} = 5.0 V)

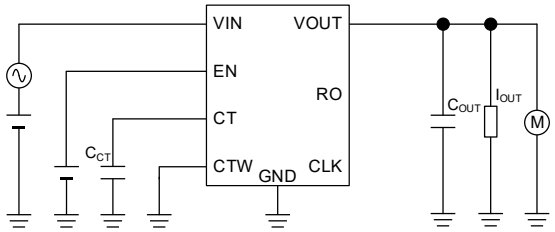
Measurement Circuit for Typical Performance Curves



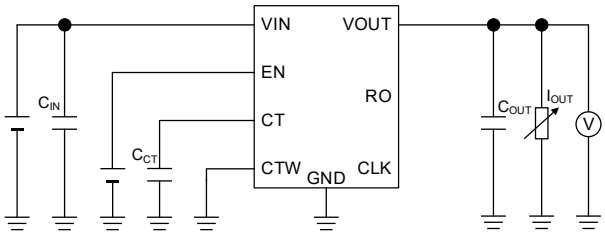
Measurement Setup for
Figure 1 to 6, 9 to 11, 14, 15, 30 to 35, 38, 39



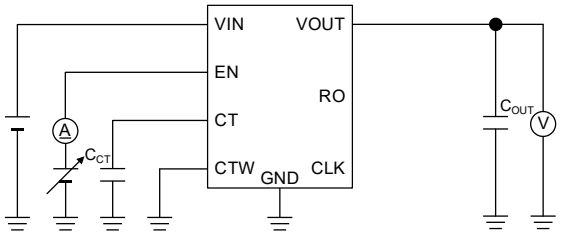
Measurement Setup for
Figure 7, 36



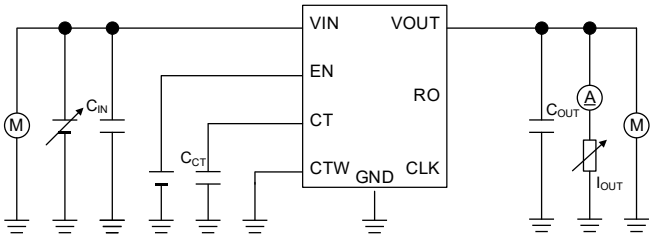
Measurement Setup for
Figure 8, 37



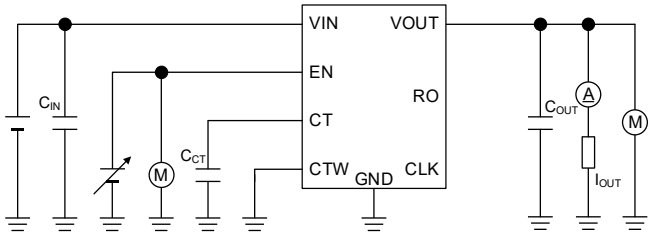
Measurement Setup for
Figure 12, 13, 40, 41



Measurement Setup for
Figure 16, 17

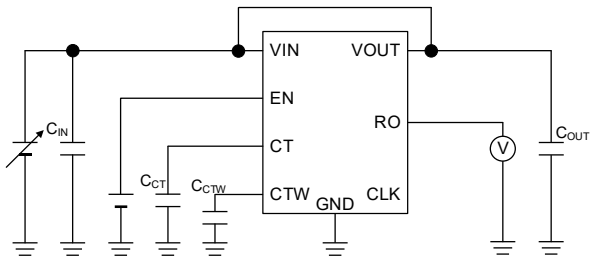


Measurement Setup for
Figure 18 to 27, 42 to 51

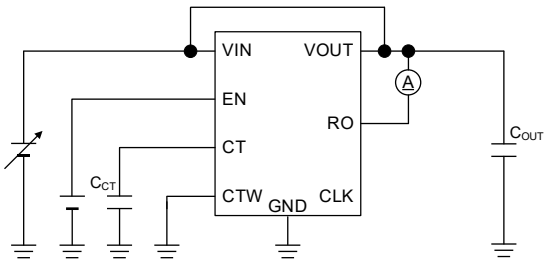


Measurement Setup for
Figure 28, 29, 52, 53

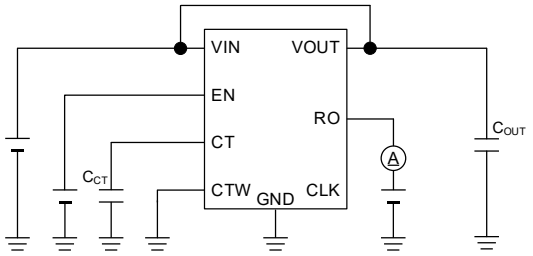
Measurement Circuit for Typical Performance Curves – continued



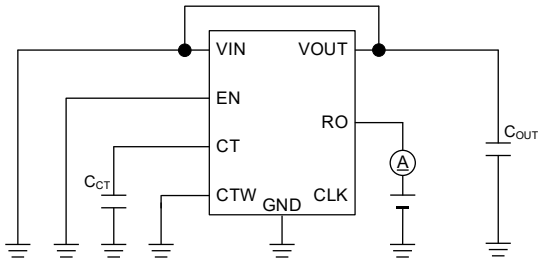
Measurement Setup for
Figure 54 to 62



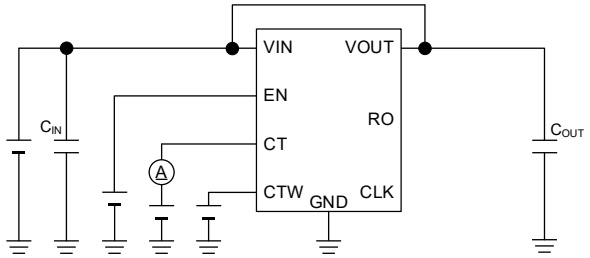
Measurement Setup for
Figure 63



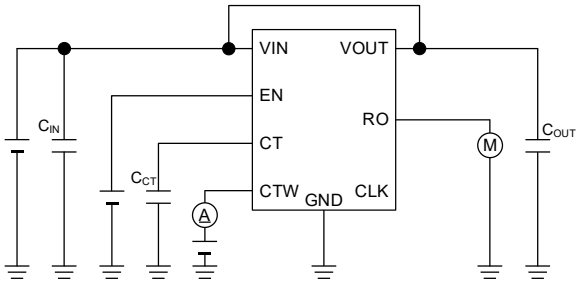
Measurement Setup for
Figure 64, 65



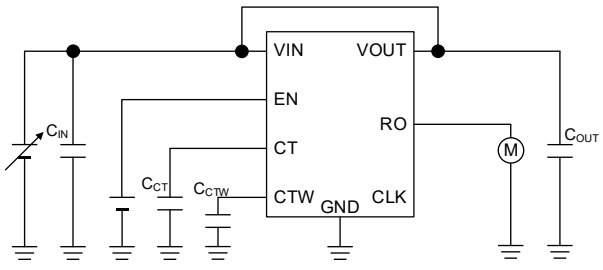
Measurement Setup for
Figure 66



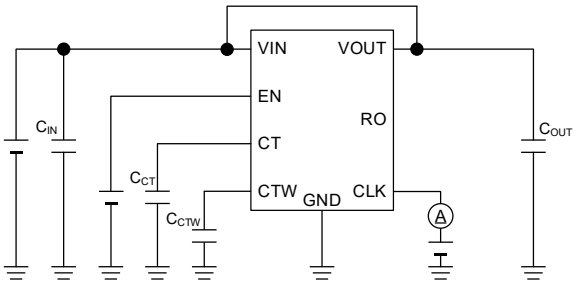
Measurement Setup for
Figure 67, 68



Measurement Setup for
Figure 69, 70



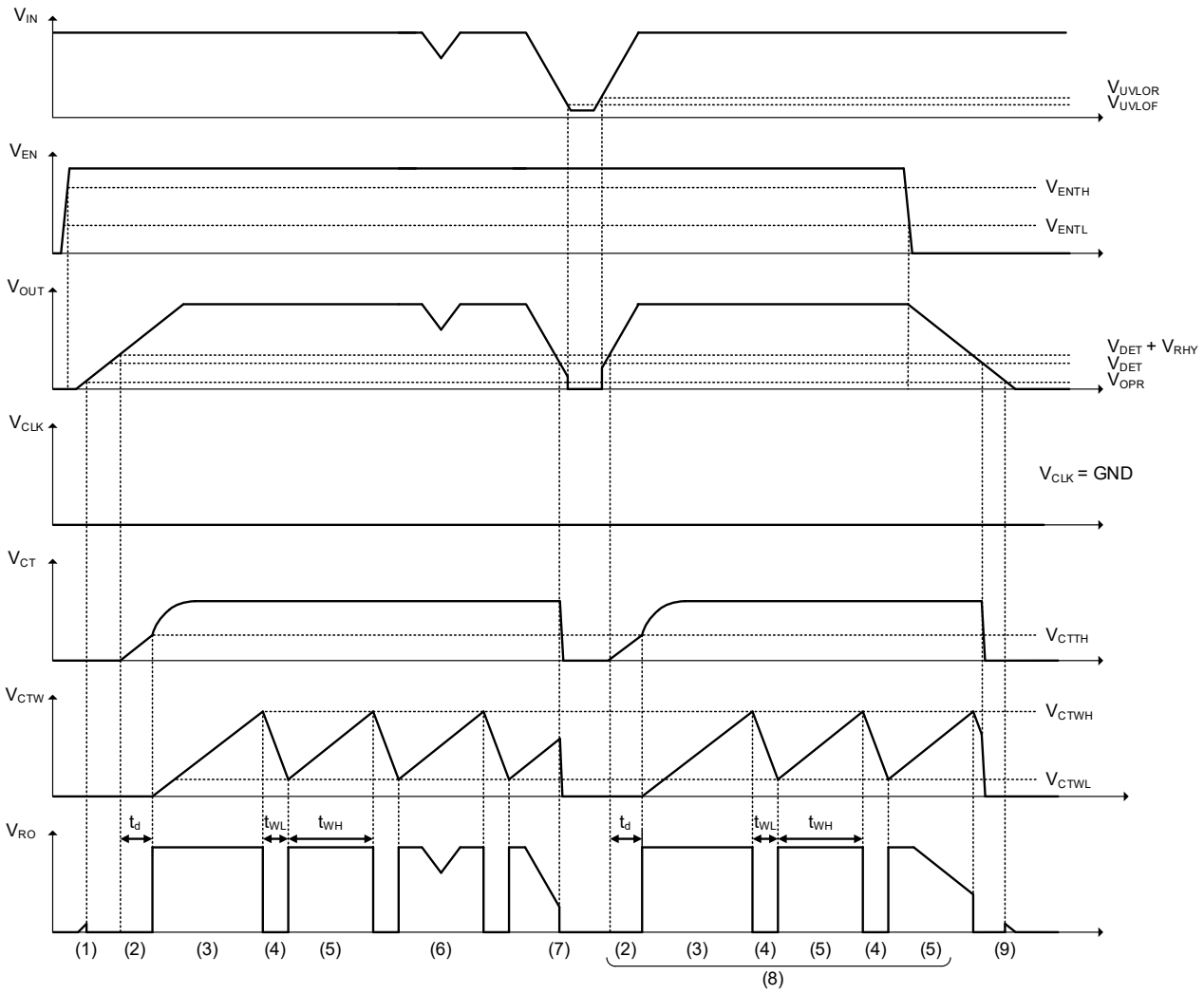
Measurement Setup for
Figure 71 to 74



Measurement Setup for
Figure 75 to 76

Timing Chart

1. EN ON/OFF



This page shows the details of RESET and WDT operation without CLK signal input.

(1) When a voltage equal to or greater than the UVLO turn-on threshold (V_{UVLOR}) is applied to the input pin, and a voltage equal to or greater than the EN ON threshold voltage (V_{ENTH}) is applied to the EN pin, the VOUT voltage is output. When VOUT voltage (V_{OUT}) reaches 1 V (V_{OPR}), RO outputs a LOW state.

(2) RESET starts operating when V_{OUT} becomes higher than the RESET detection voltage (V_{DET}) + RESET detection hysteresis (V_{RHY}), i.e. the reset state caused by low output is removed. When it starts, CT voltage is raised by charging C_{CT}, the external capacitor connected to the CT pin, with an internal constant current. If CT voltage reaches the high side threshold voltage, V_{CTTH}, RO outputs a HIGH state. The high state voltage level of RO is defined by the VOUT voltage at the pull-up destination. This time period, described in Timing Chart as (2), is called Delay Time L→H (t_D).

(3) WDT starts operating when V_{CT} reaches CT Threshold (V_{CTTH}). When it starts, CTW voltage is raised by charging the external capacitor connected to the CTW pin (C_{CTW}), with an internal constant current. If CTW voltage reaches the CTW Upper-side threshold (V_{CTWH}), the constant current state of CTW is switched from charging to discharging and RO outputs LOW state.

(4) Once C_{CTW} is discharged and V_{CTW} reaches the CTW Lower-side Threshold (V_{CTWL}), the constant current of CTW is switched from discharging to charging and RO outputs again HIGH state. This time period is described in Timing Chart as (4) is called WDT Reset Time (t_{WL}).

1. EN ON/OFF - continued

(5) When V_{CTW} reaches V_{CTWL}, the constant current of CTW is switched again from discharging to charging. Once C_{CTW} is charged again and V_{CTW} reaches V_{CTWH}, RO outputs a LOW state. This time period described in Timing Chart as (5) is called WDT Monitor Time (t_{WH}).

(6) When VOUT voltage fluctuates wherein $V_{OUT} > V_{DET}$, RESET function does not treat this as an abnormal state because VOUT voltage is still higher than RESET Detection Voltage, so RO keeps its HIGH state.

(7) If VOUT voltage changes below the V_{DET} threshold voltage, the CT and CTW pins will change their state to rapidly discharge C_{CT} and C_{CTW}. In this condition, regardless of whether the RO state is H or L, CT and CTW will be in their discharging states. RESET function treats this as an abnormal state because VOUT voltage is lower than RESET Detection Voltage causing RO to output LOW. It takes time to output LOW after detecting this abnormal state, and this time lag is called reaction time. Reaction time always exists in electronic circuit operation. For this reason, even with these products, it is necessary to consider reaction time for the following cases:
As a reference, 150 µs maximum reaction time is required for the RO pin to switch when VOUT voltage changes from V_{DET} + 0.5 V to V_{DET} - 0.5 V. Therefore, if instantaneous interruption of VOUT voltage is faster than reaction time, for example when voltage drops instantly, RESET may not operate correctly.
If instantaneous interruption may occur, countermeasures such as adding a capacitor between VOUT and GND and filtering voltage changes faster than reaction time are recommended.

(8) When RO outputs LOW and V_{CT} and V_{CTW} also enters LOW states after operation at (7), once VOUT voltage becomes higher than $V_{DET} + V_{RHY}$, WDT and RESET function restarts operating normally and continuously following the sequence: (2) → (3) → (4) → (5) → (4) → (5) …

(9) When VOUT voltage becomes lower than V_{DET} and then falls to LOW, the constant current of CT and CTW keep their discharging states to make CT and CTW voltages completely LOW. In this case (i.e. during the condition that $V_{OPR} < V_{OUT} < V_{DET}$), RO keep a LOW output state until VOUT voltage becomes lower than or equal to 1 V (V_{OPR}).

Each period time of t_D, t_{WH} and t_{WL} can be adjusted by choosing the values of the external capacitors CT, C_{CT} and CTW, C_{CTW}.

They can be calculated by following formulas:

$$t_D[s] \approx \frac{V_{CTTH}[V] \times C_{CT}[F]}{I_{CT\_C}[A]}$$

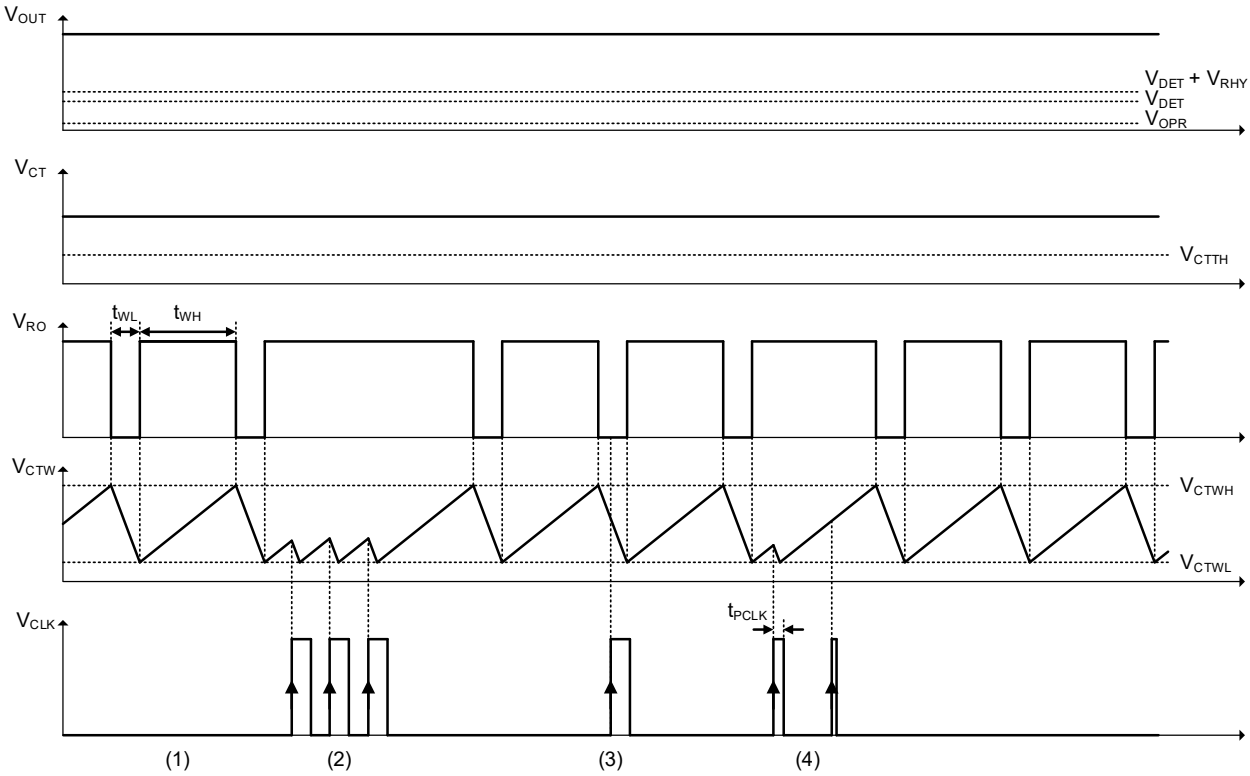
$$t_{WH}[s] \approx \frac{|V_{CTWH} - V_{CTWL}|[V] \times C_{CTW}[F]}{I_{CTW\_C}[A]}$$

$$t_{WL}[s] \approx \frac{|V_{CTWL} - V_{CTWH}|[V] \times C_{CTW}[F]}{I_{CTW\_D}[A]}$$

However, the calculated values using these formulas are just estimations. The value for CT and CTW capacitances shall be designed by the ratio calculation obtained by comparing the actual value to the value at the typical conditions with C_{CT} = 0.01 µF and C_{CTW} = 0.0047 µF as described in the Electrical Characteristics.

Timing Chart - continued

2. CLK ON/OFF



The WDT behavior when CLK input is operational is described as follows:

CLK input is acceptable only while RO outputs HIGH, i.e. during t_{WH}, for WDT.
When RO outputs LOW, i.e. during t_{WL}, t_D and other conditions, CLK input is not allowed.

(1) While RO outputs HIGH, if the input of a rising edge to the CLK pin is not supplied, CTW is kept in its charging state. If this state continues until V_{CTW} reaches V_{CTWH}, then the output of RO switches from HIGH to LOW. This state, called Timeout Failure, is when WDT does not detect the rising edge of CLK inputs from the microcomputer during the period defined by C_{CTW} capacitance.

(2) While RO outputs HIGH, if a rising edge is supplied to the CLK pin, WDT detects this and then it changes the CTW pin state from charging state to discharging state. Then when V_{CTW} reaches V_{CTWL} by the constant discharge current to C_{CTW}, CTW state changes back to the charging. RO can keep a HIGH output if CLK signal inputs with constant timing that keeps CTW state as charging.

(3) When RO outputs LOW, even if the rising edge supplies to the CLK pin, WDT does not detect the edge.

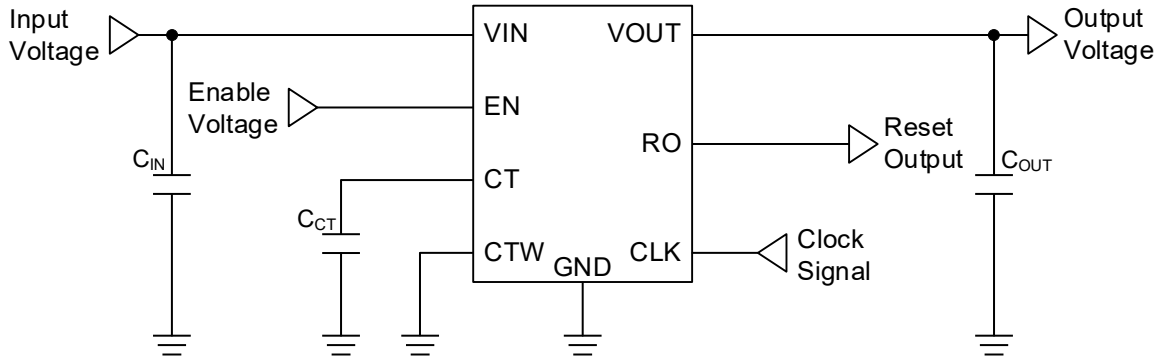
(4) The pulse width of CLK inputs, i.e. t_{PCLK}, must be always longer than or equal to 0.5 µs. If the pulse width of the signal applied to the CLK pin is shorter than t_{PCLK}, the CTW pin may not switch properly from charging to discharging.

Application Circuit Examples

Regarding cases when only the LDO and RESET functions are used, without using the WDT function

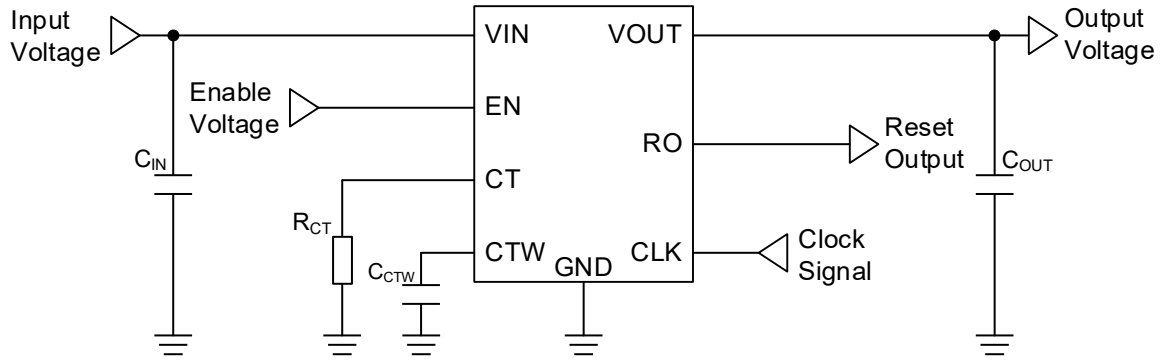
BD933F51EFJ-C, BD950F51EFJ-C, BD950F52EFJ-C don't have the INH Function*(Note 1)*, and the WDT is always ON. To disable the WDT function, short the CTW pin to the GND pin.

(Note 1) This function enables or disables the WDT.



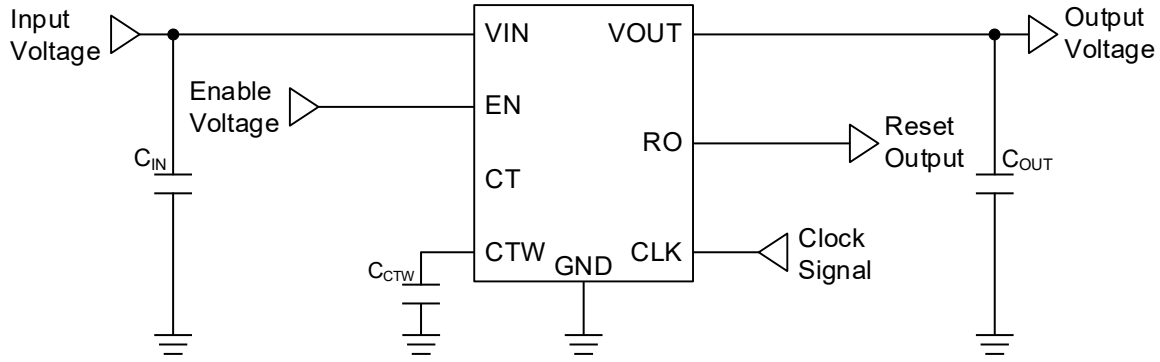
Manual Reset by external processing of the CT pin

By pulling down the CT pin to GND, it is possible to forcibly output a signal in the reset detection state. Pull down resistors(R_{CT}) can be 100 kΩ or less.



Regarding When Reset Delay Settings Are Not Required

The CT pin can be used in an open state. In that case, the RESET delay time is determined by the time required to charge the Ro pin and the operating speed of the internal circuit, with the internal circuit operation time being approximately 200 μs maximum.



Application and Implementation

Notice: The following information is given as a reference for the application and implementation. Therefore, they do not guarantee the product's operation on the specific function, accuracy, or external components in application. Application implementation shall be designed with sufficient margin by enough understanding about characteristics of the external components, e.g. capacitors, and by appropriate verification in the actual operating conditions.

Selection of External Components

Input Pin Capacitor

To fully ensure the proper performance of this IC, it is recommended that the input capacitor be placed as close as possible to the input pin and the GND pin without being affected by mounting impedance and that it be laid out on the same mounting surface. In this case, a capacitor with a capacitance of 0.1 µF (Min) or higher is recommended.
Depending on the layout of the peripheral components, including this IC, from the input power supply, for example, if the distance from the battery is too far or the impedance of the input side is too high, the current supply due to the load response of the IC cannot be withstood, and the output voltage may become unstable due to fluctuations in the input voltage. In such a case, it is necessary to use a large capacitor to prevent the line voltage from dropping. Select the capacitance of the input terminal capacitor according to the line impedance between the power-smoothing circuit and the input terminal and the load response required by the application.

In addition, careful consideration should be taken with the input pin capacitor to prevent influence on the regulator's characteristics by the deviation or the variation of the external capacitor's characteristic. All input capacitors mentioned above are recommended to have a good DC bias characteristic and a temperature characteristic (approximately ±15%, e.g. X7R, X8R) satisfying the high absolute maximum voltage rating based on EIA standard.

Output Pin Capacitor

An output capacitor is mandatory for the regulator to ensure stable operation. An output capacitor with capacitance of 0.23 µF (Min) or higher and ESR up to 400 mΩ (Max) is required between the output pin and the GND pin.

A proper selection of appropriate both the capacitance value and ESR for the output capacitor can improve the transient behavior of the regulator and can also keep the stability with better regulation loop. The correlation of the output capacitance value and ESR is shown on the graph on the next page as the **output capacitor's capacitance value and the stability region for ESR**. As described in this graph, this regulator is designed to be stable with ceramic capacitors (MLCC) capacitances 0.23 µF to 470 µF and with ESR within almost 0 Ω to 400 mΩ. The frequency range of ESR can be generally considered to be around 1 MHz.

Note that the provided stable area for the capacitance and ESR in the graph is obtained under a specific set of conditions which is based on the measurement results for a single IC on our board with a resistive load. In the actual environment, stability is affected by wire impedance on the board, input power supply impedance and load impedance. Therefore, note that a careful evaluation of the actual application, the actual usage environment, and the actual conditions should be done to confirm the actual stability of the system.

Generally, during transient events caused by the input voltage fluctuation or load fluctuation beyond the gain bandwidth of the regulation loop, the transient response ability of the regulator depends on the capacitance value of the output capacitor. Basically, a capacitance value of 0.23 µF (Min) or higher for the output capacitor is recommended as shown in the table on **Output Capacitance C_{OUT} and ESR Available Area**. Using higher capacitance values is expected to improve the transient response ability at high frequency. Various types of capacitors can be used for the output capacitors with high capacitances including electrolytic capacitors, electro-conductive polymer capacitors, and tantalum capacitors. Note, however, that depending on the type of capacitors, their characteristics such as ESR (≤ 400 mΩ), absolute value range, temperature dependency for the capacitance value and increased ESR at cold temperature need to be taken into consideration. When using capacitor with large ESR (≤ 400 mΩ), a ceramic capacitor with at least 0.23 µF of capacitance must be connected in parallel to keep stability. In this case, the total capacitance should be less than 470 µF.

In addition, the same consideration should be taken as with the input pin capacitor to prevent influence on the regulator's characteristics by the deviation or the variation of the external capacitor's characteristics. All output capacitors mentioned above are recommended to have good DC bias and temperature characteristics (approximately ±15 %, e.g. X7R, X8R) satisfying the high absolute maximum voltage rating based on EIA standard. These capacitors should be placed close to the output pin and mounted on the same board side of the regulator so as not to be influenced by mounting impedance.

Application and Implementation - continued

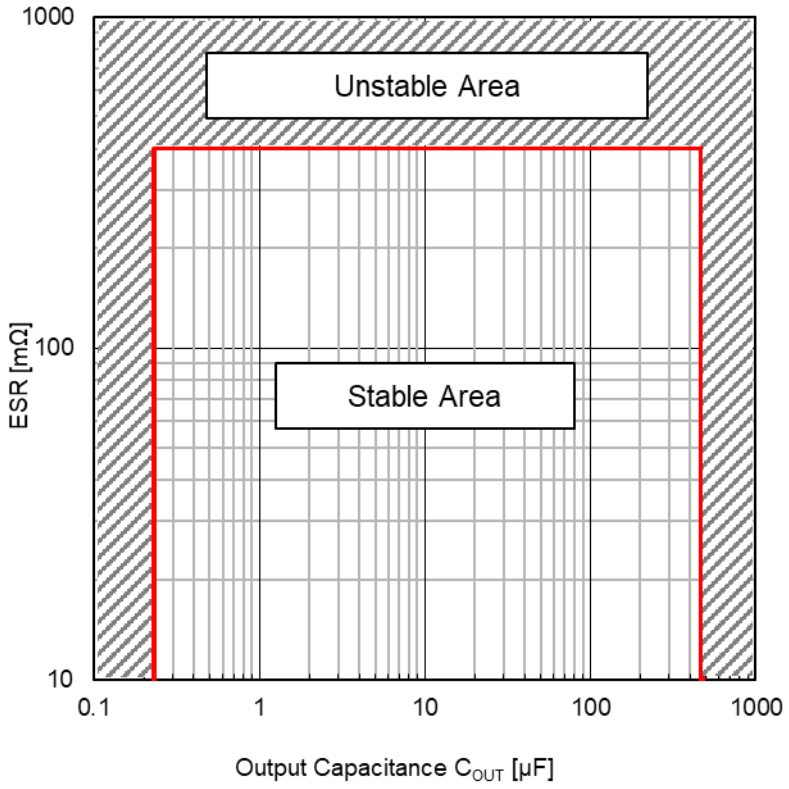


Figure 77. Output Capacitance C_{OUT}, ESR Available Area
(V_{IN} = 4.6 V to 42 V, V_{OUT} = 3.3 V*(Note 1)* , -40 °C ≤ Tj ≤ +150 °C, I_{OUT} = 0 mA to 500 mA)
(Note 1) The strictest theoretical conditions for stability of the regulator's control loop.

Typical Application

Parameter	Symbol	Reference Value for Application
Output Current Range	I_{OUT}	I_{OUT} ≤ 500 mA
Output Capacitor	C_{OUT}	0.47 µF
Input Voltage	V_{IN}	13.5 V
Input Capacitor*(Note 1)*	C_{IN}	1 µF
Enable Input Voltage	V_{EN}	5 V
CT Capacitor	C_{CT}	0.01 µF
CTW Capacitor	C_{CTW}	0.0047 µF

(Note 1) If the impedance or inductance of power supply line is high, adjust input capacitor value.
To avoid any malfunctions caused by input voltage drop on the power supply line, consider adjusting the impedance of power supply line and make it as small as possible.

Application and Implementation - continued

Surge Voltage Protection for Linear Regulators

The following shows some helpful tips to protect ICs from possible inputting surge voltage which exceeds absolute maximum ratings.

Positive Surge to the Input

If there is any potential risk that positive surges higher than absolute maximum ratings, it is applied to the input, a Zener Diode should be inserted between the VIN pin and the GND to protect the device as shown in Figure 78.

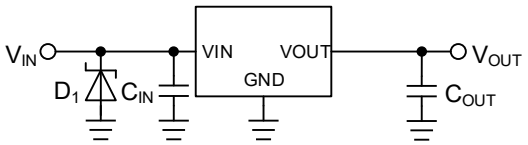


Figure 78. Surges Higher than Absolute Maximum Ratings is Applied to the Input

Negative Surge to the Input

If there is any potential risk that negative surges below the absolute maximum ratings, (e.g.) -0.3 V, is applied to the input, a Schottky Diode should be inserted between the VIN and the GND to protect the device as shown in Figure 79.

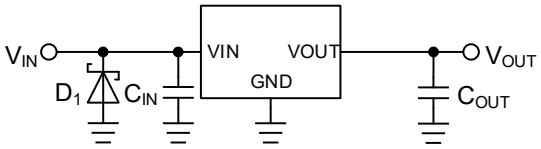


Figure 79. Surges Lower than -0.3 V is Applied to the Input

Reverse Voltage Protection for Linear Regulators

A linear regulator which is one of the integrated circuit (IC) operates normally on the condition that the input voltage is higher than the output voltage. However, it is possible to that an abnormal situation with specific conditions in which is the output voltage becomes higher than the input voltage. A reverse polarity connection between the input and the output might occur or a certain inductor component can also cause a polarity reversal conditions. If the countermeasure is not implemented, it may cause damage to the IC. The following shows some helpful tips to protect ICs from the reverse voltage occasion.

Protection against Reverse Input/Output Voltage

In the case that MOSFET is used for the pass transistor, a parasitic body diode between the drain-source generally exists. If the output voltage becomes higher than the input voltage and if its voltage difference exceeds V_F of the body diode, a reverse current flows from the output to the input through the body diode as shown in Figure 80. The current flows in the parasitic body diode is not limited in the protection circuit because it is the parasitic element, therefore too much reverse current may cause damage to degrade or destroy the semiconductor elements of the regulator.

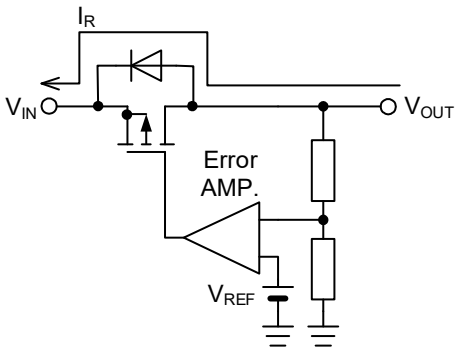


Figure 80. Reverse Current Path in a MOS Linear Regulator

Protection against Reverse Input/Output Voltage – continued

An effective solution for this problem is to implement an external bypass diode to prevent the reverse current flow inside the IC as shown in Figure 81. Especially in applications where the output voltage setting is high and a large output capacitor is connected, be sure to consider countermeasures for large reverse current values. Note that the bypass diode must be turned on prior to the internal body diode of the IC. This external bypass diode must turn on before the internal body diode, therefore it should have a lower forward voltage VF than the internal body diode. It should be selected as a diode which has a rated reverse voltage greater than the IC's rated input voltage and also which has a rated forward current greater than the anticipated reverse current in the actual application.

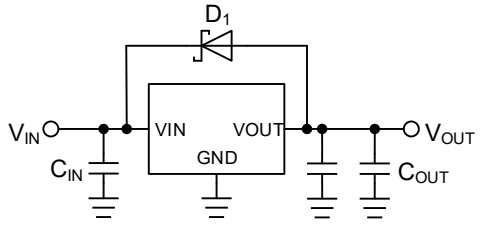


Figure 81. Bypass Diode for Reverse Current Diversion

A Schottky barrier diode which has a characteristic of low forward voltage (V_F) can meet the requirement for the external diode to protect the IC from the reverse current. However, it also has a characteristic that the leakage (I_R) caused by the reverse voltage is higher than other diodes. Therefore, careful consideration should be taken when choosing it because if I_R is large, it may cause increase of the current consumption, or raise of the output voltage in the light-load current condition. I_R characteristic of Schottky diode has positive temperature characteristic, which the details shall be checked with the datasheet of the products, and the careful confirmation of behavior in the actual application is mandatory.

Even in the condition when the input/output voltage is inverted, if the VIN pin is open as shown in Figure 82, or if the VIN pin becomes high-impedance condition as designed in the system, it cannot damage or degrade the parasitic element. It's because a reverse current via the pass transistor becomes extremely low. In this case, therefore, the protection external diode is not necessary.

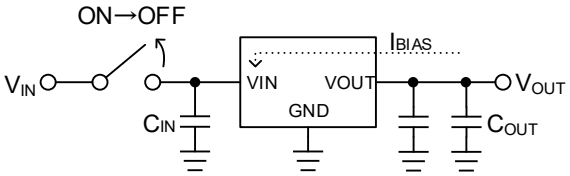


Figure 82. Open VIN

Protection against Input Reverse Voltage

When the input of the IC is connected to the power supply, if the plus and minus are routed in reverse accidentally, or if there is a possibility that the input may become lower than the GND pin, it may cause destruction to the IC because a large current can pass via the internal electrostatic breakdown prevention diode between the input pin and the GND pin inside the IC as shown in Figure 83.

The simplest solution to avoid this problem is to connect a Schottky barrier diode or a rectifier diode in series to the power supply line as shown in Figure 84. However, it increases power loss calculated as V_F x I_{CC}, and it also causes a voltage drop by the forward voltage V_F at the supply voltage while normal operation.
Generally, since the Schottky barrier diode has lower V_F, it contributes to smaller power losses than rectifier diodes. If IC has load currents, the required input current to the IC is also bigger. In this case, this external diode generates more heat, therefore select a diode with enough margin for power dissipation. On the other hand, on reverse connection conditions, a reverse current passes through this diode. However, it is negligible because in its small amount.

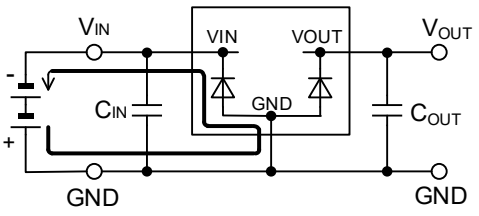


Figure 83. Current Path in Reverse Input Connection

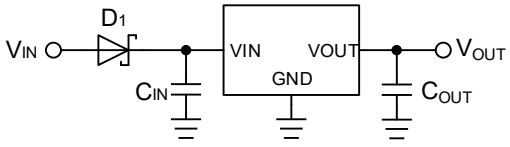


Figure 84. Protection against Reverse Polarity 1

Protection against Input Reverse Voltage - continued

Figure 85 shows a circuit in which a P-channel MOSFET is connected in series to power. The body diode (parasitic element) is located in the drain-source junction area of the MOSFET. The voltage drop in forward connection is calculated from the on state resistance of the MOSFET and the output current I_{OUT}. It is smaller than the voltage drop by the diode as shown in Figure 84 and results in less of a power loss. No current flows in a reverse connection where the MOSFET remains off in Figure 85.

If the gate-source voltage exceeds maximum rating of MOSFET gate-source junction with derating curve in consideration, reduce the gate-source junction voltage by connecting resistor voltage divider as shown in Figure 86.

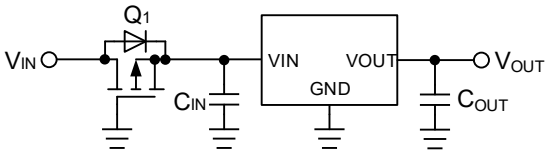


Figure 85. Protection against Reverse Polarity 2

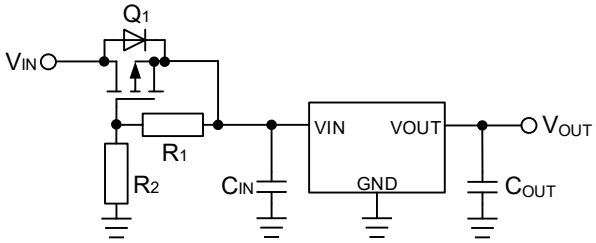


Figure 86. Protection against Reverse Polarity 3

Protection against Reverse Output Voltage when Output Connect to an Inductor

If the output load is inductive, electrical energy accumulated in the inductive load is released to the ground at the moment that the output voltage is turned off. IC integrates ESD protection diodes between the IC output and ground pins. A large current may flow in such condition finally resulting in the destruction of the IC. To prevent this situation, connect a Schottky barrier diode in parallel to the integrated diodes as shown in Figure 87.

Further, if a long wire is in use for the connection between the output pin of the IC and the load, confirm that the negative voltage is not generated at the VOUT pin when the output voltage is turned off by observing its waveform on an oscilloscope since it is possible that the load becomes inductive. An additional diode is required for a motor load that is affected by its counter electromotive force, as it produces an electrical current in a similar way.

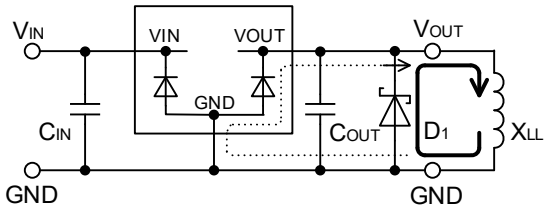


Figure 87. Current Path in Inductive Load (Output: Off)

Power Dissipation

■HTSOP-J8

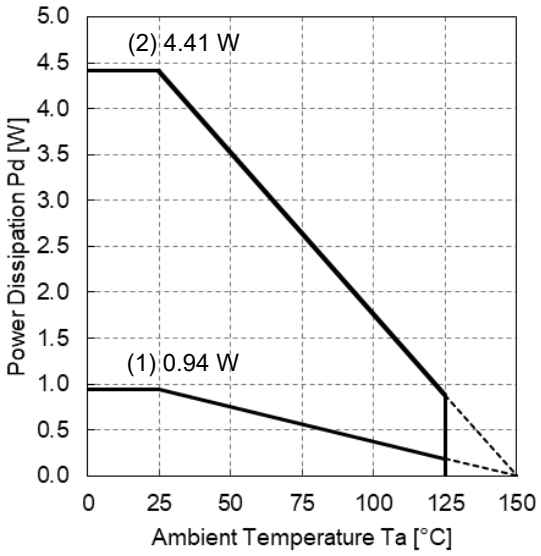


Figure 88. Power Dissipation Graph (HTSOP-J8)

(1): 1-layer PCB
(Copper foil area on the reverse side of PCB: 0 mm x 0 mm)
Board material: FR-4
Board size: 114.3 mm x 76.2 mm x 1.57 mmt
Top copper foil: ROHM-recommended footprint
+ wiring to measure, 70 µm. copper.

(2): 4-layer PCB
(Copper foil area on the reverse side of PCB: 74.2 mm x 74.2 mm)
Board material: FR-4
Board size: 114.3 mm x 76.2 mm x 1.60 mmt
Top copper foil: ROHM-recommended footprint
+ wiring to measure, 70 µm. copper.
2 inner layers copper foil area of PCB:
74.2 mm x 74.2 mm, 35 µm. copper.
Copper foil area on the reverse side of PCB:
74.2 mm x 74.2 mm, 70 µm. copper.

Condition (1): θ_{JA} = 132.6 °C/W, Ψ_{JT} (top center) = 14 °C/W
Condition (2): θ_{JA} = 28.3 °C/W, Ψ_{JT} (top center) = 5 °C/W

Thermal Design

This product exposes a frame on the back side of the package for thermal efficiency improvement. The power consumption of the IC is decided by the dropout voltage condition, the load current and the current consumption. Refer to power dissipation curves illustrated in Figure 88 when using the IC in an environment of Ta ≥ 25 °C. Even if the ambient temperature Ta is at 25 °C, chip junction temperature (Tj) can be very high depending on the input voltage and the load current. Consider the design to be Tj ≤ Tjmax = 150 °C in whole operating temperature range.
Should by any condition the maximum junction temperature Tjmax = 150 °C rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Therefore, care should be taken because its characteristics might be different from the actual conditions in usage. Verify the application and allow sufficient margins in the thermal design by the following method to calculate the junction temperature Tj. Tj can be calculated by either of the two following methods.

1. The following method is used to calculate the junction temperature Tj with ambient temperature Ta.

$$Tj = Ta + P_C \times \theta_{JA} \text{ [°C]}$$

Where:

Tj is the Junction Temperature
Ta is the Ambient Temperature
P_C is the Power Consumption
θ_{JA} is the Thermal Resistance (Junction to Ambient)

2. The following method is also used to calculate the junction temperature Tj with top center of case's (mold) temperature T_T.

$$Tj = T_T + P_C \times \Psi_{JT} \text{ [°C]}$$

Where:

Tj is the Junction Temperature
T_T is the Top Center of Case's (mold) Temperature
P_C is the Power Consumption
Ψ_{JT} is the Thermal Resistance (Junction to Top Center of Case)

The following method is used to calculate the power consumption Pc (W).

$$Pc = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{CC} \text{ [W]}$$

Where:

P_C is the Power Consumption
V_{IN} is the Input Voltage
V_{OUT} is the Output Voltage
I_{OUT} is the Load Current
I_{CC} is the Current Consumption

Calculation Example (HTSOP-J8)
If V_{IN} = 13.5 V, V_{OUT} = 5.0 V, I_{OUT} = 100 mA, I_{CC} = 224 μA, the power consumption Pc can be calculated as follows:

$$\begin{aligned} P_C &= (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{CC} \\ &= (13.5\,V - 5.0\,V) \times 100\,mA + 13.5\,V \times 224\,\mu A \\ &= 0.85\,W \end{aligned}$$

At the maximum ambient temperature Tamax = 85 °C,
the thermal impedance (Junction to Ambient) θ_{JA} = 28.3 °C/W (4-layer PCB)

$$\begin{aligned} Tj &= Tamax + P_C \times \theta_{JA} \\ &= 85\,°C + 0.85\,W \times 28.3\,°C/W \\ &= 109.1\,°C \end{aligned}$$

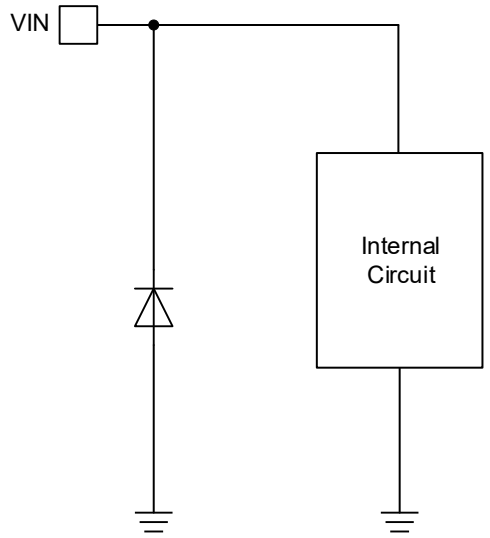
When operating the IC, the top center of case's (mold) temperature T_T = 100 °C, Ψ_{JT} = 14 °C/W (1-layer PCB)

$$\begin{aligned} Tj &= T_T + P_C \times \Psi_{JT} \\ &= 100\,°C + 0.85\,W \times 14\,°C/W \\ &= 111.9\,°C \end{aligned}$$

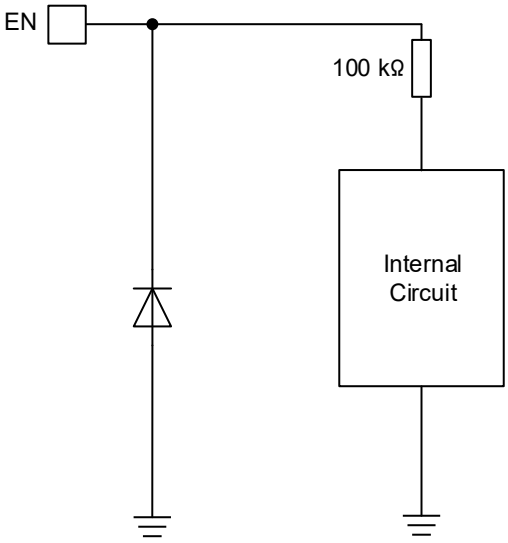
If it is difficult to ensure the margin by the calculations above, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad for optimum thermal performance.

I/O Equivalence Circuit

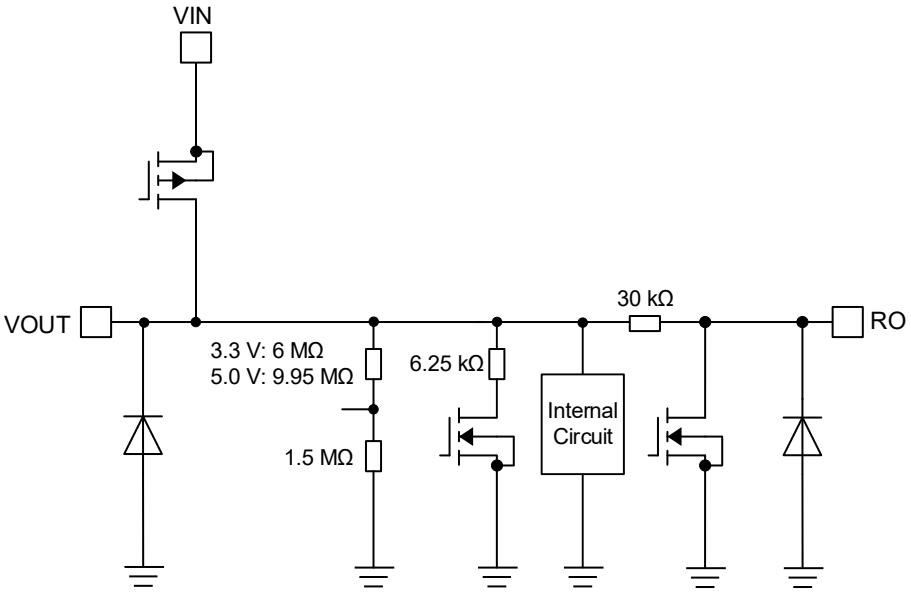
VIN



EN

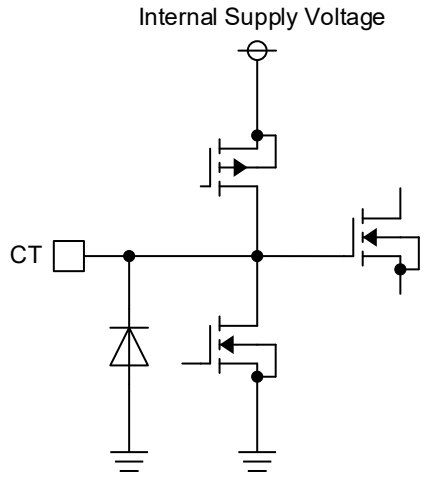


VOUT / RO

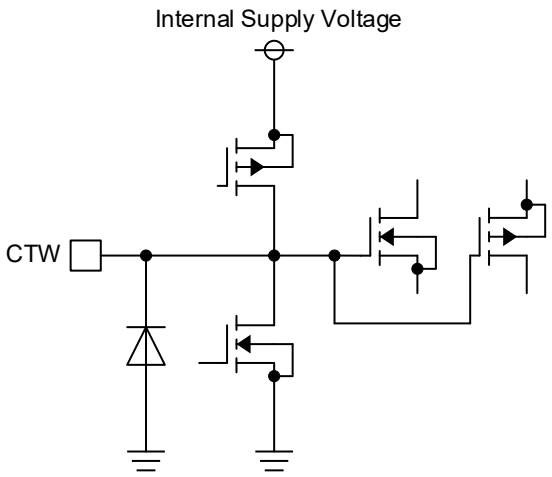


I/O Equivalence Circuit - continued

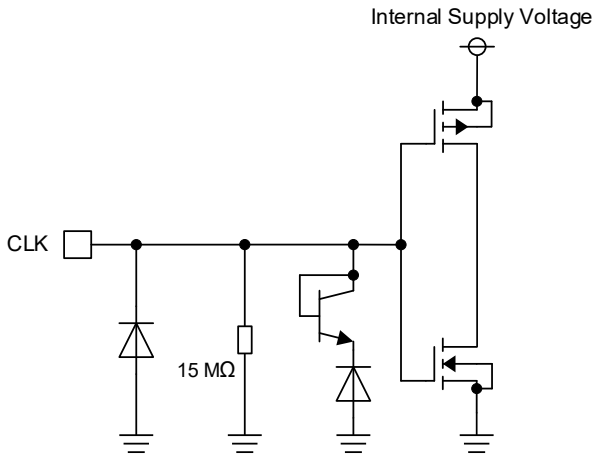
CT



CTW



CLK



Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Thermal Consideration**
   The power dissipation under actual operating conditions should be taken into consideration and a sufficient margin should be allowed in the thermal design. On the reverse side of the package this product has an exposed heat pad for improving the heat dissipation. The amount of heat generation depends on the voltage difference between the input and output, load current, and bias current. Therefore, when actually using the chip, ensure that the generated heat does not exceed the Pd rating. If Junction temperature is over Tjmax (=150 °C), IC characteristics may be worse due to rising chip temperature. Heat resistance in specification is measurement under PCB condition and environment recommended in JEDEC. Ensure that heat resistance in specification is different from actual environment.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

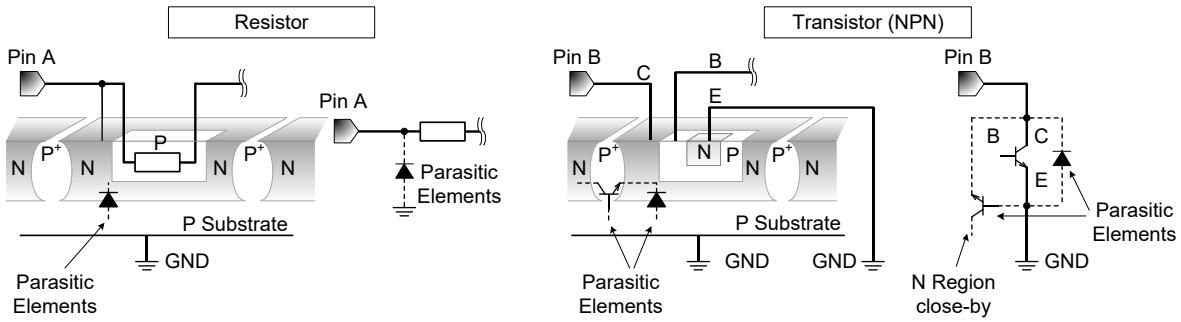


Figure 89. Example of Monolithic IC Structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Thermal Shutdown Protection Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

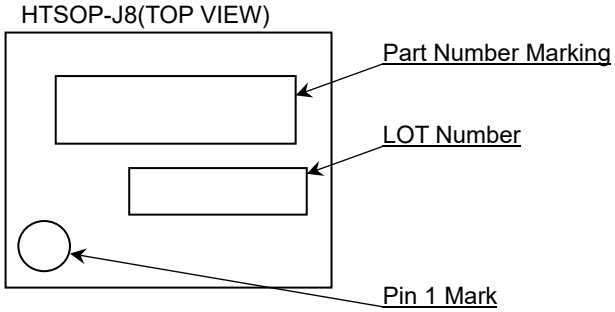
15. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*"
A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.
"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"
A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.
"Functional Safety Supportive Automotive Products"
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.
Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

ROHM launched the ComfySIL™ brand for customers involved in the design of functional safety to use products that support SIL (Safety Integrity Level) in a 'Comfy' (comfortable) manner, and for social systems' greater safety, security, and convenience to which ROHM can contribute through its products. ComfySIL™ is awarded to products that conform to the ComfySILTM concept for functional safety in the industrial equipment and automotive markets.

ComfySIL Functional Safety

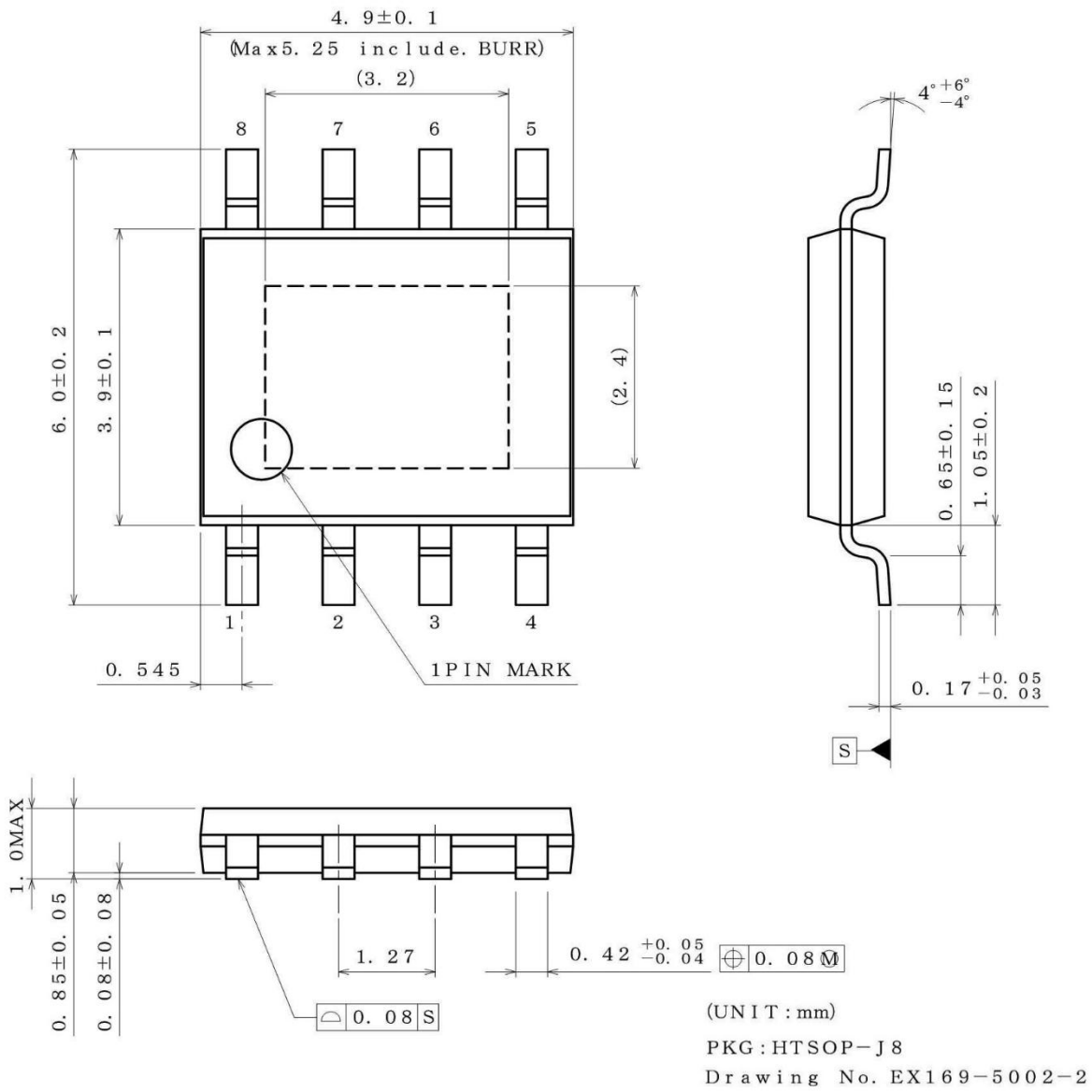
Marking Diagrams



Part Number	Part Number Marking	Output Voltage [V]	RESET Detection Voltage [V]
BD933F51EFJ-CE2	933F51	3.3	2.9
BD950F52EFJ-CE2	950F52	5.0	4.1
BD950F51EFJ-CE2	950F51	5.0	4.6

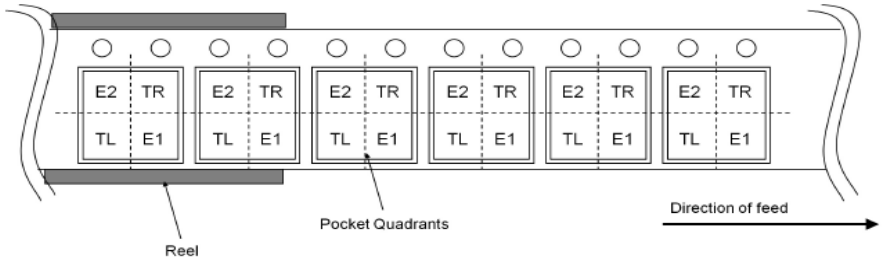
Physical Dimension and Packing Information

Package Name	HTSOP-J8



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
12.Feb.2026	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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